N11 Series

Hardware User Guide

Issue 1.5 Date 2020-09-18

Notice

This document provides a guide for users to use the N11 Series.

This document is intended for system engineers (SEs), development engineers, and test engineers.

THIS GUIDE PROVIDES INSTRUCTIONS FOR CUSTOMERS TO DESIGN THEIR APPLICATIONS. PLEASE FOLLOW THE RULES AND PARAMETERS IN THIS GUIDE TO DESIGN AND COMMISSION. NEOWAY WILL NOT TAKE ANY RESPONSIBILITY OF BODILY HURT OR ASSET LOSS CAUSED BY IMPROPER OPERATIONS.

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About This Document

Scope

This document is applicable to the N11 Series.

It defines the features, indicators, and test standards of the N11 Series module and provides reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2018-03	Initial draft	Wang Qiang
1.1	2018-03	Modified the signal	Zhuo JianZheng
1.2	2018-09	Added N11 V2	Zhuo JianZheng
1.3	2018-11	• Corrected SIM design • Added guidelines to reference designs • Added antenna matching	Zhuo JianZheng
1.4	2019-06	Modified supply voltage	Gong Hualiang
1.5	2019-10	Modified the description of UART port	Gong Hualiang

Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.

	This means the reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

Related Documents

*Neoway*_N11 Series_*Datasheet*

*Neoway*_N11 Series_*Product_Specifications*

*Neoway*_N11 Series_*AT_Command_Mannual*

*Neoway*_N11 Series_*EVK_User_Guide*

1 About N11

N11 is a compact wireless GSM/GPRS module. It provides high-quality SMS and data services. N11 is widely used in industrial and consumer applications.

N11 series include two variants: N11 and N11 V2. These two variants are completely compatible with each other in pin definition, packaging, and electric features. In this document, N11 refers to both variants if not specified.

1.1 Overview

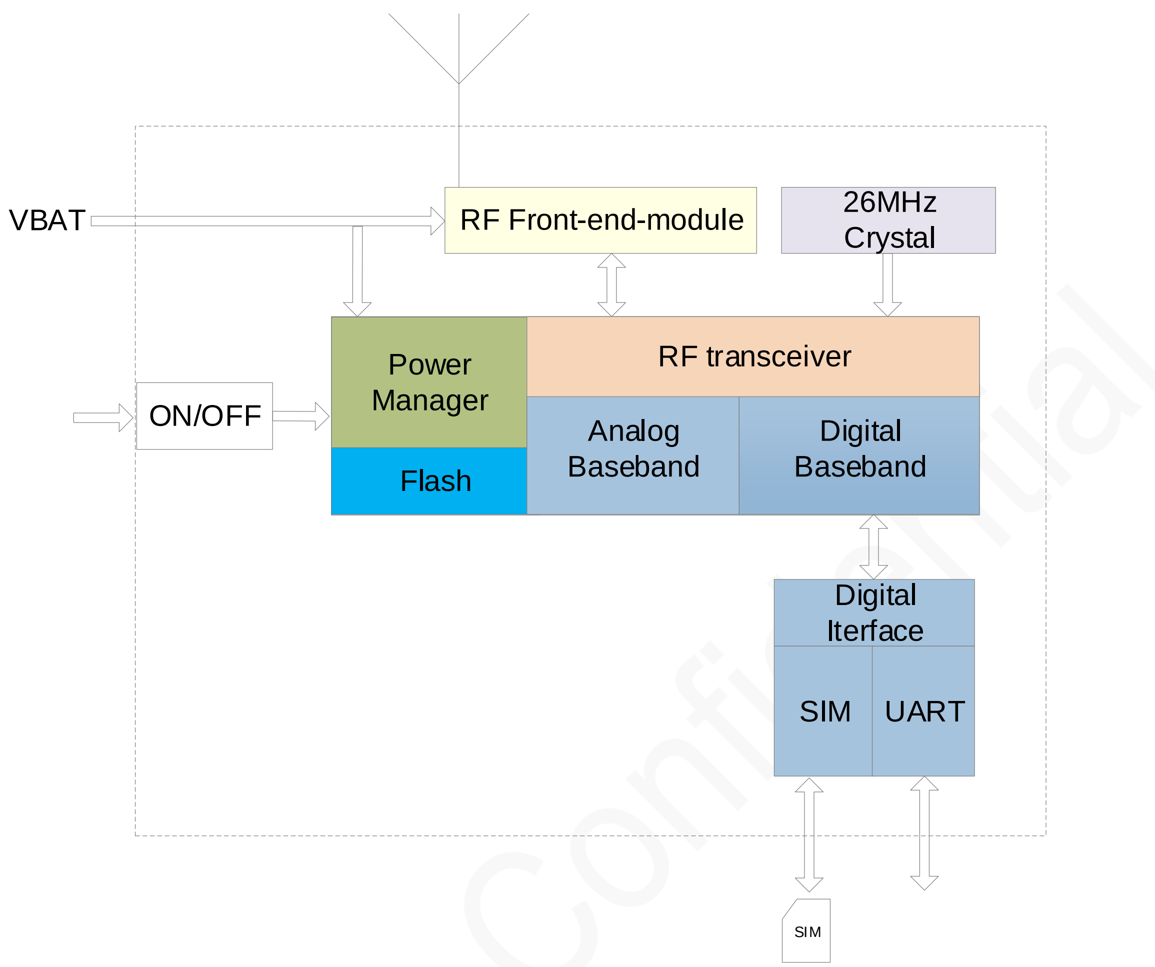
The N11 module adopts a 20-pin LGA package and its dimensions are 15.8 mm x 13.8 mm x 2.5 mm, which can meet most customer requirements for space reduction. It has the following hardware resources and features:

- UART interface, used for data communication, software upgrade and debugging
- Support SIM card 1.8/3.0V self-adaption
- Support RING (incoming call and SMS reminder)/NET_LIGHT (network indicator)/DTR (sleep mode) function

1.2 Block Diagram

The N11 module consists of a baseband controller, Flash ROM, RF section, application interfaces, etc. All sections coordinate with each other to provide such communication functions as GPRS data. Its design block diagram is shown in Figure 1-1.

Figure 1-1 N11 Block Diagram



1.3 Specifications

Table 1-1 N11 Specifications

Specifications	Description
Dimensions	(15.8±0.1) mm x (13.8±0.1) mm x (2.5±0.2) mm (H x W x D)
Weight	1.3 g
Package	20-pin LGA
Operating Temperature	-40 ºC to +85 ºC
Operating Voltage	3.4 V to 4.3 V (3.9 V is recommended)
Peak Current	Max 2.0 A
Operating Current (Idle)	11 mA
Current in Sleep Mode	• < 2.5 mA (on live network) • < 1.1 mA (through instrument, DRX=9)

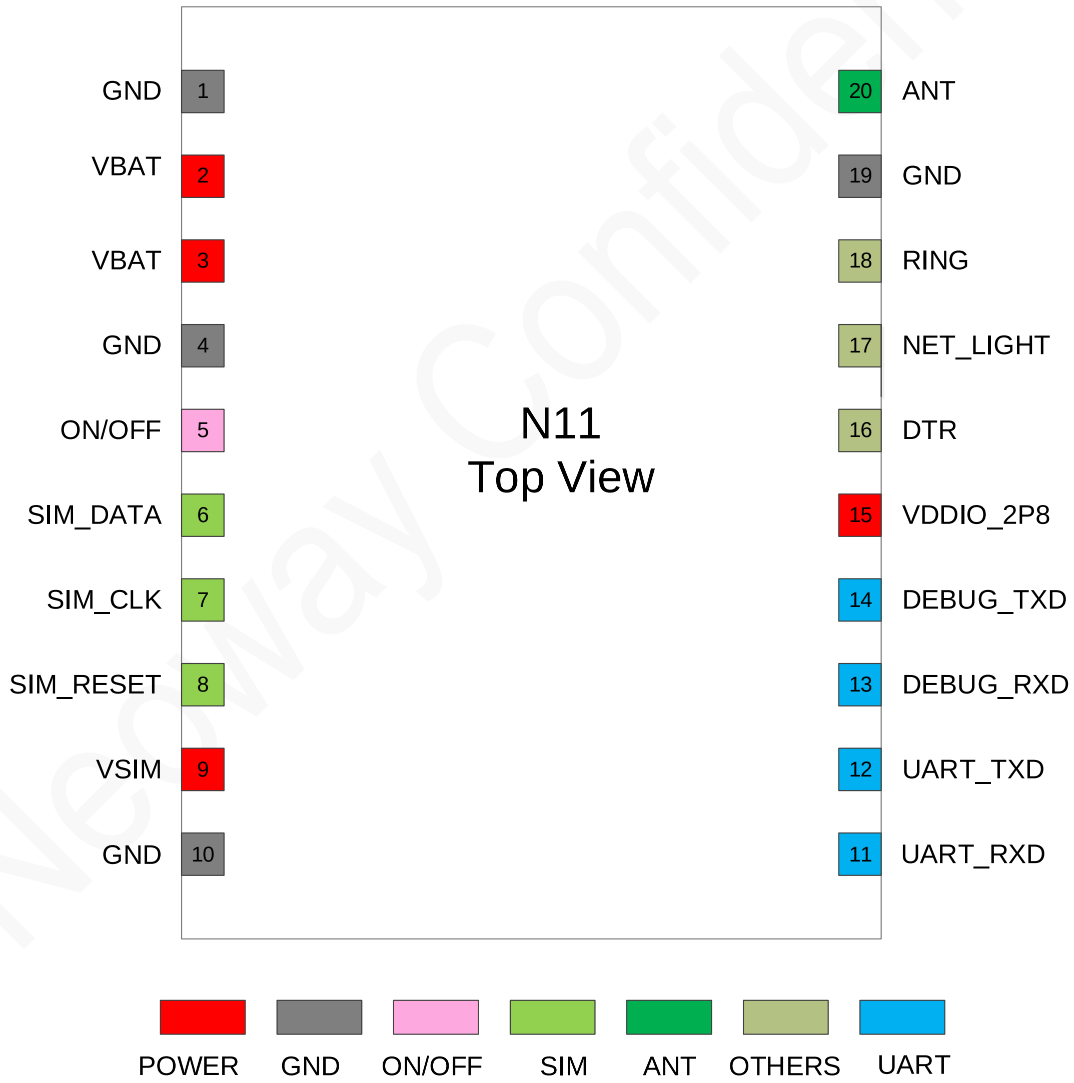
Frequency band	GSM850/EGSM900/DCS1800/PCS1900
Sensitivity	< -108 dBm
Transmit power	• GSM850/EGSM900 Class4(2W) • DCS1800/PCS1900 Class1(1W)
Protocol	Support GSM/GPRS Phase2/2+
AT commands	• GSM07.07 • Extended AT commands
SMS	• Support PDU and TEXT mode • Support SMS message receiving/sending and alerts for new SMS messages • Support SMS message management: reading/deleting/storage/list
GPRS Features	• Support GPRS CLASS 12 • Theoretical maximum uplink transmission rate: 85.6 Kbit/s • Theoretical maximum downlink transmission rate: 85.6 Kbit/s • Embedded TCP/IP protocol, support multi-link • Support server and client mode
UART	• Support AT command sending, data transmission, and firmware download • Support baud rate from 9600 bit/s to 115200 bit/s
Antenna Feature	50 Ω characteristic impedance

2 Pin Description

There are 20 pins on N11 and their pads are introduced in the LGA package. This chapter describes its pin definition and features.

2.1 Pin Allocation

Figure 2-1 Top view of N11 module



2.2 Pin Definition

Table 2-1 IO types

IO Type	Description
P	Power supply
NC	Not supported and must leave floating
DI	Digital signal input
DO	Digital signal output
AI	Analog signal input
AO	Analog signal output

Table 2-2 N11 Pin definition

Pin	Pin Name	I/O	Function	Level Feature (V)	Remarks
Power supply and Switch Interfaces					
2, 3	VBAT	P	Power supply input		3.4 V to 4.3 V (3.9 V is recommended)
1, 4, 10, 19	GND	P	Ground		
5	ON/OFF	DI	ON/OFF input	$0<V_{IL}<0.6$; $2.1<V_{IH}<VBAT$	Low-level pulse triggers the ON/OFF state.
15	VDDIO_2P8	P	2.8V power supply output		Used only for level shifting and to supply power for IO. Load capacity < 50 mA
UART Interface					
12	UART_TXD	DO	UART data transmit	$0<V_{IL}<0.6$; $2.1<V_{IH}<3.1$; $0<V_{OL}<0.42$; $2.38<V_{OH}<2.8$	N11: used for AT command issuing, firmware download, and calibration & final test N11 V2: used for AT command issuing
11	UART_RXD	DI	UART data receive		
SIM Card					
6	SIM_DATA	DI/O	SIM card data	$0<V_{IL}<0.25*VSIM$; $0.75*VSIM<V_{IH}<VSIM$; $0<V_{OL}<0.15*VSIM$;	Compatible with 1.8/3.0 V SIM card
7	SIM_CLK	DO	SIM card clock		
8	SIM_RESET	DO	SIM card reset		

9	VSIM	P	SIM card power output	0.85*VSIM<V_{OH}<VSIM	
Network indicator					
17	NET_LIGHT	DO	Network status LED	2.8 V/4 mA output	Used with AT commands
SMS and Call Reminder					
18	RING	DO	Ring output	0<V_{IL}<0.6; 2.1<V_{IH}<3.1; 0<V_{OL}<0.42; 2.38<V_{OH}<2.8	Detect incoming voice calls or SMS messages
Sleep Mode Control					
16	DTR	DI	Sleep mode control	0<V_{IL}<0.6; 2.1<V_{IH}<3.1; 0<V_{OL}<0.42; 2.38<V_{OH}<2.8	Used together with AT commands
GPRS Antenna					
20	ANT	AI/O	GPRS antenna interface		50 Ω impedance
Reserved Pins					
13	DEBUG_TXD	DO			N11: used to capture log; can be configured as AT port by software N11 V2: used for download, and calibration & final test
14	DEBUG_RXD	DI			

The maximum input voltage at all IO ports (including peak signal current) cannot exceed 3.1 V because the module uses a 2.8 V IO power system. In the application of the module, the IO output voltage from the 3.3 V power supply system of the external circuit might greatly overshoot 3.1 V due to the signal integrity design. In this situation, the IO pins of the module might be damaged if the IO signals are connected to the IO port on the 2.8 V systems. To rectify this issue, take measures to match the level. For details, see the 3.2 UART.

3 Application Interfaces

N11 provides power supply and control, communications, RF, and other interfaces to meet customers' requirements in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

3.1 Power Supply

Schematic design and PCB layout of power supply are the most critical process in application design and determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Table 3-1 Power supply and switch interface

Pin	Signal	I/O	Function	Remarks
2, 3, 4	VBAT	P	Main power supply input	3.4 V to 4.3 V (3.9 V is recommended)
1, 4, 10, 19	GND	P	Ground	
5	ON/OFF	DI	ON/OFF input	Low-level triggers ON/OFF state.

3.1.2 VBAT

The power supply design consists of two parts: schematic design and PCB layout.

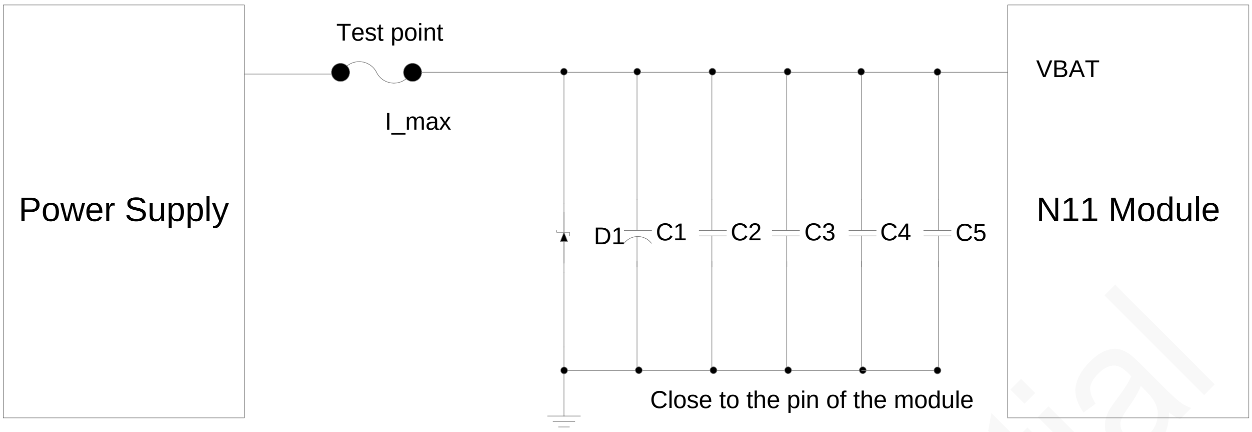
Schematic Design

Design the circuit of the power supply for N11 based on the input voltage you choose. Generally, there are three types of input voltages:

- 3.4 V to 4.3 V (3.9 V typically, output by cellphone battery)
- 4.3 V to 5.5 V (5.0 V typically, output by computer through USB)
- 5.5 V to 24 V (12 V typically, output by automotive battery)

Figure 3-1 shows a schematic design recommended for 3.4 V to 4.3 V input.

Figure 3-1 Recommended design 1

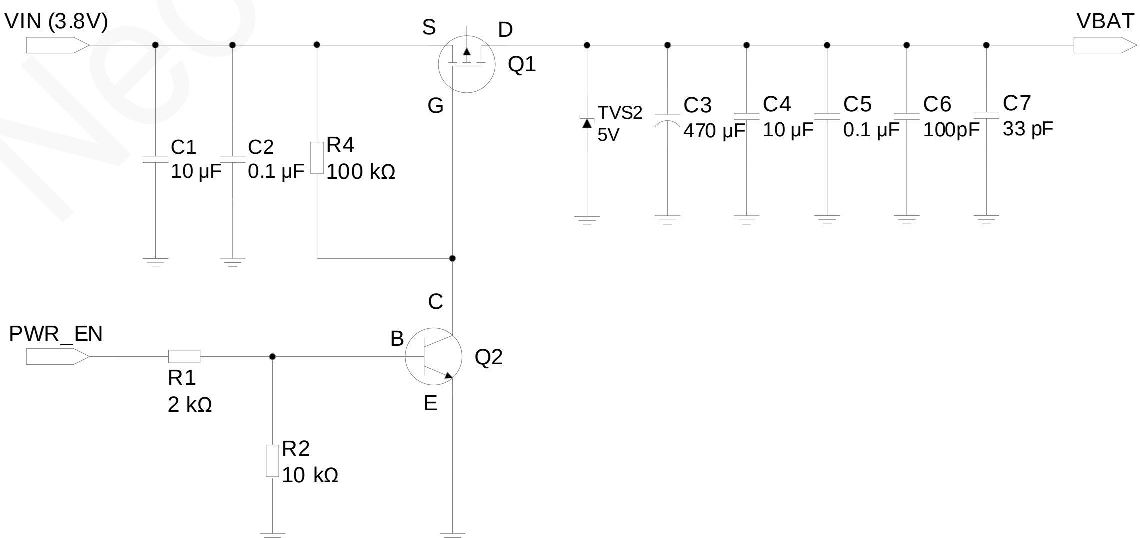


- The maximum input voltage for the module is 4.3 V and the typical value is 3.9 V.
- SMF5.0AG (Vrwm=5V&Pppm=200W) is recommended at D1. The protection voltage across D1 should not exceed the maximum input voltage the module can bear.

  Place the TVS diode close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be larger than 1.5 times the voltage across the power supply.
- Place low-ESR bypass capacitors close to the module to filter out high-frequency noise from the power supply.

A controllable power supply is preferable if the module is used in harsh conditions. Figure 3-2 shows the recommended schematic design.

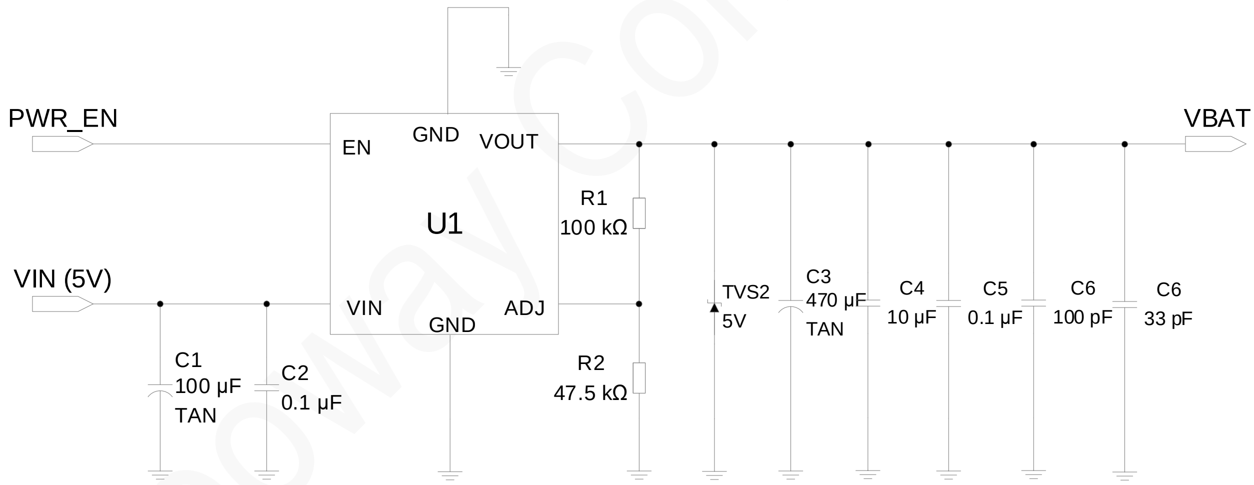
Figure 3-2 Recommended design 2



- Select an enhanced p-MOSFET at Q1, of which the maximum safe operating voltage and drain current is high and Rds. is low.
- Select a common NPN bipolar transistor or a digital NPN bipolar transistor at Q2. If selecting common NPN bipolar transistor, reserve enough tolerances of resistors at R1 and R2 in design, especially for the situation in which the operating voltage of the bipolar transistor might increase in low temperature.
- Place TVS2 close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Place C3 close to the module. A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be larger than 1.5 times the voltage across the power supply.
- Place low-ESR bypass capacitors close to the module to filter out high-frequency noise from the power supply.

The following design is recommended for 4.3 V to 5.5 V input.

Figure 3-3 Recommended design 3



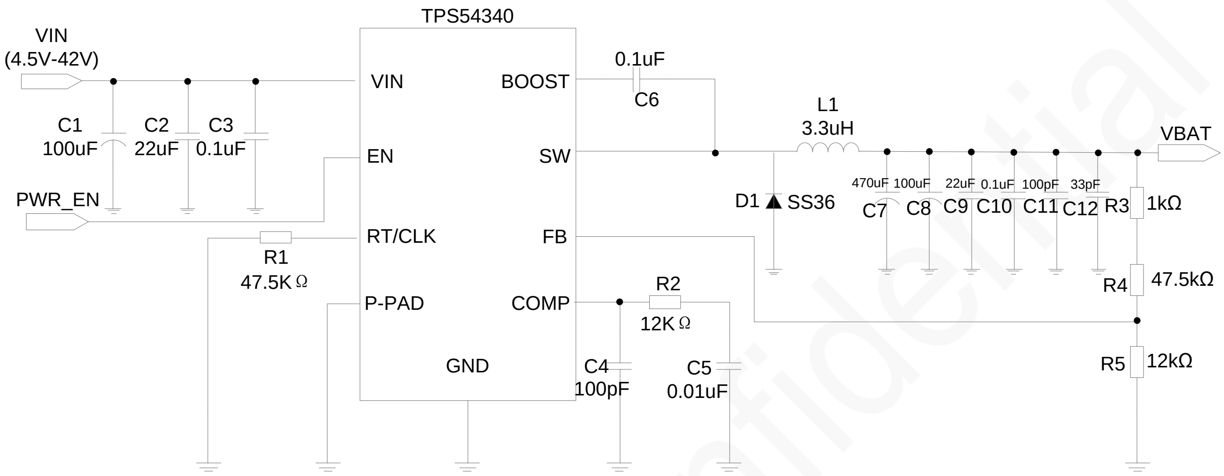
- Design with LDO is simpler and more efficient when the output of the power supply is close to the permissible voltage across VBAT.
- Select an LDO that can output a current larger than 2 A at U1 to ensure the performance of the module. MIC29302WU is recommended.
- Place TVS2 close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Place C3 close to the module. A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected to reduce voltage drops during bursts. Its

maximum safe operating voltage should be larger than 1.5 times the voltage across the power supply.

- Place low-ESR bypass capacitors close to the module to filter out high-frequency noise from the power supply.

The following design is recommended for 5.5 V to 24 V input.

Figure 3-4 Recommended design 4



- Select DC-DC that outputs a maximum current larger than 2 A when the output of power supply is much larger than the permissible voltage across VBAT.
- 500 kHz or higher switching frequency is recommended for DC-DC.
- The switching frequency of DC-DC might produce EMC noise and it determines the performance of end products.
- Add surge protection to the front end of the power supply circuit if automotive battery supplies power. The maximum safe operating voltage of the component should be larger than 42 V.
- Place TVS2 close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Place C7 close to the module. A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected to reduce voltage drops during bursts. Its maximum safe operating voltage should be larger than 1.5 times the voltage across the power supply.
- Place low-ESR bypass capacitors close to the module to filter out high-frequency noise from the power supply.

PCB Layout Guidelines

- TVS diodes dissipate the transient pulse power during a surge and have a short response time. Place the TVS as close to the interface as possible to ensure that the surge voltage can be clamped before the pulse is coupled to the neighbor traces.

- Place filer capacitors close to the power pin of the module to filter out the high-frequency noise from the power supply.
- Ensure that the width of PCB traces for VBAT circuits allows 2 A current and ensure no obvious decrease of loop voltages. Trace width of VBAT should be at least 2 mm and the ground plane should be as complete as possible. The traces of the power supply circuit should be as short and wide as possible.
- Noise-sensitive circuits such as audio and RF should be placed far away from power supply circuits, especially when the DC-DC is adopted in the design.
- Ensure that the loop is minimum in design with DC-DC since the frequency is high at the SW pin. Place sensitive components far away from the SW pin in case of noise coupling. Place feeding components as close to FB pin and COMP pin as possible.
- Connect GND pins and bottom pads to the ground to optimize heat sink and separate noise.

In GSM/GPRS mode, RF data is transmitted in burst mode that generates voltage drops on the power supply. Furthermore, this results in a 216 Hz noise through the power and the transient peak current is up to 2A. Ensure low resistance of power supply trace in design to avoid voltage drop.

Never use a diode to make the drop voltage between a higher input and module power. Otherwise, Neoway will not provide a warranty for product issues caused by this. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, because the forward voltage of the diode will vary greatly in different temperature and current. The module might not work properly with a diode power supply.

3.1.3 VDDIO_2P8

N11 provides one VDDIO_2P8 pin that outputs 2.8 V@50 mA.

It is recommended that VDDIO_2P8 is used only for level shifting and IO power supply.

3.1.4 On/Off Control and Procedure

Prior to turning on the module, power on the host MCU and finish the UART initialization. Otherwise, conflictions may occur during initialization, due to unstable conditions. ON/OFF is a pin triggered by a negative pulse and used to turn on or off the module.

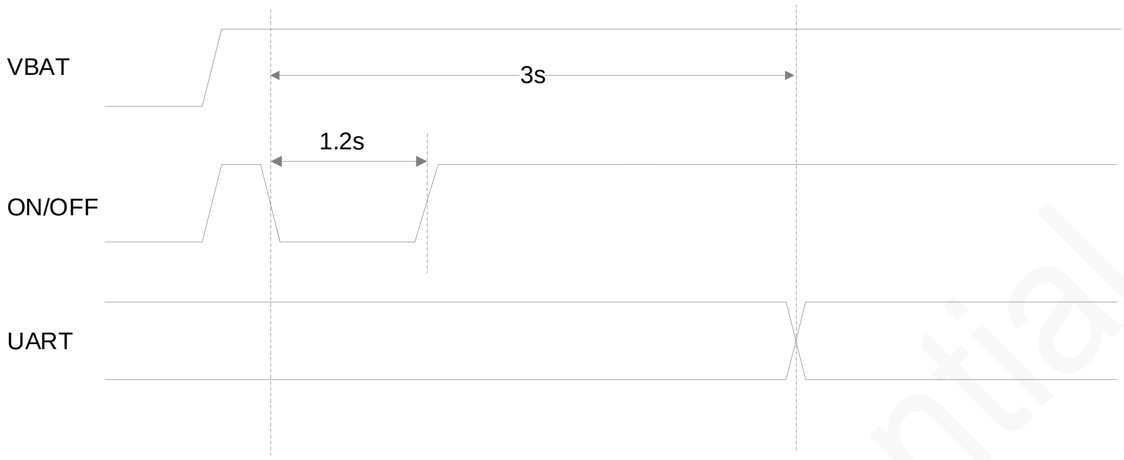
Power-On Procedure

While the module is off, pull the ON/OFF pin to ground for at least **1.2 seconds** and then release it, the module will start.

If the module uses a fixed baud rate, UART port prints an unsolicited message (\r\nMODEM:STARTUP\r\n), indicating that the module is initialized and the UART is ready to respond to

AT commands.

Figure 3-5 Power-on timing



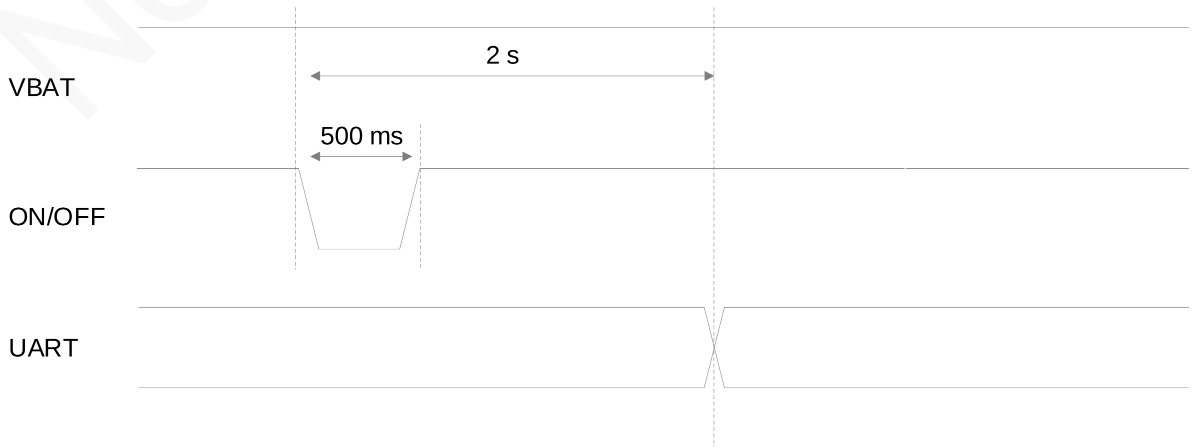
In program design, use the unsolicited message \r\nMODEM:STARTUP\r\n to determine whether the module is started or whether the module is reset properly after setting the baud rate.

Pay attention to the interface level exception between MCU and the module, especially the UART port, which might affect the power-on procedure of the module. E.g. in the turn-on procedure, the IO port of MCU has not completed the initialization and is in the output state, UTXD signal of the port (also the output pin) forced to pull low or high, the module may not be able to turn on normally.

Power-Off Procedure

While the module is on, pull the ON/OFF pin to ground for at least **500 ms** and then release, the module will try to detach to network and normally 2 seconds later it will shut down. Another approach to turn off the module is using AT commands. For details, please refer to *Neoway_N11_AT_Commands_Manual*.

Figure 3-6 Power-off procedure



Automatic Shutdown Triggered by Low Supply Voltage

The module keeps monitoring the voltage across VBAT. When the supply voltage is lower than 3.4 V, the module shuts down automatically.

Power-On/Off Control

Figure 3-7 shows a reference circuit for ON/OFF control with inverted control logic.

Figure 3-7 Reference circuit for power-on/off control

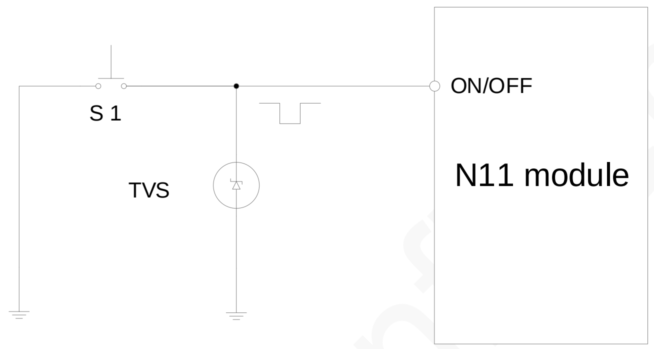
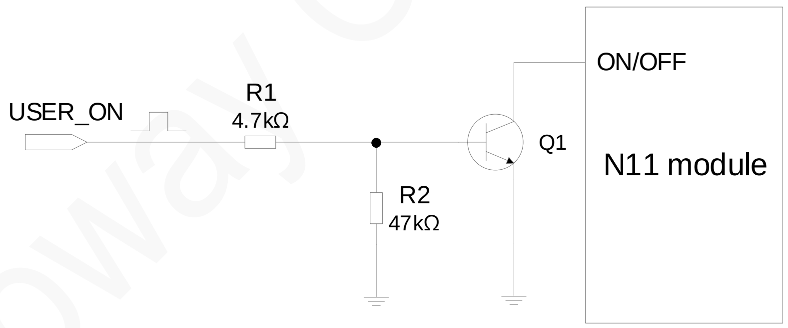


Figure 3-8 Reference circuit for power-on/off controlled by high level



In Figure 3-8, the level at ON/OFF is shifted, and the module powers on when USER_ON is at a high level.

R1 and R2 can be adjusted according to the driving capability of the USER_ON pin.

Use a common NPN transistor, e.g. MMBT3904; or a digital NPN transistor embedded with a serial resistor, e.g. DTC123. If a digital transistor is used, delete R1 and R2.

- Level abnormalities at interfaces connected to the external MCU, especially the UART port, might affect the power-on procedure of the module. For example, when a module is turned on, the IO ports of the MCU are still in output status because they have not been initialized completely. The module might fail to start if the UTXD signal (output pin) is forced to pull up or down.
- The better way to rescue the module from abnormal condition is to apply a power OFF-ON procedure, rather than using the ON/OFF control signal. In fact, the ON/OFF signal is software-dependent.

3.2 UART

Table 3-2 UART

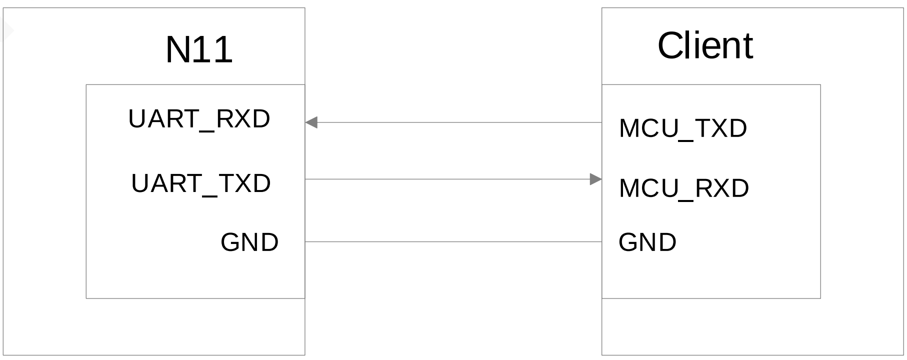
Pin	Signal	I/O	Description	Remarks
12	UART_TXD	DO	UART data transmit	N11: used for AT command issuing, firmware download, and calibration & final test N11 V2: used for AT command issuing
11	UART_RXD	DI	UART data receive	
13	DEBUG_TXD	DO		N11: used to capture log; can be configured as AT port by software N11 V2: used for download, and calibration & final test
14	DEBUG_RXD	DI		

Note the UART differences between N11 and N11 V2 when you are designing your products.

The UART of N11 works at a **2.8 V** CMOS logic level. The voltages for input high level should **not** exceed 3.1 V. The factory setting of UART is automatic adaption. UART supports baud rates of 9600, 14400, 19200, 38400, 57600, 115200 bit/s, and the default rate is **115200 bit/s**.

Figure 3-9 shows the signal connection between the module (DCE) and the terminal (DTE).

Figure 3-9 Signal connection between DCE and DTE



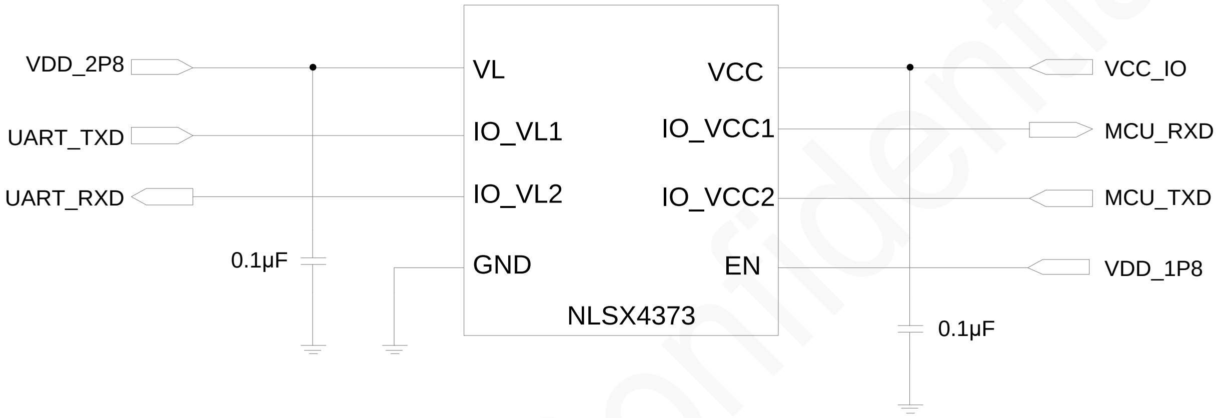
Schematic Design Guidelines

- Note the match of signals.
- If the UART does not match the logic voltage of the MCU, add an external level shifting circuit.

Three types of level shifting circuits are recommended based on the logic level quality. The first one is preferred and the other two are cost-effective simple circuits. Note their application scenarios.

Level shift chip is recommended if the level of MCU is higher than 3.3 V or the baud rate is higher than 1 MHz. Figure 3-10 shows the reference design.

Figure 3-10 Level shifting circuit 1



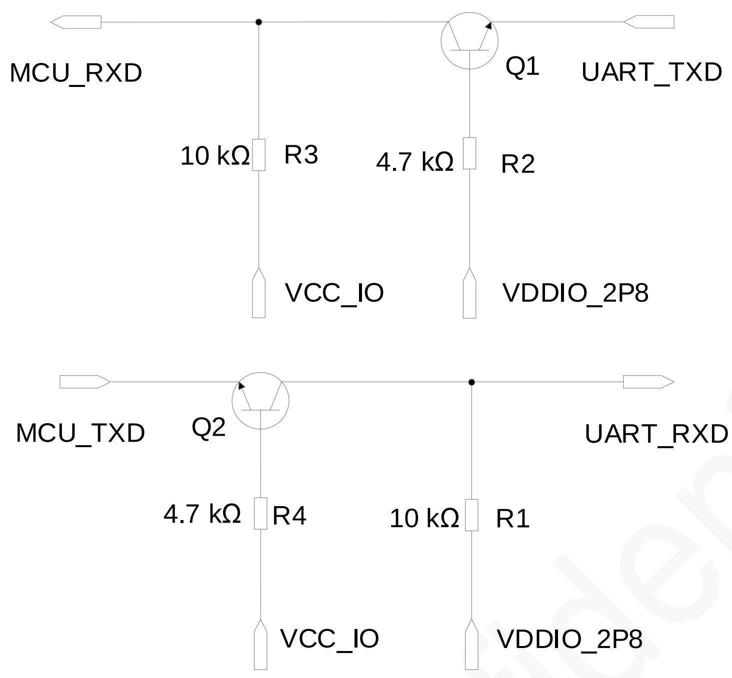
NLSX4373 is a dual-supply level shifter, the rate of which is up to 20 Mb/s.

- VL is the reference voltage of IO_VL1 and IO_VL2, ranging from 1.5 V to 5.5 V.
- VCC is the reference voltage of IO_VCC1 and IO_VCC2, ranging from 1.5 V to 5.5 V.
- EN is the enable pin, which works at a voltage of greater than VL-0.2V.

  In the above circuit, the EN pin is connected to VDD_1P8 and the level shifter is always working.

If the low level at MCU_UART (V_{IL}) is lower than 200 mV, use the level shifting circuit in Figure 3-11.

Figure 3-11 Level shifting circuit 1



Components:

- R2/R4: 2 kΩ-10 kΩ.

  The greater the UART baud rate is, the lower the R2/R4 value is.

- R1/R3: 4.7 kΩ-10 kΩ.

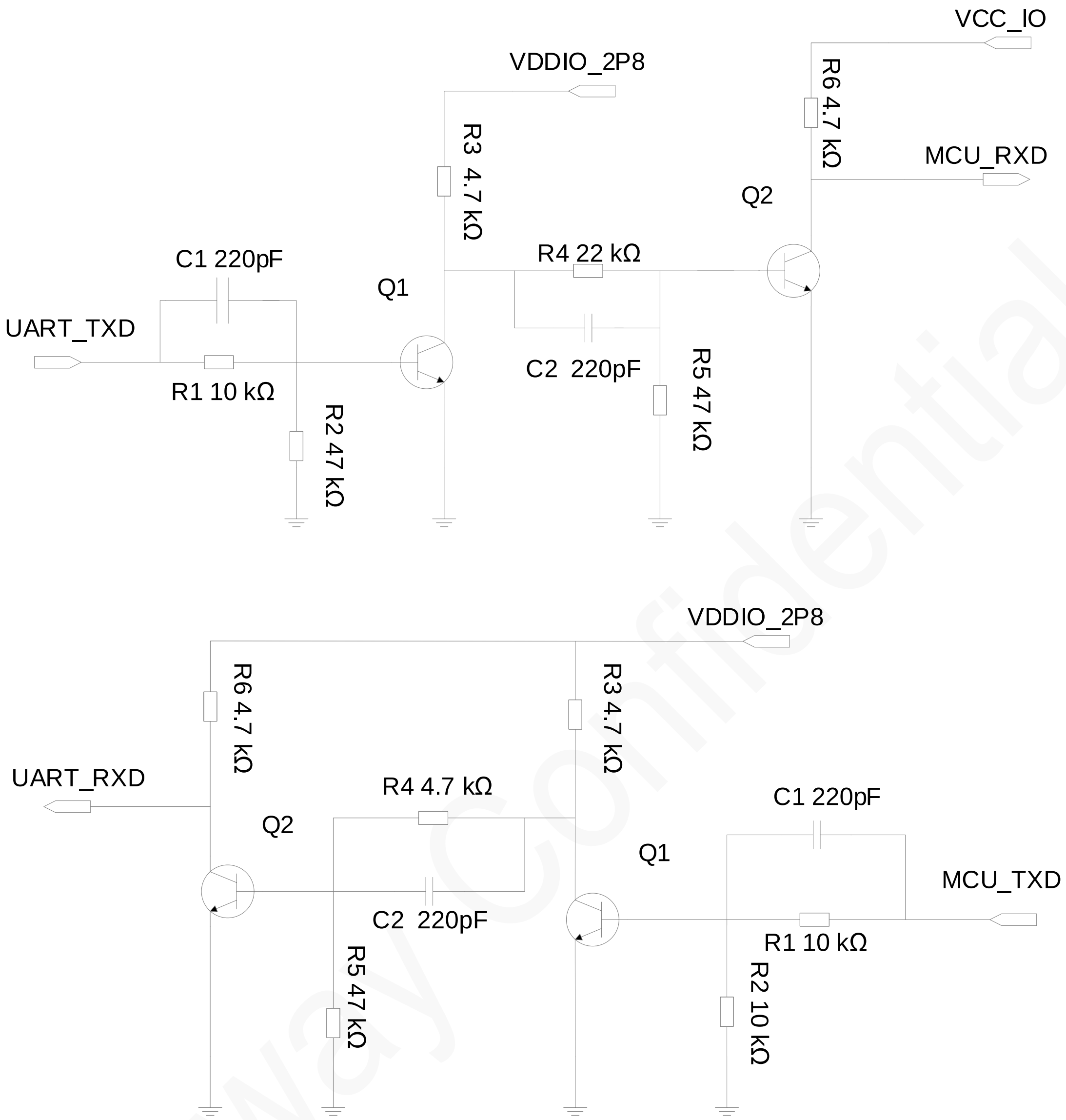
  The greater the UART baud rate is, the higher the R1/R3 value is.

- Q1/Q2: MMBT3904 or MMBT2222

  A high-speed transistor is better.

If the low level at MCU_UART (V_{IL}) is greater than 200mV, use the level shifting circuit in Figure 3-12. Otherwise, a low level across UART might be higher than required, resulting in failure to identify signals.

Figure 3-12 Recommended level shifting circuit 2



Q1, Q2: MMBT3904 or MMBT2222. A high-speed transistor is better.

MCU_TXD and MCU_RXD are respectively the TX and RX ports of the MCU while UART_TXD and UART_RXD are respectively the TX and RX ports of the module.

VCC_IO indicates the voltage at the UART of the MCU while VDDIO_2P8 indicates the voltage at the UART of the module.

3.3 DTR and RING

Table 3-3 DTR and RING pins

Pin	Signal	I/O	Function	Remarks
16	DTR	DI	Signal for controlling sleep mode	Leave this pin floating if it is not used
18	RING	DO	Ring output	Leave this pin floating if it is not used

3.3.2 DTR Pin

DTR is a pin to control the sleep mode of N11 and used with AT commands. For details, see *Neoway_N11_AT_Command_Manual*. In sleep mode, the module can respond to the incoming calls, SMS, and GPRS data.

Figure 3-13 shows the process of entering sleep mode.

Figure 3-13 Process of entering sleep mode

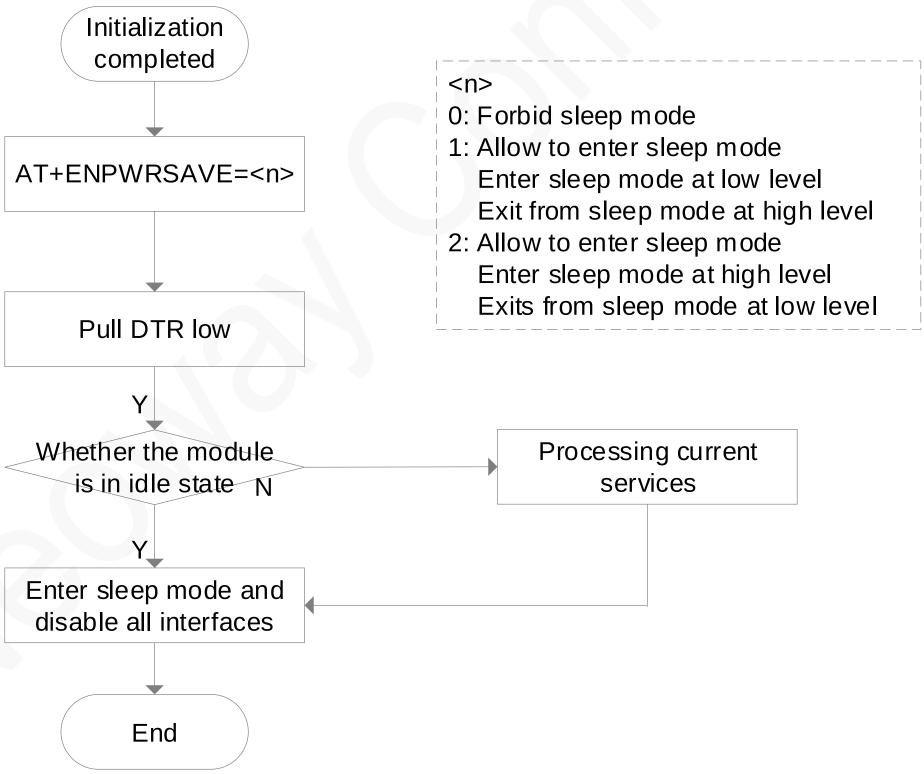


Figure 3-14 Incoming call service process

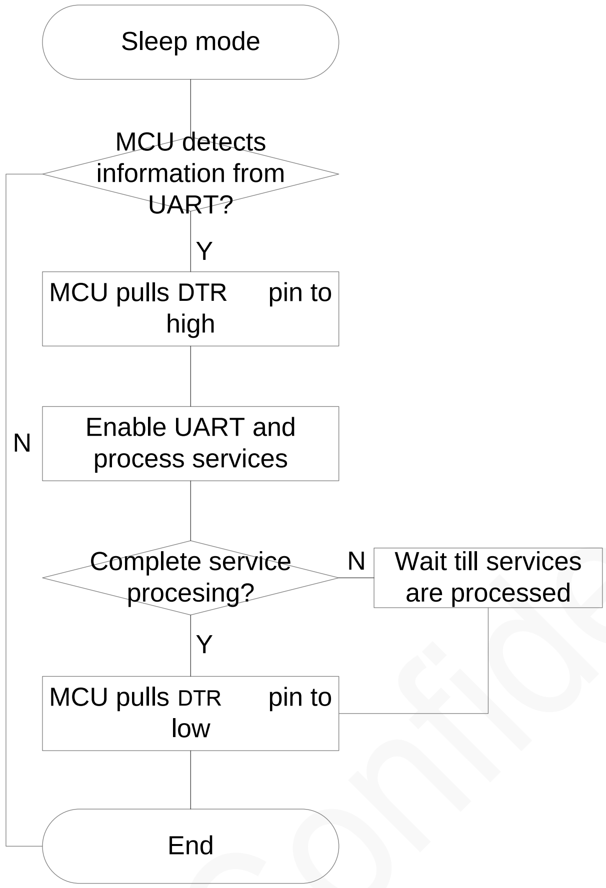


Figure 3-15 Outgoing call service process

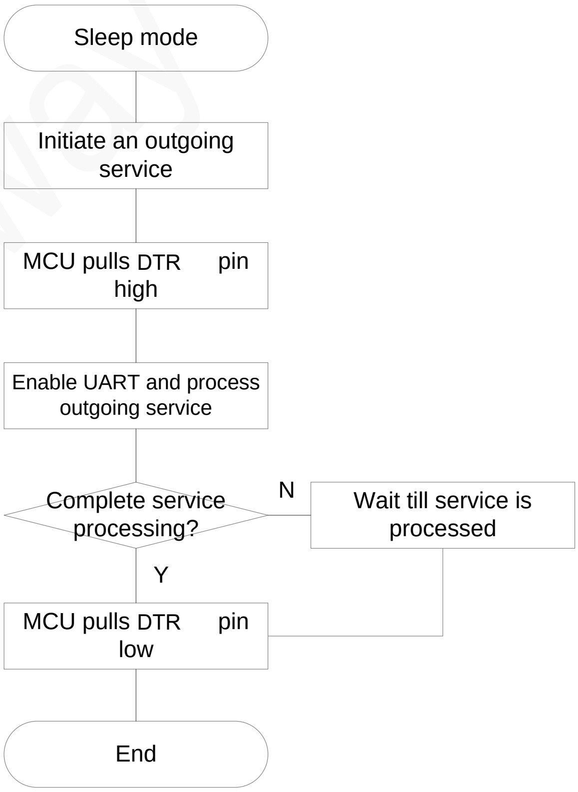
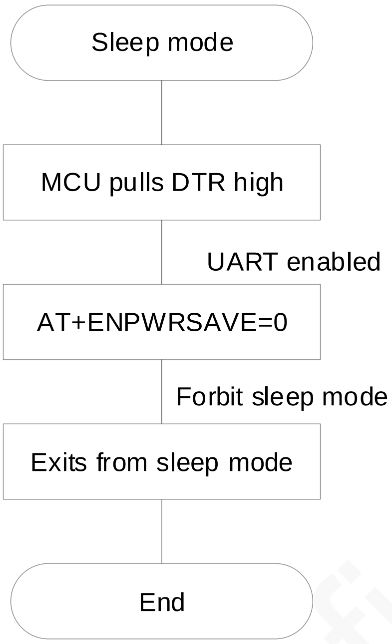


Figure 3-16 shows the process of exiting from sleep mode.

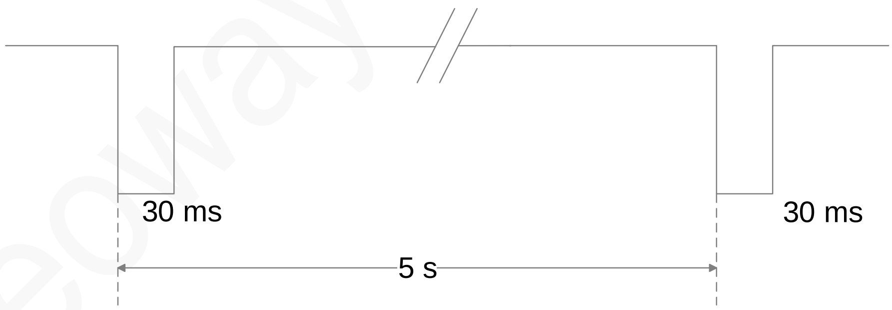
Figure 3-16 Process of exiting from sleep mode



3.3.3 RING Signal

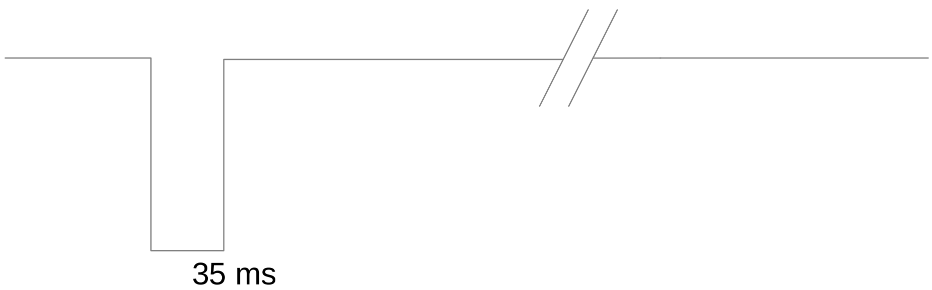
- Call: Once a voice call is coming, UART outputs "RING" character strings and meanwhile the RING pin outputs 30 ms negative pulses at 5s period. After the call is answered, the high level restores.

Figure 3-17 RING indicator for incoming call



- SMS: Upon receipt of SMS, the module outputs a 35 ms negative pulse.

Figure 3-18 RING indicator for SMS



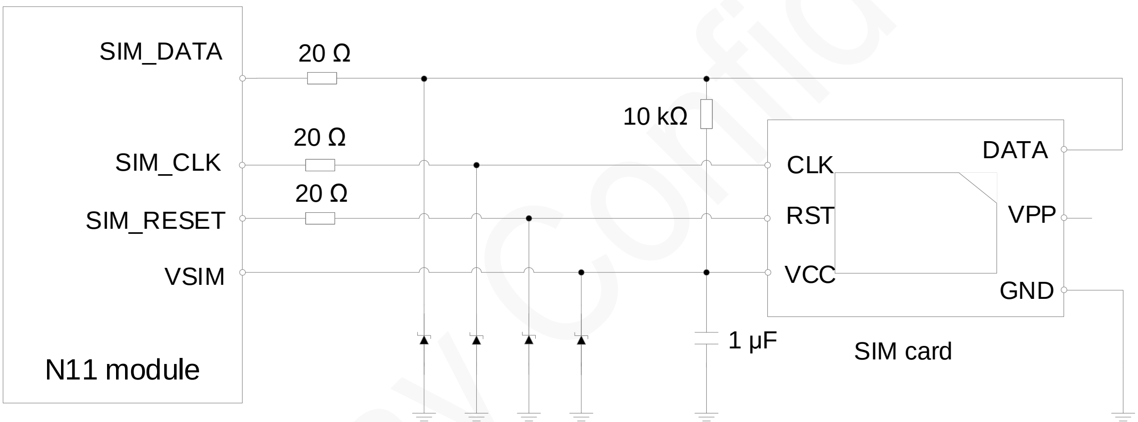
3.4 SIM Card

Table 3-4 SIM card interfaces

Pin	Signal	I/O	Function Description	Remarks
6	SIM_DATA	DI/O	SIM card data input/output	Self-adaption to 1.8V/3.0V
7	SIM_CLK	DO	SIM card clock	
8	SIM_RESET	DO	SIM card reset	
9	VSIM	P	SIM card power supply output	

N11 provides one USIM card interface that is compatible with 1.8 V/3.0 V USIM cards. Figure 3-19 shows the connection of the SIM card interface.

Figure 3-19 Reference design of SIM card interface



Schematic Design Guidelines

- VSIM is the pin to supply power for SIM card and its maximum load is 30 mA. Do not use it for any other purpose.
- Connect SIM_DATA to VSIM through an external 10 kΩ pull-up resistor since the SIM_DATA pin is not pulled up internally.
- SIM_CLK is the clock signal pin, supporting a clock frequency of 3.25 MHz.
- Add ESD diodes (with a junction capacitance as low as possible) on the SIM signal lines in applications with a high requirement of ESD protection.
- Connect a resistor less than 20 Ω respectively to SIM_DATA, SIM_RST, and SIM_CLK in series to enhance the ESD performance.

PCB Design Guidelines

- SIM signals are like to be jammed by RF radiation, resulting in failure to detect the SIM card. Place SIM far away from RF circuits.
- Place SIM card close to the module and SIM traces should be as short as possible.
- Place ESD protection resistors and components close to the SIM card.
- Surround SIM traces with ground to enhance EMC.

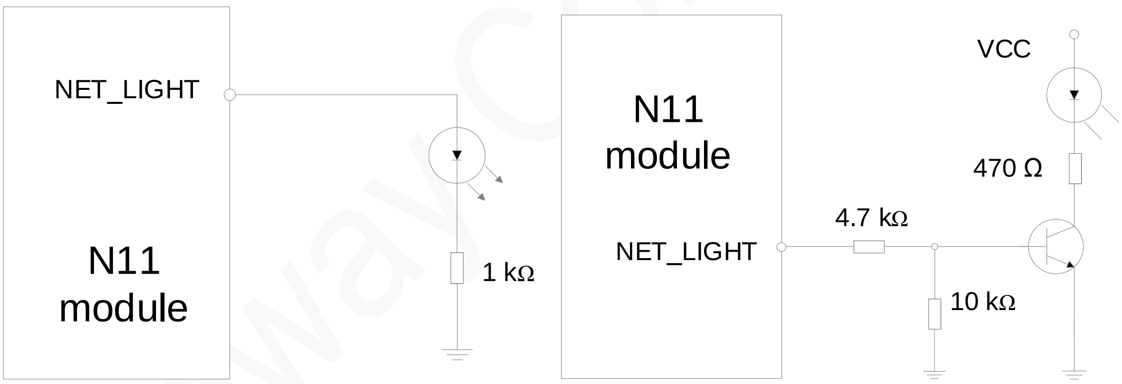
3.5 LIGHT

Table 3-5 LED indicator

Pin	Signal	I/O	Function	Remarks
17	NET_LIGHT	DO	Indicates network status	2.8 V output, max. 4 mA

The NET_LIGHT pin can output 4 mA and 2.8 V, therefore the LED can be directly connected to this pin with a resistor in series. For better luminance, drive the LED with a transistor.

Figure 3-20 LED indicator



When the module is running, NET_LIGHT outputs PMW waves of duty cycle varying with the status of the module and drives an LED indicator to blink at different frequencies.

For how to set the LED indicator, see *Neoway_N11_AT_Commands_Mannual*.

3.6 RF Interface

3.6.1 RF Design and PCB Layout

ANT_MAIN of N11 requires a characteristic impedance of 50 Ω, and the impedance of the traces should be controlled between the pins and antenna.

To ensure the RF performance, add an impedance matching circuit, such as L network, T network, or pi network in between. Pi network is recommended.

Figure 3-21 L network

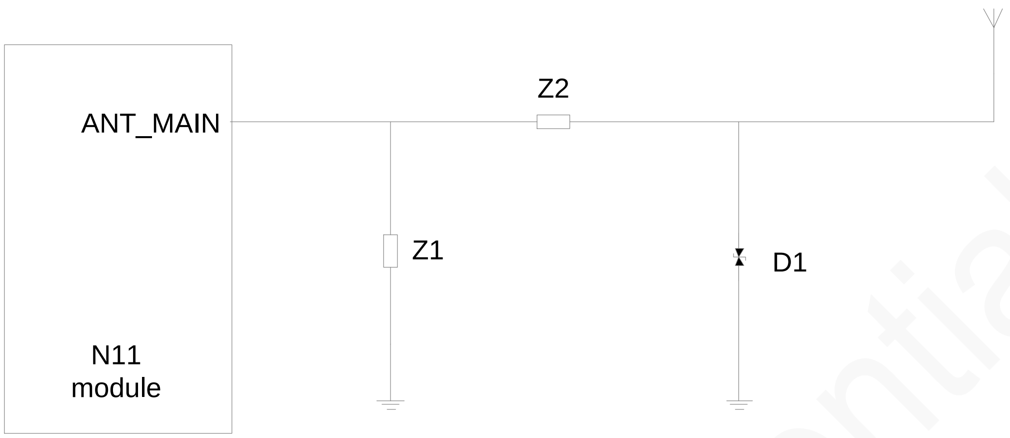


Figure 3-22 T network

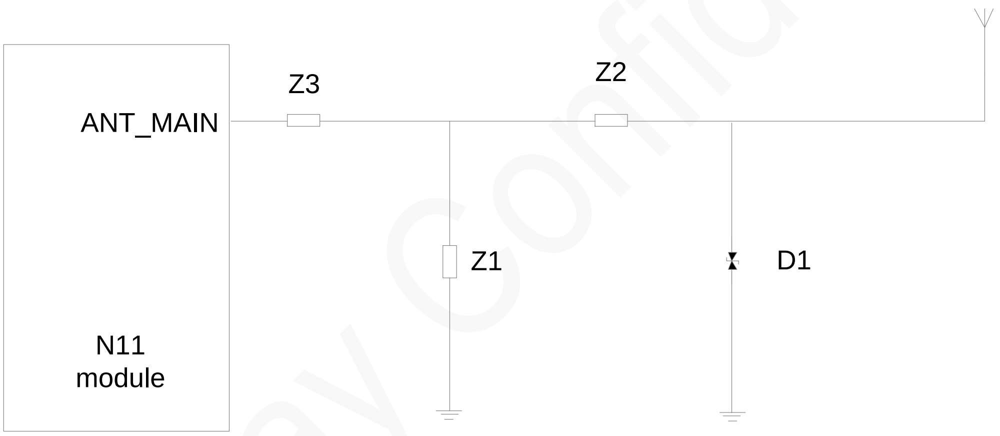
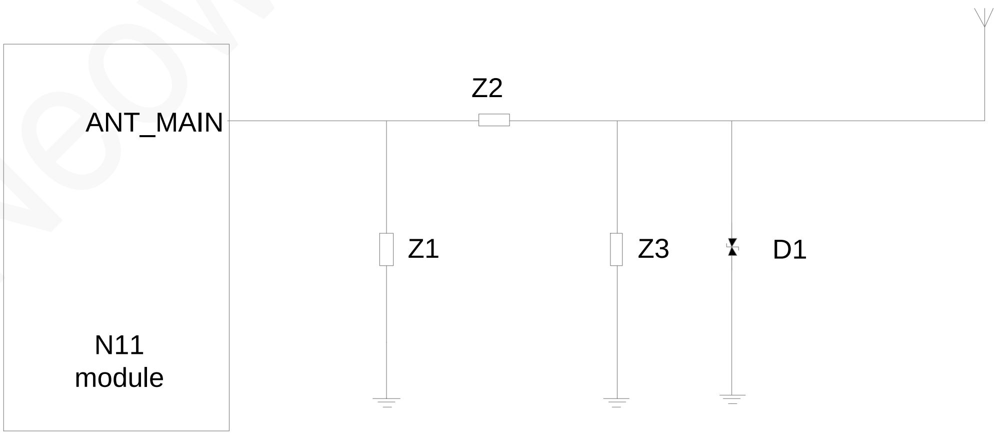


Figure 3-23 Pi network



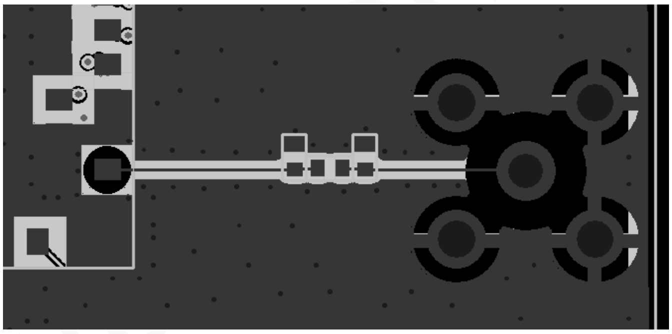
Schematic Design Guidelines

- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- Add an ESD protector. The protector can be a TVS diode with a junction capacitance of lower than 0.5 pF. Ensure that the reverse breakdown voltage of the TVS is greater than 10 V (above 15V is recommended).

PCB Layout Guidelines

- Lay copper foil around the RF connector. Dig as many via holes as possible on the copper to ensure the lowest grounding impedance.
- The traces between N11 and the antenna connector should be as short as possible. Control the trace impedance to 50 Ω.
- If customers adopt an SMA connector, a big RF solder pad might result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and second layers under the RF solder pad and keep complete reference ground plane on the third layer.
- Keep clearance (no ground) area at least on the layer the antenna solder pad resides and ensure that the neighboring reference ground is connected to the main ground properly.

Figure 3-24 RF layout reference



- On the PCB, keep the RF signals and RF components away from digital circuits, power supplies, transformers, power inductors, clock circuits, etc.

3.6.2 Antenna Assembling

The antenna used for the module should meet the mobile device requirements: The VSWR ranges from 1.1 to 1.5 and the input impedance is 50Ω. Antenna should be well matched to achieve the best performance in different application scenarios.

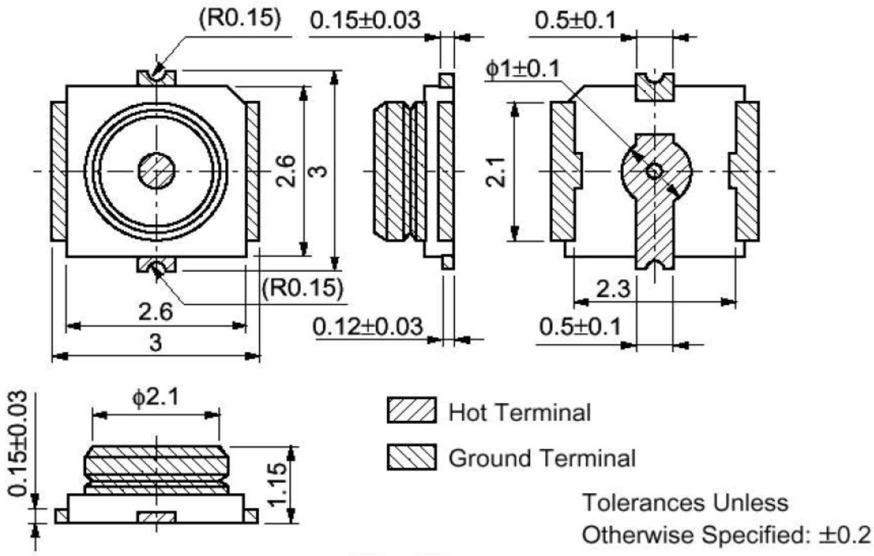
Antenna interfaces can be connected to a rubber ducky antenna, magnet antenna, or embedded Planar Inverted F Antenna (PIFA). Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.

The following methods are commonly used to assemble antenna:

- GSC RF connector

  MM9329-2700RA1 from Murata is recommended. Figure 3-25 shows its encapsulation specifications.

Figure 3-25 Specifications of MM9329-2700RA1



- Soldering

  RF wire can also be soldered to connect to the module. Ensure sufficient soldering in case of line loss that lowers RF performance.

Figure 3-26 shows the two types of connections.

Figure 3-26 RF connections

For more details, refer to the antenna manuals and other documents.

4 Electric Features and Reliability

4.1 Electric Feature

Table 4-1 Electric feature of the module

Parameter		Minimum Value	Typical Value	Maximum Value
VBAT	Vin	3.4 V	3.9 V	4.3 V
	Iin	/	/	2 A
VDDIO_2P8	Vout	/	2.8 V	/
	Iout	/	/	50 mA
DIO	Vout	2.3 V	2.8 V	3.1 V
	Iout	/	/	4 mA
	Vin	-0.3 V	0 V	0.6 V
	Iin	/	/	22.5 μA

If the voltage is too low, the module might fail to start. If the voltage is too high or there is a voltage burst during the startup, the module might be damaged permanently.

If LDO or DC-DC is used to supply power for the module, ensure that it output at least 2 A current.

4.2 Temperature

Table 4-2 Temperature Feature

Module Status	Minimum Value	Typical Value	Maximum Value
Working	-40 °C	25 °C	85 °C
Storage	-45 °C		90 °C

If the module works in temperature exceeding the thresholds, its RF performance (e.g. frequency deviation or phase deviation) might be worse but it can still work properly.

4.3 Current

Table 4-3 Current feature

Parameter	Testing Conditions		Testing Result (Average Current)
Testing voltage	3.9 V Agilent power supply		/
Idle mode	Set the instrument and power on the module.		11 mA
Off leakage current	Power on the module or use AT command to shut the module down.		170 μA
Average network searching current	Set the instrument. Start the module. Wait until the module registers the instrument.		50 mA
Sleep mode	On a live network, the module registers the network and then enters the sleep mode.		<2.5 mA
Sleep mode	Set the instrument properly (DRX=9)		1.1 mA
Voice service	Maximum power level in full rate mode	GSM850	194 mA
Voice service	Maximum power level in full rate mode	EGSM900	185 mA
Voice service	Maximum power level in full rate mode	DCS1800	135 mA
Voice service	Maximum power level in full rate mode	PCS1900	126mA
GPRS class 12	4TX, 1RX (4Up/1Down)	GSM850	435 mA
GPRS class 12	4TX, 1RX (4Up/1Down)	EGSM900	397 mA
GPRS class 12	4TX, 1RX (4Up/1Down)	DCS1800	268 mA
GPRS class 12	4TX, 1RX (4Up/1Down)	PCS1900	242 mA
GPRS class 12	1TX, 4RX (1Up/4Down)	GSM850	184 mA
GPRS class 12	1TX, 4RX (1Up/4Down)	EGSM900	170 mA
GPRS class 12	1TX, 4RX (1Up/4Down)	DCS1800	122 mA
GPRS class 12	1TX, 4RX (1Up/4Down)	PCS1900	117 mA

The data in the above table are typical values obtained during tests in the lab. It might be a little bit different in manufacturing. Also, the test results might be various due to different settings or testing methods.

4.4 ESD Protection

Electronics need to pass severe ESD tests. The following table shows the ESD capability of key pins of our module. Add ESD protection to those pins in accordance with the application to ensure product quality when designing better products.

Humidity: 45%

Temperature: 25 °C

Table 4-4 ESD feature of the module

Testing Point	Contact Discharge	Air Discharge
VBAT	±8 kV	±15 kV
GND	±8 kV	±15 kV
ANT	±8 kV	±15 kV
Cover	±8 kV	±15 kV
UART_RXD/UART_TXD	±4 kV	±8 kV
Others	±4 kV	±8 kV

5 RF Features

5.1 Operating Band

Table 5-1 Operating band

Operating Band	Uplink	Downlink
GSM850	824~849 MHz	869~894 MHz
EGSM900	880~915 MHz	925~960 MHz
DCS1800	1710~1785 MHz	1805~1880 MHz
PCS1900	1850~1910 MHz	1930~1990 MHz

5.2 Transmitting Power and Receiving Sensitivity

5.2.1 Transmitting Power

Table 5-2 Transmitting power (GSM850&EGSM900)

PCL	Transmitting Power	Threshold Range
5	33 dBm	±2 dBm
6	31 dBm	±3 dBm
7	29 dBm	±3 dBm
8	27 dBm	±3 dBm
9	25 dBm	±3 dBm
10	23 dBm	±3 dBm
11	21 dBm	±3 dBm
12	19 dBm	±3 dBm
13	17 dBm	±3 dBm
14	15 dBm	±3 dBm
15	13 dBm	±5 dBm
16	11 dBm	±5 dBm

17	9 dBm	±5 dBm
18	7 dBm	±5 dBm
19	5 dBm	±5 dBm

Table 5-3 Transmitting power (DCS1800&PCS1900)

PCL	Transmitting Power	Threshold Range
0	30 dBm	±2 dBm
1	28 dBm	±3 dBm
2	26 dBm	±3 dBm
3	24 dBm	±3 dBm
4	22 dBm	±3 dBm
5	20 dBm	±3 dBm
6	18 dBm	±3 dBm
7	16 dBm	±3 dBm
8	14 dBm	±3 dBm
9	12 dBm	±3 dBm
10	10 dBm	±4 dBm
11	8 dBm	±4 dBm
12	6 dBm	±4 dBm
13	4 dBm	±4 dBm
14	2 dBm	±5 dBm
15	0 dBm	±5 dBm

5.2.2 Receiving Sensitivity

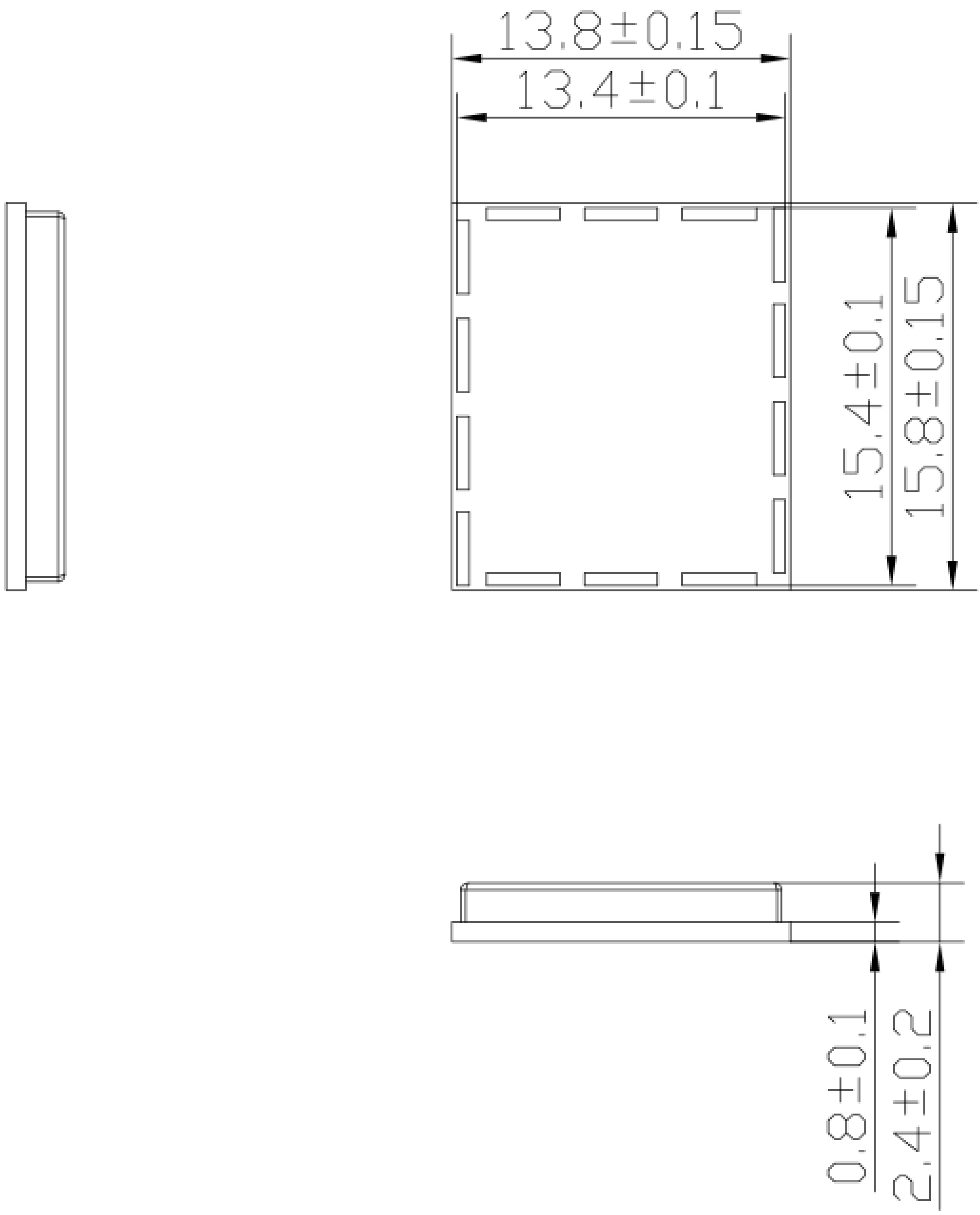
Band	Typical
GSM850&EGSM900	<-108 dBm
DCS1800&PCS1900	<-108 dBm

The data in the above tables is obtained by connecting the module to the RF test instrument (e.g. CMU200, CWM500, or Agilent8960) in lab tests. It is for reference only.

6 Mechanical Features

6.1 Dimensions

Figure 6-1 N11 dimensions (Unit: mm)



6.2 Label

The label is made of materials that are deformation-resistant, fade-resistant, and high-temperature-resistant and it can endure high temperatures up to 260 °C.

Figure 6-2 N11 label

Figure 6-3 N11 V2 label

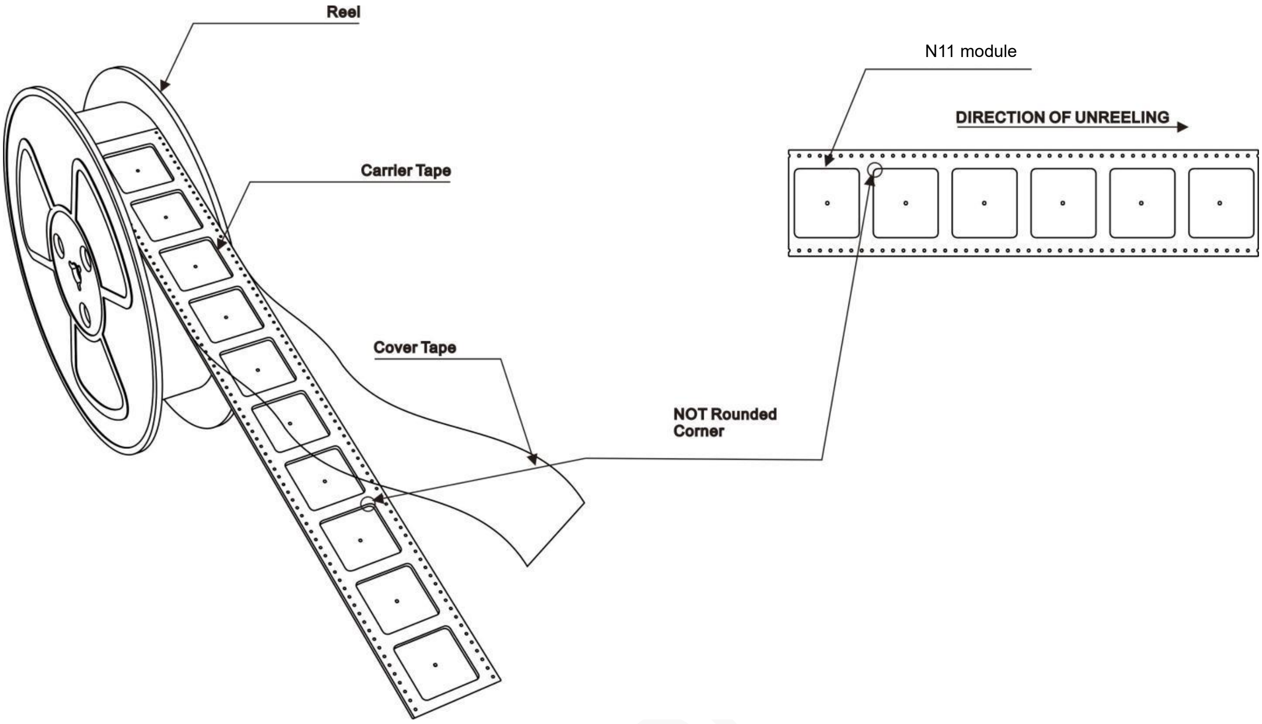
- The picture above is only for reference.
- The silk-screen printing must be clear. No blur is allowed.
- The material and surface finishing must comply with RoHS directives.

6.3 Package

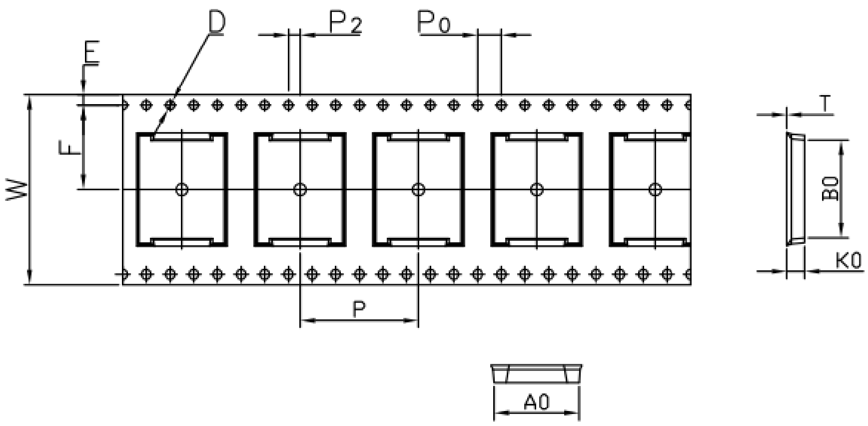
N11 modules are packed in sealed bags on delivery to guarantee a long shelf life. Follow the same package of the modules again in case of opened for any reason.

6.3.1 Tape & Reel Packaging

N11 in mass production is shipped in the following package.

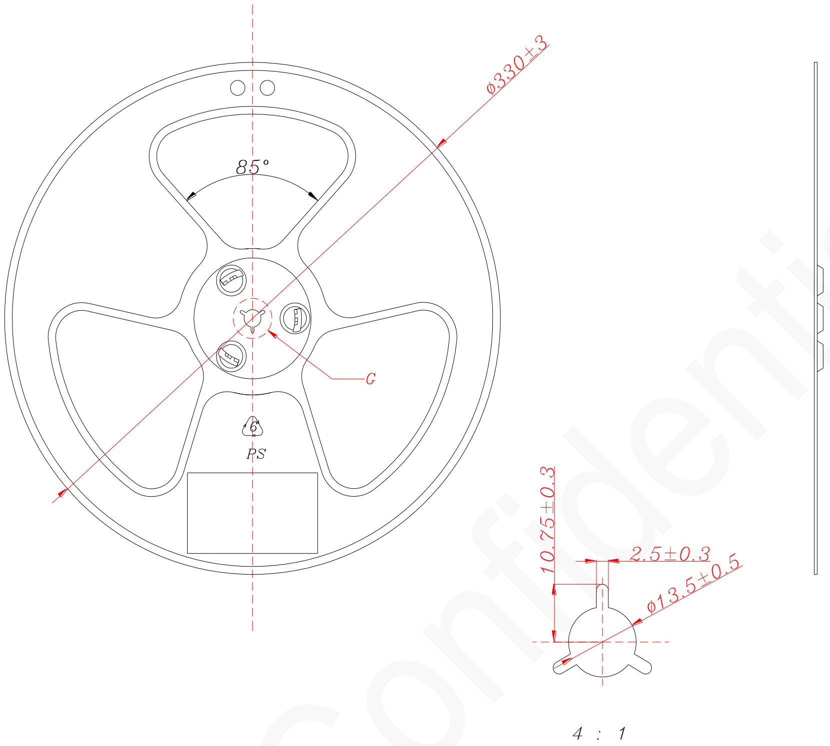


Tape



ITEM	W	A_0	B_0	K_0	K_1	P	F	E	D	D_1	P_0	P_2
DIM	$32.0^{+0.30}_{-0.10}$	$14.35^{+0.10}_{-0.10}$	$16.45^{+0.10}_{-0.10}$	$3.30^{+0.10}_{-0.10}$	$0.00^{+0.10}_{-0.10}$	$20.0^{+0.10}_{-0.10}$	$14.2^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$0.00^{+0.25}_{-0.00}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$

Reel



6.3.2 Humidity-Sensitive

N11 is a level 3 moisture-sensitive electronic elements, in compliance with IPC/JEDEC J-STD-020 standard.

If the module is exposed to air for more than 48 hours at conditions not worse than 30°C/60% RH, bake it at a temperature higher than 90°C for more than 12 hours before SMT. Or, if the indication card shows humidity greater than 20%, the baking procedure is also required. Do not bake modules with the package tray directly.

6.4 Storage

N11 should be stored in the following conditions:

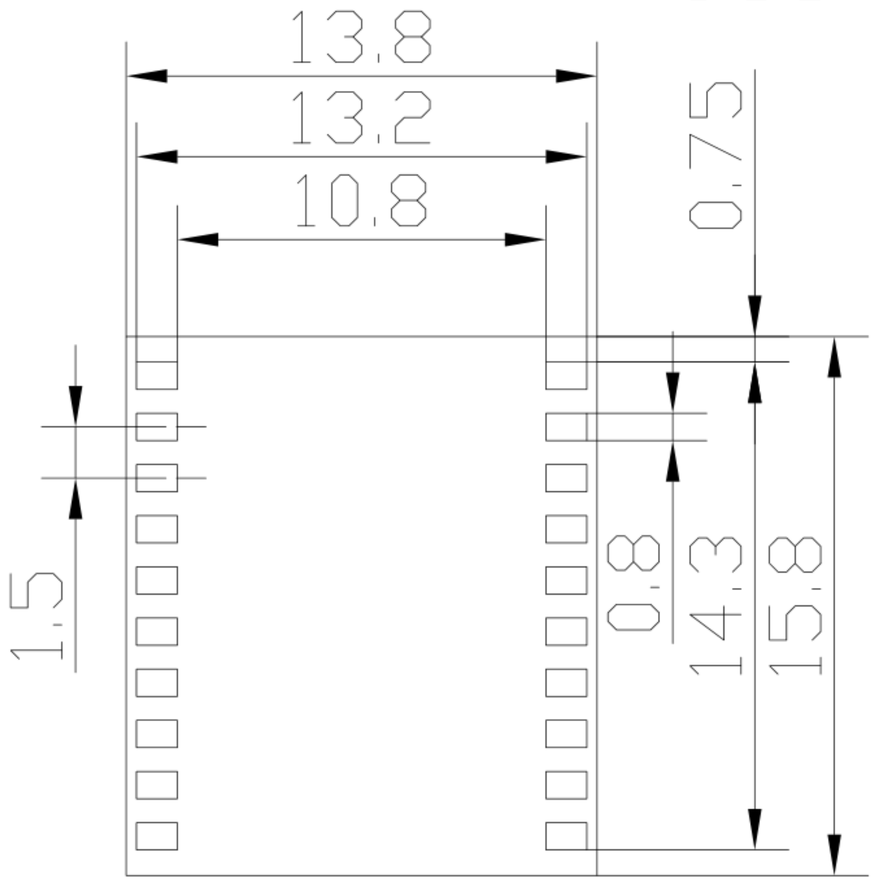
- Temperature: 20°C to 26°C
- Humility: 40% to 60%
- Period: 120 days

7 Mounting N11 onto Application Board

N11 is introduced in a 20-pin LGA package. This chapter describes N21 footprint, recommended PCB design and SMT information to guide users on how to mount the module onto the application PCB board.

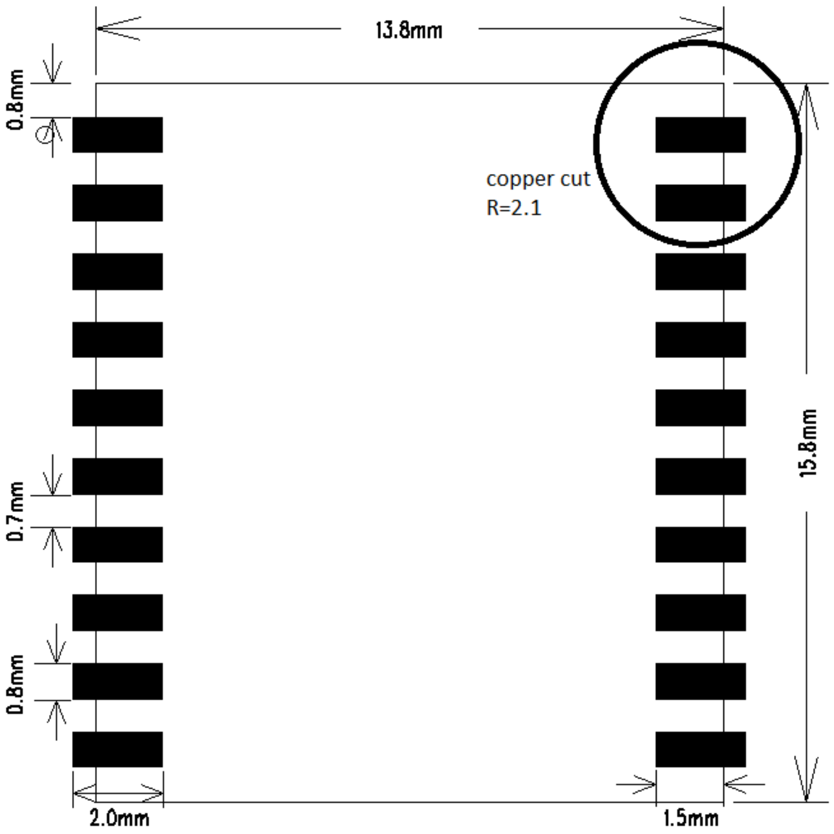
7.1 Bottom Dimensions

Figure 7-1 N11 bottom dimensions (Unit: mm)



7.2 Application Footprint

Figure 7-2 Recommended PCB footprint (Unit: mm)



7.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

7.4 Solder Paste

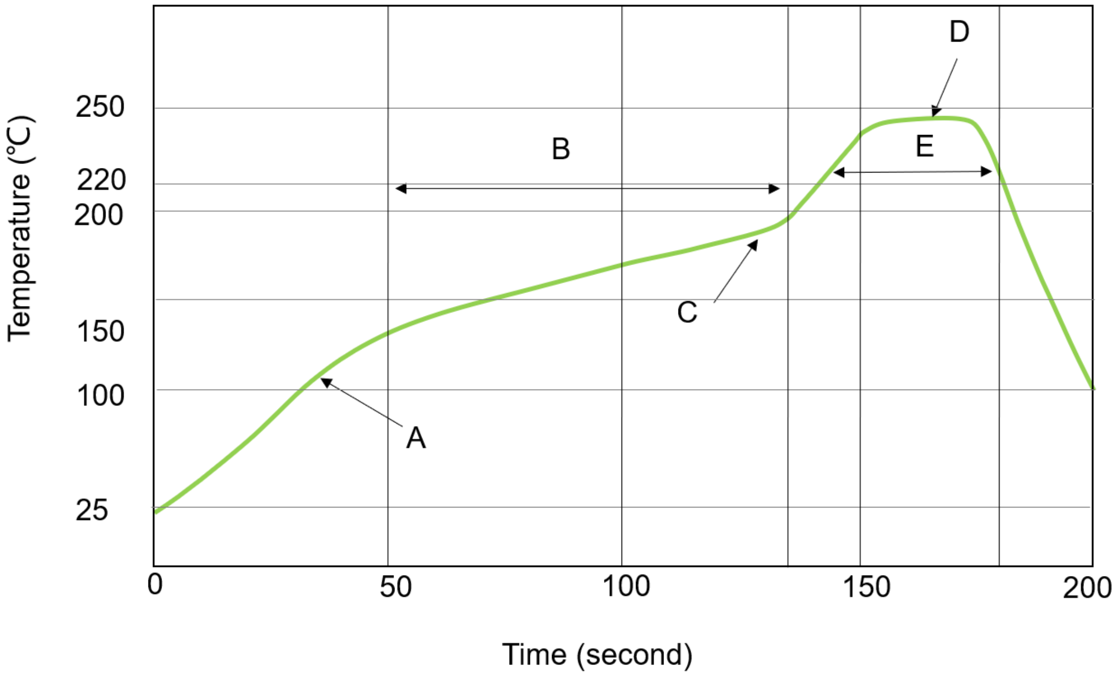
Do not use the kind of solder paste different from our module technique.

- The melting temperature of solder paste with lead is 35 °C lower than that of solder paste without lead. It is easy to cause voiding for LCC inside the module after the second reflow soldering.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220 °C for more than 45 seconds and the peak temperature reaches 240 °C.

7.5 SMT Profile

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 7-3 SMT furnace temperature curve



Technical parameters:

- Ramp up rate: 1 to 4 °C/sec
- Ramp down rate: -3 to -1 °C/sec
- Soaking zone: 150-180 °C, Time: 60-100 s
- Reflow zone: >220 °C, Time: 40-90 s
- Peak temperature: 235-245 °C

Neoway will not provide a warranty for heat-responsive element abnormalities caused by improper temperature control.

For information about cautions in N11 storage and mounting, refer to *Neoway Module Reflow Manufacturing Recommendations*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 245°C (depending on the type of the solder paste), and heat the module till the solder paste is melt.

Then remove the module using tweezers. Do not shake the module in high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

8 Safety Recommendations

Ensure that this product is used in compliance with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or workplace:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, etc.
- Do not use this product in environments such as hospitals or airplanes where it might interfere with other electronic equipment.

Please follow the requirements below in application design:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Please design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Please connect the product to a stable power supply and route traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.

  Do not remove the USIM card in idle mode if the module does not support hot-swapping.

A Abbreviations

Abbreviation	Full English
ADC	Analog-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AMR	Acknowledged multi-rate (speech coder)
CSD	Circuit Switched Data
CPU	Central Processing Unit
DAI	Digital Audio interface
DAC	Digital-to-Analog Converter
DCE	Data Communication Equipment
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
DTMF	Dual Tone Multi-Frequency
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electronic Static Discharge
ETS	European Telecommunication Standard
FDMA	Frequency Division Multiple Access
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
LCD	Liquid Crystal Display

LED	Light Emitting Diode
MS	Mobile Station
PCB	Printed Circuit Board
PCS	Personal Communication System
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
RMS	Root Mean Square
RTC	Real-Time Clock
SIM	Subscriber Identification Module
SMS	Short Message Service
SRAM	Static Random Access Memory
TA	Terminal adapter
TDMA	Time Division Multiple Access
UART	Universal asynchronous receiver-transmitter
VSWR	Voltage Standing Wave Ratio