CMOSTEK

CMT2380F64

Ultra-low Power Sub-1GHz Wireless Transceiver

MCU Features

- A 32-bit general-purpose micro-controller based on the Arm® Cortex®-M0 core，Single cycle hardware multiply instruction
- Up to 64 KByte on-chip Flash
  - supports encrypted storage and hardware ECC verification
  - Endurance more than 100,000 cycles, 10 years of data retention
- 8 KByte on-chip SRAM，supports hardware parity
- Programming method：
  - SWD online debugging interface
  - UART Bootloader
- 23 / 29 general IO (4 with SPI multiplexing in RF part)
- Low-power management：
  - Stop mode: RTC Runs, maximum 8 KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode (PD): supports 3 IO wakeup
- Clock：Up to 48 MHz
  - HSE ：4 MHz~20 MHz，external high-speed crystal
  - LSE ：32.768 KHz，external low-speed crystal
  - HSI：Internal high-speed RC OSC 8 MHz
  - LSI：Internal low-speed RC OSC 30 kHz
  - Built-in high-speed PLL
  - One channel clock output, which can be configured as configurable system clock, HSE, HSI or PLL post-divided output
- Reset
  - Supports power-on/power-down/external pin reset
  - Supports programmable low voltage detection and reset
  - Supports watchdog reset
- Communication Interface
  - 3xUART interface, with a maximum rate of 3 Mbps, of which 2 USART interfaces support 1xISO7816 , 1xIrDA, LIN,1 of which supports low power consumption (LPUART），the highest communication rate in this mode is 9600bps and stop mode can be awakened.
  - 2xSPI, the rate is up to 18 MHz, one of which supports multiplexing with I2S
  - 2xI2C, the rate is up to 1 MHz, master-slave mode is configurable, and dual-address response is supported in slave mode
- Analog interface
  - 1x12 bit high-speed ADC, 1 Msps, up to 6 external single-ended input channels
  - 1xOPAMP, built-in programmable gain amplifier up to 32 times
  - 1xCOMP, built-in 64-level adjustable comparison benchmark
  - 1x high speed 5-channel DMA control, source address and destination address can be configured

arbitrarily

- Timer/Counter
  - 1xRTC (real-time clock), supports leap year perpetual calendar, alarm event, periodic wake-up, supports internal and external clock calibration
  - 2x16 bit Advanced Timer Counters, supports input capture, complementary output, quadrature encoding input, 4 independent channels, of which 3 channels support 6 complementary PWM outputs
  - 1x16 bit General Timer, 4 independent channels, supports input capture/output comparison/PWM output
  - 1x16 bit Basic Timer
  - 1 x 16 bit Low-Power Timer
  - 1 x 24 bit SysTick
  - 1x 7 bit Window Watchdog (WWDG)
  - 1x12 bit Independent Watchdog (IWDG)
- Hardware Divider (HDIV) and Square Root(SQRT)
- Security features
- Flash storage encryption
- CRC16/32 calculation
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Supports clock failure monitoring, anti-dismantling monitoring
- 96-bit UID and 128-bit UCID

RF Features

- Working frequency： 127 - 1020 MHz
- Modulation style: (G)FSK, (G)MSK, OOK
- Data rate： 0.5 - 300 kbps
- Sensitivity： -121 dBm @ 434 MHz，FSK
- RX current： 8.5 mA @ 434 MHz，FSK
- TX current： 72 mA @ 20 dBm, 434 MHz
- Maximum configurable FIFO of 64 Byte

System Features

- Working voltage： 1.8 – 3.6 V
- Working temperature： -40 – 85 ℃
- Package: QFN40 5x5 / QFN 48 6x6

Overview

CMT2380F64 integrates a 32-bit ARM Cortex®-M0 core with a super low power consumption RF transceiver. It is a high efficiency super-low power MCU, applying for wireless application of (G) FSK、(G) MSK and OOK transceiver from 127 to 1020 MHz.CMT2380F64 is an ultra-low power, high performance, OOK (G) FSK RF transceiver suitable for a variety of 140 to 1020 MHz wireless applications. CMT2380F64 operates from 1.8 V to 3.6 V and supports up to +20 dBm TX power consumption and -121 dBm receiving sensitivity with the corresponding TX current and RX current of 72 mA and 8.5 mA.(MCU power consumption is not included). CMT2380F64 integrates a wealth of peripherals supports standard UART, I2C and SPI interface, with up to 23 general IO

（CMT2380F64-EQR40）/ 30 general IO（CMT2380F64-EQR48）, supports internal high speed /low speed low power consumption RC oscillator and 32.768 kHz external crystal oscillator, supports a variety of packet formats and encoding and decoding methods up to 64-byte Tx/Rx FIFO, supports featured rich RF GPIO, a variety of low power operation mode and fast startup mechanism, high precision RSSI, manual fast frequency hopping and 12 bit high speed ADCmulti-channel input,etc. CMT2380F64 has a small QFN package size of 5mmx5mm/6mmx6mm, which is ideal for small size and power consumption of Internet applications.

Application

- Auto metering
- Home security and building automation
- Wireless sensor nodes and industrial monitoring
- ISM band data communication

Table1. CMT2380F64 resources list

Memory		Analog peripheral		Digital peripheral							Package
ROM	RAM	ADC	PDR	RTC	WDT	Timer	UART	SPI	I2C	I2S	GPIO	
64 KB Flash	8 KB	12 bits x 6-ch 1Msps	√	1	1	5	2xUSART 1xLPUART	2	2	1	19+4	QFN40
64 KB Flash	8 KB	12 bits x 6-ch 1Msps	√	1	1	5	2xUSART 1xLPUART	2	2	1	25+4	QFN48

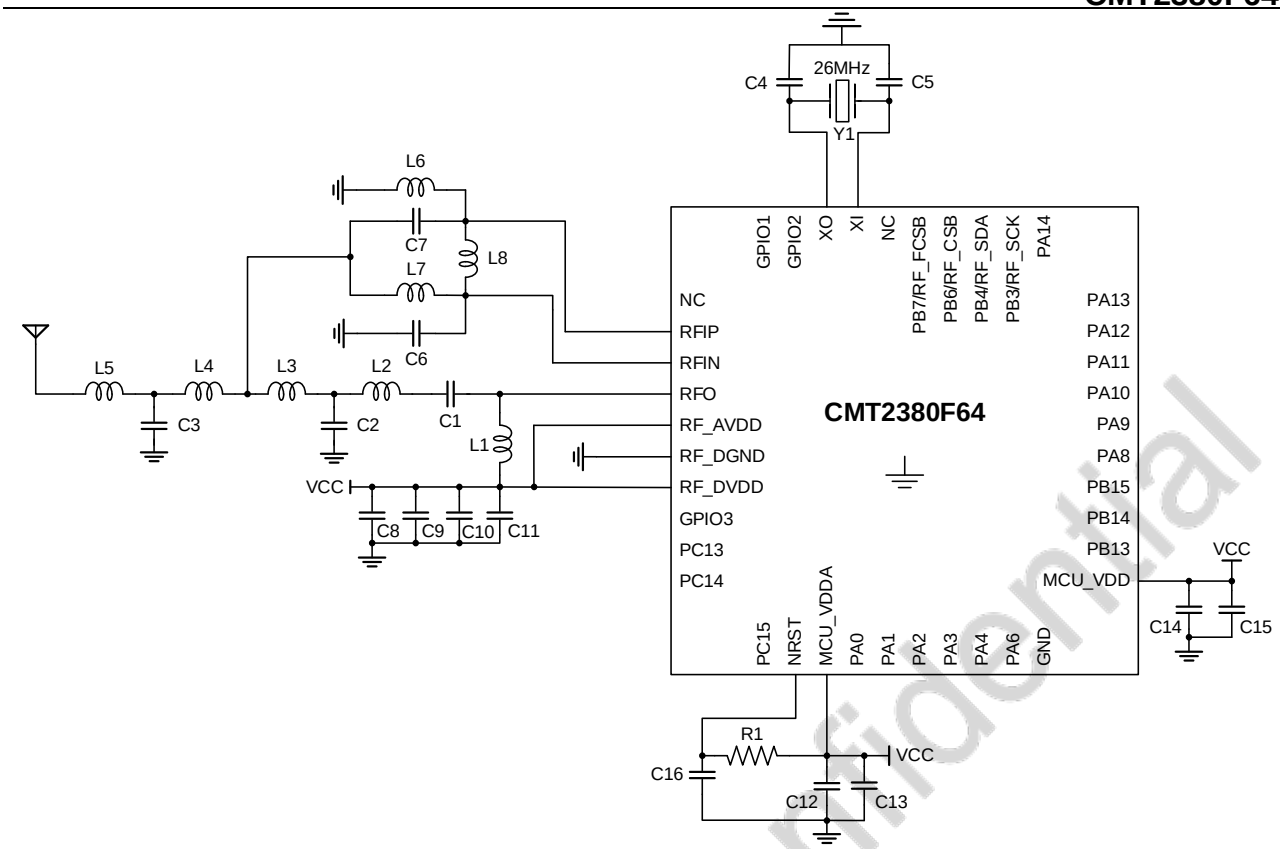

Figure1.CMT2380F64 (QFN 40 5x5) Typical application diagram (20 dBm power output)

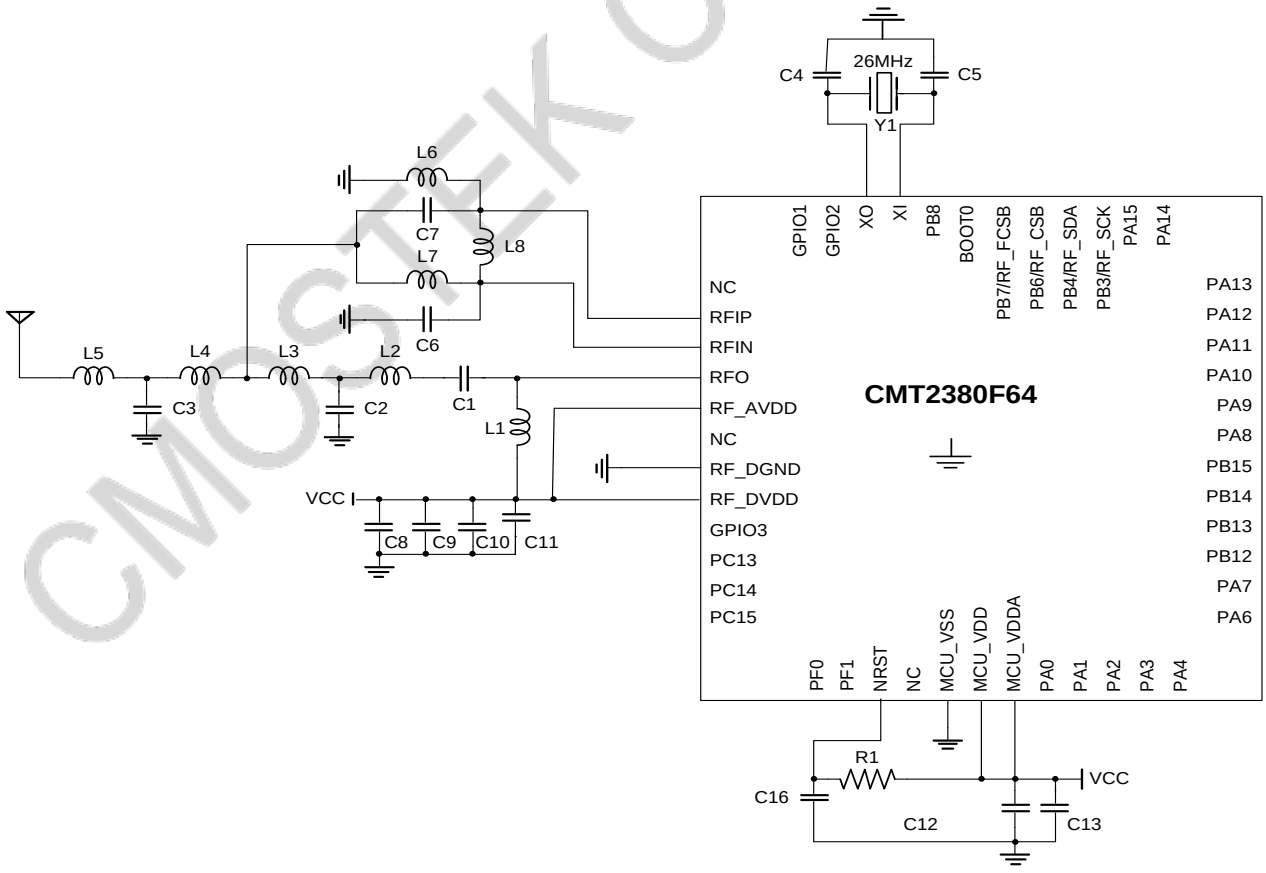

Figure 2.CMT2380F64（QFN 48 6x6）Typical application diagram (20 dBm power output)

No.	Description	Component value			Unit	Supplier
		434 MHz	868 MHz	915 MHz		
C1	±5%, 0402 NP0, 50 V	15	18	18	pF	-
C2	±5%, 0402 NP0, 50 V	3	3.6	3.6	pF	-
C3	±5%, 0402 NP0, 50 V	6.2	3.3	3.3	pF	-
C4	±5%, 0402 NP0, 50 V	24	24	24	pF	-
C5	±5%, 0402 NP0, 50 V	24	24	24	pF	-
C6	±5%, 0402 NP0, 50 V	4.7	2	1.8	pF	-
C7	±5%, 0402 NP0, 50 V	4.7	2	1.8	pF	-
C8	±20%, 0603 X7R, 25 V	4.7			uF	-
C9	±5%, 0402 NP0, 50 V	470			pF	-
C10	±20%, 0402 X7R, 25 V	0.1			uF	
C11	±20%, 0402 X7R, 25 V	0.1			uF	
C12	±20%, 0402 X7R, 25 V	0.1			uF	-
C13	±20%, 0603 X7R, 25 V	1			uF	-
C14	±20%, 0402 X7R, 25 V	0.1			uF	-
C15	±20%, 0603X7R, 25 V	1			uF	-
C16	±20%, 0402 X7R, 25 V	0.1			uF	
R1	±5%, 0603 Chip Resistor	10			kΩ	
L1	±10%, 0603 Multi-layer Chip Inductor	180	100	100	nH	Sunlord SDCL
L2	±10%, 0603 Multi-layer Chip Inductor	22	12	12	nH	Sunlord SDCL
L3	±10%, 0603 Multi-layer Chip Inductor	15pF	15	15	nH	Sunlord SDCL
L4	±10%, 0603 Multi-layer Chip Inductor	33	6.2	6.2	nH	Sunlord SDCL
L5	±10%, 0603 Multi-layer Chip Inductor	33	6.2	6.2	nH	Sunlord SDCL
L6	±10%, 0603 Multi-layer Chip Inductor	27	15	15	nH	Sunlord SDCL
L7	±10%, 0603 Multi-layer Chip Inductor	27	15	15	nH	Sunlord SDCL
L8	±10%, 0603 Multi-layer Chip Inductor	68	12	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	
U1	CMT2380F64, Ultra low power consumption Sub-1 GHz Wireless transceiver micro-controller	-			-	CMOSTEK

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1 Electrical Characteristic

VDD= 3.3 V，TOP= 25 °C，FRF = 433.92 MHz, sensitivity is measured by receiving a PN9 coded data and matching impedance to 50Ω under 0.1% BER standard.Unless otherwise stated, all results are tested on the CMT2380F17-EM evaluation board.

1.1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage	V_{DD-RF}		1.8		3.6	V
	V_{MCU}	CPU working rate 0-48 MHz	1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
RF power voltage slope	V_{RF-PSR}		1			mV/us
Voltage slope	$V_{MCU-PSR}$		10			mV/us
AHB clock frequency	f_{HCLK}		0		48	MHz
APB1 clock frequency	f_{PCLK1}		0		48	MHz
APB2 clock frequency	f_{PCLK2}		0		48	MHz

1.2 Absolute Maximum Rating

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	3.6	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Retention at least 30 s		255	℃
ESD Rating[2]		Human body mode(HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA
MCU-VDD maximum current to Ground				200	mA
MCU pin maximum sink current				16	mA

Notes：

[1]. Exceeding the Absolute Maximum Ratings may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. CMT2380F64 is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good protection.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep timer is off		300		nA
		Sleep mode, sleep timer is on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator is on		1.45		mA
RFS current	I_{RFS}	433 MHz		5.7		mA
		868 MHz		5.8		mA
		915 MHz		5.8		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
RX current (high performance)	I_{Rx-HP}	FSK, 433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		FSK, 915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
RX current (low power consumption)	I_{Rx-LP}	FSK, 433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		FSK, 915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA
TX current	I_{Tx}	FSK, 433 MHz, +20 dBm (Direct Tie)		72		mA
		FSK, 433 MHz, +20 dBm (RF switch)		77		mA
		FSK, 433 MHz, +13 dBm (Direct Tie)		23		mA
		FSK, 433 MHz, +10 dBm (Direct Tie)		18		mA
		FSK, 433 MHz, - 10 dBm (Direct Tie)		8		mA
		FSK, 868 MHz, +20 dBm (Direct Tie)		87		mA
		FSK, 868 MHz, +20 dBm (RF switch)		80		mA
		FSK, 868 MHz, +13 dBm (Direct Tie)		27		mA
		FSK, 868 MHz, +10 dBm (Direct Tie)		19		mA
		FSK, 868 MHz, - 10 dBm (Direct Tie)		8		mA
		FSK, 915 MHz, +20 dBm (Direct Tie)		70		mA
		FSK, 915 MHz, +20 dBm (RF switch)		75		mA
		FSK, 915 MHz, +13 dBm (Direct Tie)		28		mA
		FSK, 915 MHz, +10 dBm (Direct Tie)		19		mA
		FSK, 915 MHz, - 10 dBm (Direct Tie)		8		mA

Notes: The above power consumption is only RF working current, excluding the working current of the controller part.

1.4 RF Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR	OOK	0.5		40	kbps
		FSK and GFSK	0.5		300	kbps
Deviation	F_{DEV}	FSK and GFSK	2		200	kHz
Sensitivity @ 433 MHz	S_{433-HP}	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (Low power setting)		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (Low power setting)		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--103		dBm
Sensitivity @ 868 MHz	$S_{868\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (Low power setting)		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (Low power setting)		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity @ 915 MHz	$S_{915\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-117		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz (Low power setting)		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz (Low power setting)		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--99		dBm
Saturation Input Signal Level	P_{LVL}				20	dBm
Image Rejection Ratio	IMR	F_{RF}=433 MHz		35		dBc
		F_{RF}=868 MHz		33		dBc
		F_{RF}=915 MHz		33		dBc
RX Channel Bandwidth	BW	RX channel bandwidth	50		500	kHz
Co-channel Rejection Ratio	CCR	DR = 10 kbps, F_{DEV} = 10 kHz; Interfere with the same modulation		-7		dBc
Adjacent Channel Rejection Ratio	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100 kHz, 200 kHz Channel spacing, interfere with the same modulation		30		dBc
Alternate Channel Rejection Ratio	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100 kHz, 400 kHz Channel spacing, interfere with the same modulation		45		dBc
Blocking Rejection Ratio	BI	DR = 10 kbps, F_{DEV} = 10 kHz; ±1 MHz Deviation, continuous wave interference		70		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ± 2 MHz Deviation, continuous wave interference		72		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ±10 MHz Deviation, continuous wave interference		75		dBc
Input3rd Order Intercept Point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz; 1 MHz 和 2 MHz Deviation dual tone test, maximum system gain setting.		-25		dBm
RSSI Range	RSSI		-120		20	dBm
More Sensitivity (Typical Configuration)		433.92 MHz, DR = 1.2 kbps, F_{DEV} = 5 kHz		-122.9		dBm
		433.92 MHz, DR = 1.2 kbps, F_{DEV} = 10 kHz		-121.8		dBm
		433.92 MHz, DR = 1.2 kbps, F_{DEV} = 20 kHz		-119.5		dBm
		433.92 MHz, DR = 2.4 kbps, F_{DEV} = 5 kHz		-120.6		dBm
		433.92 MHz, DR = 2.4 kbps, F_{DEV} = 10 kHz		-120.3		dBm
		433.92 MHz, DR = 2.4 kbps, F_{DEV} = 20 kHz		-119.7		dBm

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		433.92 MHz, DR = 9.6 kbps, F_{DEV} = 9.6 kHz		-116.0		dBm
		433.92 MHz, DR = 9.6 kbps, F_{DEV} = 19.2 kHz		-116.1		dBm
		433.92 MHz, DR = 20 kbps, F_{DEV} = 10 kHz		-114.2		dBm
		433.92 MHz, DR = 20 kbps, F_{DEV} = 20 kHz		-113.0		dBm
		433.92 MHz, DR = 50 kbps, F_{DEV} = 25 kHz		-110.6		dBm
		433.92 MHz, DR = 50 kbps, F_{DEV} = 50 kHz		-109.0		dBm
		433.92 MHz, DR = 100 kbps, F_{DEV} = 50 kHz		-107.8		dBm
		433.92 MHz, DR = 200 kbps, F_{DEV} = 50 kHz		-103.5		dBm
		433.92 MHz, DR = 200 kbps, F_{DEV} = 100 kHz		-104.3		dBm
		433.92 MHz, DR = 300 kbps, F_{DEV} = 50 kHz		-98.0		dBm
		433.92 MHz, DR = 300 kbps, F_{DEV} = 150 kHz		-101.6		dBm

1.5 RF Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Specific peripheral materials are needed for different frequency bands	-20		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Output power variation	$P_{OUT-TOP}$	Temperature from -40 to +85℃		1		dB
Transmitting spurious emission		P_{OUT}= +13 dBm,433 MHz, F_{RF}<1 GHz			-54	dBm
		1 GHz to 12.75 GHz, with harmonic			-36	dBm
Harmonic output for F_{RF}= 433 MHz[1]	$H2_{433}$	2nd harmonic +20 dBm P_{OUT}		-46		dBm
	$H3_{433}$	3nd harmonic +20 dBm P_{OUT}		-50		dBm
Harmonic output for FRF= 868 MHz[1]	$H2_{868}$	2nd harmonic +20 dBm P_{OUT}		-43		dBm
	$H3_{868}$	3ndharmonic +20 dBm P_{OUT}		-52		dBm
Harmonic output for FRF= 915 MHz[1]	$H2_{915}$	2ndharmonic +20 dBm P_{OUT}		-48		dBm
	$H3_{915}$	3ndharmonic +20 dBm P_{OUT}		-53		dBm
Harmonic output for FRF= 433 MHz[1]	$H2_{433}$	2ndharmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{433}$	3ndharmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2ndharmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3ndharmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{915}$	2ndharmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{915}$	3ndharmonic +13 dBm P_{OUT}		-52		dBm

Notes:

[1]. The harmonic parameter values mainly depend on the quality of the hardware matching network. The above data is measured based on the CMT2380F17-EM module; testing results will be differently when it is done on the self-designed PCB.

1.6 Settling Time of RF Status Switching

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	T_{SLP-RX}	From Sleep to RX		1000		us
	T_{SLP-TX}	From Sleep toTX		1000		us
	T_{STB-RX}	From Standby to RX		350		us

Settling time	T_{STB-TX}	From Standby toTX		350		us
	T_{RFS-RX}	From RFS to RX		20		us
	T_{TFS-RX}	From TFS toTX		20		us
	T_{TX-RX}	From TX to RX （Ramp Down time needs 2 T_{symbol}）		2 T_{symbol} +350		us
	T_{RX-TX}	From RX to TX		350		us
Notes: [1]. Both of TSLP-RX and TSLP-TX are depend on the crystal oscillator startup time, which is mainly related to the crystal itself.						

1.7 RF Frequency Synthesizer

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Different matching network is required	760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Synthesizer frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise@ 433 MHz	PN_{433}	10 kHz frequency deviation		-94		dBc/Hz
		100 kHz frequency deviation		-99		dBc/Hz
		500 kHz frequency deviation		-118		dBc/Hz
		1 MHz frequency deviation		-127		dBc/Hz
		10 MHz frequency deviation		-134		dBc/Hz
Phase noise@ 868 MHz	PN_{868}	10 kHz frequency deviation		-92		dBc/Hz
		100 kHz frequency deviation		-95		dBc/Hz
		500 kHz frequency deviation		-114		dBc/Hz
		1 MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz frequency deviation		-89		dBc/Hz
		100 kHz frequency deviation		-92		dBc/Hz
		500 kHz frequency deviation		-111		dBc/Hz
		1 MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz

1.8 Crystal Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Equivalentresistance	Rm			60		Ω
Start-up time[3]	t_{XTAL}			400		us

Notes:

[1]. CMT2380F64 can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3 V and 0.7 V.

[2]. The value includes (1) initial error; (2) crystal load; (3)aging; and (4) change with temperature. The acceptable crystal frequency tolerance is limited by the receiver bandwidth and the RF frequency offset between the transmitter and the receiver.

[3]. The parameter is largely related to the crystal.

1.9 Controller Reset and Power Control Module Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Rising	V_{PVD}	PLS[3:0]=0	1.8	1.88	1.96	V
Falling		PLS[3:0]=0	1.7	1.78	1.86	
Rising		PLS[3:0]=1	2	2.08	2.16	
Falling		PLS[3:0]=1	1.9	1.98	2.06	
Rising		PLS[3:0]=2	2.2	2.28	2.36	
Falling		PLS[3:0]=2	2.1	2.18	2.26	
Rising		PLS[3:0]=3	2.4	2.48	2.56	
Falling		PLS[3:0]=3	2.3	2.38	2.46	
Rising		PLS[3:0]=4	2.6	2.68	2.76	
Falling		PLS[3:0]=4	2.5	2.58	2.66	
Rising		PLS[3:0]=5	2.8	2.88	2.96	
Falling		PLS[3:0]=5	2.7	2.78	2.86	
Rising		PLS[3:0]=6	3	3.08	3.16	
Falling		PLS[3:0]=6	2.9	2.98	3.06	
Rising		PLS[3:0]=7	3.2	3.28	3.36	
Falling		PLS[3:0]=7	3.1	3.18	3.26	
Rising		PLS[3:0]=8	3.4	3.48	3.56	
Falling		PLS[3:0]=8	3.3	3.38	3.46	
Rising		PLS[3:0]=9	3.6	3.68	3.76	
Falling		PLS[3:0]=9	3.5	3.58	3.66	
Rising		PLS[3:0]=10	3.8	3.88	3.96	
Falling		PLS[3:0]=10	3.7	3.78	3.86	
PVD delay	$V_{PVDhyst}$(2)	-	80	100	125	mV
VDD power up/down	V_{POR}	-	-	1.53	-	V

1.10 Controller Embedded Reference Voltage

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Embedded reference voltage	V_{REFINT}	-40℃<TA<+105℃	1.16	1.21	1.26	V
Sampling time of ADC when internal reference voltage read out	$T_{S\_vrefint}$(1)	PLS [2:0]=001 (rising edge)	-	10	-	μs
1. The minimum sampling time was obtained from multiple cycles in application.						

1.11 Controller Working Current Characteristic

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin turnover rate, program location in memory, and code executed, etc.

- **Maximum current consumption**

The micro-controller is in the following conditions：

- All I / O pins are in input mode and are connected to a static level VDD or VSS with no load.
- All peripherals are disabled, unless otherwise noted.
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 wait period for 0 to 18 MHz, 1 wait period for 18 to 36 MHz, 2 waiting period for over 36 MHz).
- The command pre-fetch function is turned on (notes: this parameter must be set before the clock and bus frequency distribution is set).
- When the peripherals are turned on：$f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$.

Maximum current consumption in operating mode and the data processing code is run from the internal flash memory

Parameter	Sign	Condition	f_{HCLK}	Typical Value (1)	Unit
Operating current in the operating mode	I_{DD}	External clock(2)，enable all the peripherals	48 MHz	8.4	mA
			24 MHz	5.0	
			8 MHz	2.8	
		External clock(2)，disable all the peripherals	48 MHz	5.0	
			24 MHz	3.3	
			8 MHz	2.3	
1. Guaranteed by design and comprehensive assessment, not tested in production. 2. External clock, PLL is enabled when the f_{HCLK} is 24 MHz or 48 MHz.					

Maximum current consumption in operating mode, and data processing code is run from the internal RAM

Parameter	Symbol	Condition	f_{HCLK}	Typ. (1)	Unit
		External clock(2)，enable all the peripherals	48 MHz	6.2	
			24 MHz	4.1	
			8 MHz	3.2	

Operating current in the operating mode	I_{DD}	External clock(2)，disable all the peripherals	48 MHz	4.4	mA
			24 MHz	3.2	
			8 MHz	2.6	
1. Guaranteed by design and comprehensive assessment, not tested in production. 2. External clock, PLL is enabled when the f_{HCLK} is 24 MHz or 48 MHz.					

Maximum current consumption in sleep mode, and the code runs in the internal flash memory

Parameter	Symbol	Condition	f_{HCLK}	Typ. (1)	Unit
Working current in sleep mode	I_{DD}	External clock(2)，enable all the peripherals	48 MHz	6.5	mA
			24 MHz	3.9	
			8 MHz	2.0	
		External clock(2)，disable all the peripherals	48 MHz	2.9	
			24 MHz	2.1	
			8 MHz	1.4	
1. According to the comprehensive assessment, V_{DDmax} and $f_{HCLKmax}$ enabling peripheral are the test condition. 2. External clock, PLL is enabled when the f_{HCLK} is 24 MHz or 48 MHz.					

Typical consumption in stop and sleep mode

Parameter	Symbol	Condition	Typ(1)	Max	Unit
			V_{DD}=3.3V	V_{DD}=3.3V	
SLEEP mode current		Kernel stopped, all peripherals including Cortex-M 0 core peripherals such as NVIC, system ticking clock (SysTick) still running	2.7	5	mA
STOP mode current		RTC is not running, SRAM, registers and all I/O states retain	1.5	2.5	uA
PD mode current		VDD power down mode, 3 WAKEUP IO and NRST can be awakened	0.5	1	uA
1. Typ/ Max value is tested under TA=25 ℃.					

- **Typical current consumption**

MCU is under the following conditions：

- All I / O pins are in input mode and are connected to a static level VDD or VSS with no load.
- All peripherals are disabled, unless otherwise noted.
- The access time of the flash memory is adjusted to the fHCLK frequency (0 wait period for 0 to 18 MHz, 1 wait period for 18 to 36 MHz, 2 waiting period for over 36 MHz).
- The command pre-fetch function is turned on (notes: this parameter must be set before the clock and bus frequency distribution is set).
- When the peripherals are turned on：$f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/3$.

Typical current consumption in operation mode, with data processing code running from an internal Flash

Parameter	Symbol	Condition	f_{HCLK}	Typ(1)		Unit
				Enable all the peripherals	Disable all the peripherals	
Supply current in operating mode	I_{DD}	External high speed clock (HSE,) using AHB prefrequency to reduce the frequency	48 MHz	8.2	4.8	mA
			24 MHz	5.0	3.3	
			8 MHz	2.7	2.1	
		Internal high speed RC oscillator (2) (HSI)，AHB pre-frequency to reduce the frequency	48 MHz	7.6	4.3	mA
			24 MHz	4.3	2.7	
			8 MHz	2.1	1.5	

1. Typical value is tested under TA=25℃, VDD=3.3V.
2. The internal high-speed clock is 8 MHz，and PLL is enabled when f_{HCLK}>8 MHz.

Typical current consumption in sleep mode, data processing code is run from internal Flash or RAM

Parameter	Symbol	Condition	f_{HCLK}	Typ(1)		Unit
				Enable all the peripherals	Disable all the peripherals	
Working current in sleep mode	I_{DD}	External high speed clock (HSE)，using AHB prefrequency to reduce the frequency	48 MHz	6.3	2.7	mA
			24 MHz	3.7	2.0	
			8 MHz	1.8	1.2	
		Internal high speed RC oscillator(2) (HSI)， AHB pre-frequency to reduce the frequency	48 MHz	5.7	2.1	mA
			24 MHz	3.1	1.4	
			8 MHz	1.2	0.6	

1. Typical value is tested under TA=25 ℃, VDD=3.3 V.
2. The internal high-speed clock is 8 MHz，and PLL is enabled when fHCLK>8 MHz.

1.12 External Clock Source Charateristic

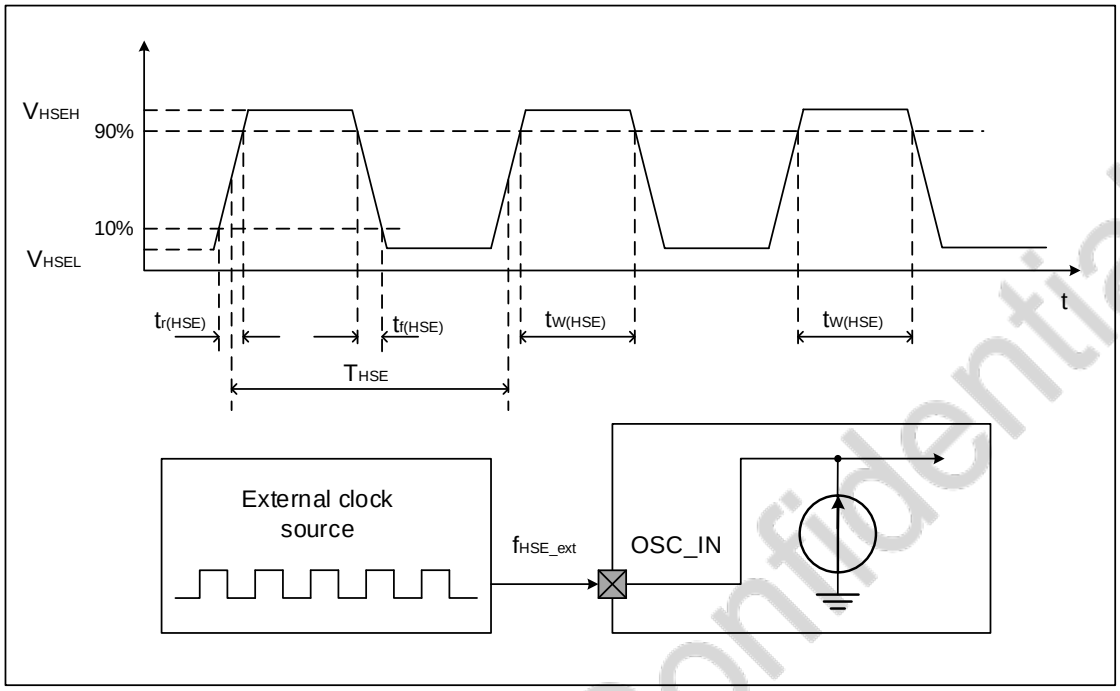
- High-speed external user clock generated from external oscillation sources

The characteristic parameters in the following table are measured under a high-speed external clock source and the ambient temperature and supply voltage meet the conditions in the following table.

High-speed external user clock features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency	-	4	8	20	MHz
V_{HSEH}	OSC_IN input pin at high-level voltage(1)		0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin at low-level voltage(1)		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSE)}$	OSC_IN high /low time(1)		16	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC_IN up/ down time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance (1)			5		pF

$DuCy_{(HSE)}$	Duty cycle(1)		45	-	55	%
I_L	OSC_IN input leakage current(1)	VSS≤VIN≤VDD	-	-	±1	μA
1. Guaranteed by design and comprehensive evaluation, not tested in production.						

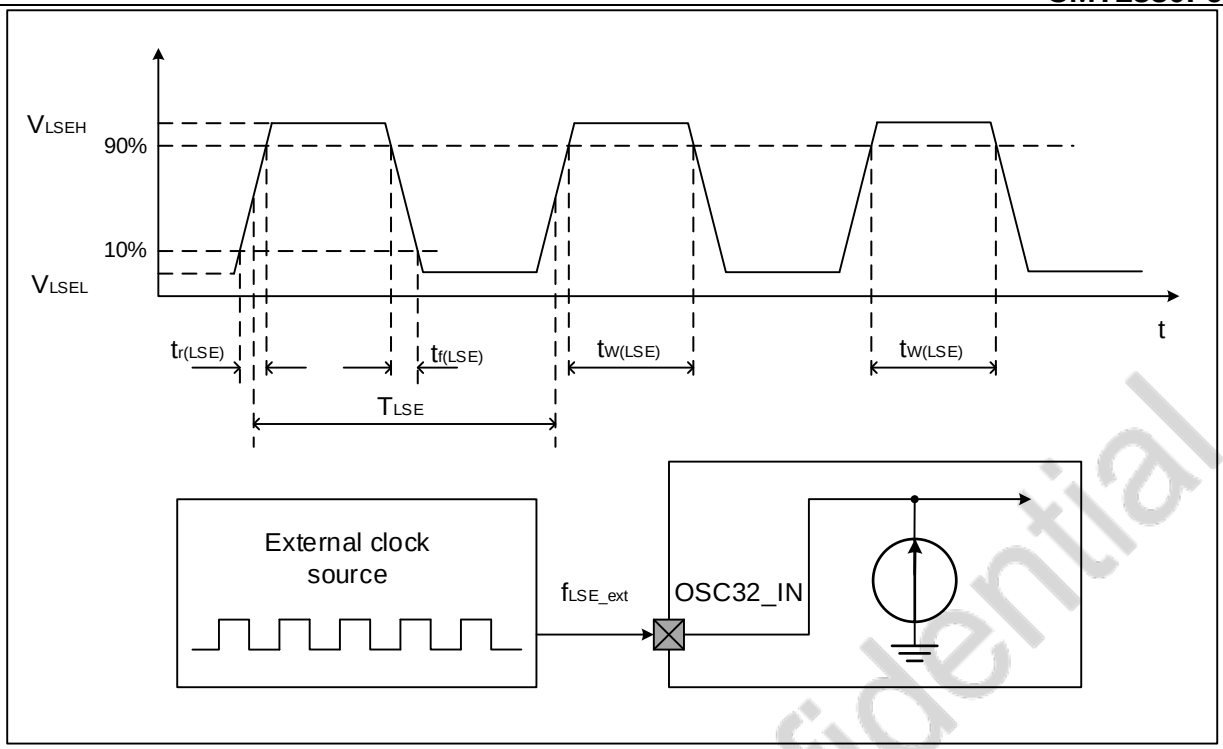


The AC timing diagram of the external high-speed clock source

- **Low-speed external user clock generated from external oscillation sources**

Low-speed external user clock features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin at high-level voltage(1)		0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin at low-level voltage(1)		V_{SS}	-	0.3 V_{DD}	
$tw_{(LSE)}$	OSC32_IN high /low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN up/ down time(1)		-	-	10	
$DuCy_{(LSE)}$	Duty cycle(1)		30	-	70	%
I_L	OSC32_IN input leakage current(1)	$V_{SS}≤V_{IN}≤V_{DD}$	-	-	±1	μA
1. Guaranteed by design and comprehensive assessment, not tested in production。						



The AC timing diagram of the external low-speed clock source

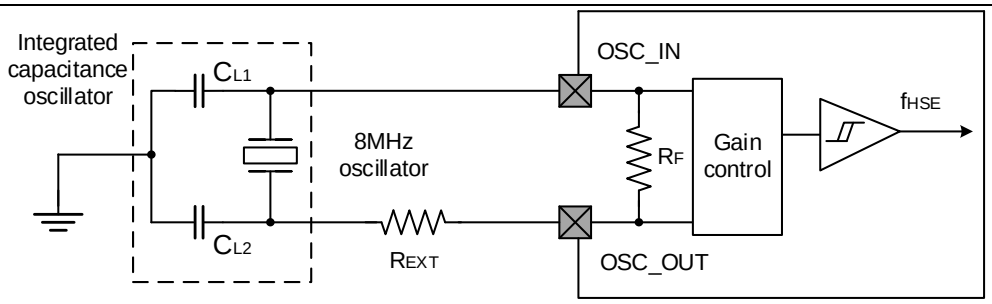
- **A high-speed external clock generated by using a crystal / ceramic resonator**

The high speed external clock (HSE) can be generated using an oscillator consisting of a 4～20 MHz crystal/ceramic oscillator. The information given in this section is based on the use of typical external components listed in the table below. In applications where the oscillator and load capacitance must be as close to the oscillator pin as possible to reduce output distortion and stability time at startup. For detailed parameters of crystal oscillator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer (the crystal resonators mentioned here are usually referred to the passive crystal oscillator).

HSE 4～20 MHz Oscillator Characteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	20	MHz
C_{L1} C_{L2}(3)	The suggested load capacitance and corresponding crystal serial resistance（R_S）	R_S = 30 Ω	-	20	--	pF
i_2	HSE drive current	V_{DD}=3.3 V, V_{IN}=V_{SS} 30pF load	-	1.1	1.6	mA
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stable		3		ms

1. The parameters of the resonator are given by the crystal resonator manufacturer.
2. Guaranteed by design and comprehensive assessment, not tested in production.
3. For CL1 and CL2, it is recommended to use high quality ceramic dielectric capacitance (typically) between 5pF and 25pF designed for high-frequency applications, and to select suitable crystals or resonators. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of CL1 and CL2. The capacitive reactance of PCB and MCU pins should be taken into account when selecting CL1 and CL2.
4. tSU(HSE) is the startup time. It is measured from the time when HSE is enabled by software until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.



Typical applications of using 8MHz crystals

Note: The value of R_{EXT} is depended on the crystal characteristic.

- A low-speed external clock generated by using a crystal / ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic oscillator. The information given in this section is based on the use of typical external components listed in the table below. In applications where the oscillator and load capacitance must be as close to the oscillator pin as possible to reduce output distortion and stability time at startup. For detailed parameters of crystal oscillator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer (the crystal resonators mentioned here are usually referred to the passive crystal oscillator).

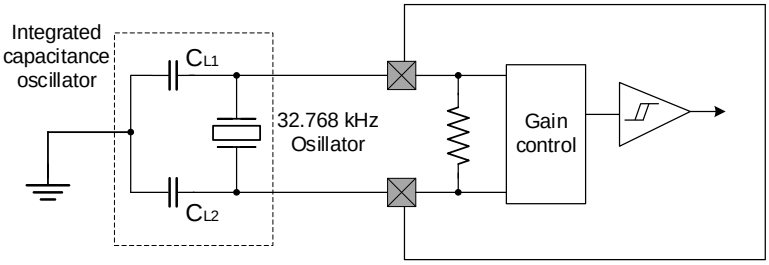
Note: For CL1 and CL2, high quality porcelain dielectric capacitors between 5 p F and 15 p F and well-compliant crystals or oscillators are recommended. Usually, CL1 and CL2 have the same parameters. Crystal manufacturers usually give the parameters of the load capacitance as a serial combination of CL1 and CL2.

Load capacitance CL is calculated by the following equation: CL = CL1 CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitor of the pin and the capacitor associated with the PCB board or PCB.

LSE Oscillator Characteristic (f_{LSE}=32.768 kHz)(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{L1} C_{L2}(2)	Recommended load capacitance and corresponding crystal serial impedance (RS)(3)	R_S:30 KΩ~65 KΩ	-	-	20	pF
I2	LSE drive current	VDD=3.3 V CL1=CL2=12.5 pF R_S= 30 KΩ	-	0.3	-	μA
$t_{SU(LSE)}$(4)	Startup time	VDD is stable	-	2	-	s

1. Guaranteed by design and comprehensive assessment, not tested in production.
2. See the attention and warning paragraph above this table.
3. Choose high quality oscillator with a small RS value that can optimize current consumption. Check with the crystal manufacturer for more details.
4. $t_{SU(LSE)}$ is the start time, measured from the software enabling LSE, until the stable 32.768 KHz oscillation is stabled.This value is measured on a standard crystal oscillator, which may vary greatly by the crystal manufacturer.



Typical applications of using 32.768 kHz crystals

1.13 Controller internal clock source characteristics

- **High speed internal (HSI) RC Oscillator**

HSI Oscillator Characteristic(1)(2)

Sign	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	Frequency	VDD=3.3 V，T_A= 25 ℃，after calibration	7.92	8	8.08	MHz
ACC_{HSI}	HSI oscillator temperature drift	VDD=3.3 V，T_A= -40~105 ℃，temperature drift	-3	-	3	%
		VDD=3.3 V，T_A= - 10~85 ℃，temperature drift	-2.5	-	2	%
		VDD=3.3 V，T_A= 0~70 ℃，temperature drift	-2	-	1.5	%
$t_{SU(HSI)}$	HSI oscillator startup time		1	-	3	μs
$I_{DD(HSI)}$	HIS oscillator power consumption		-	80	150	μA

1. Unless otherwise specified, VDD = 3.3 V，TA = -40~85 ℃.
2. Guaranteed by design and comprehensive assessment, not tested in production.

- **Low speed internal (LSI) RC oscillator**

LSI Oscillator Characteristic(1)

Sign	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	output frequency	25℃ calibration, VDD =3.3 V	29	30	31	KHz
		VDD =1.8 V ~5.5 V, TA = -40~105 ℃	24	30	36	KHz
$t_{SU(LSI)}$ (3)	LSI oscillator start time		-	30	80	μs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption		-	0.2	-	μA

1. Unless otherwise specified, VDD = 3.3 V，TA = -40~85 ℃.
2. Guaranteed by design and comprehensive assessment, not tested in production.

1.14 Controller low-power mode wake-up time

The arousal times listed in the table below are measured during the arousal phase of an 8MHz HIS RC oscillator. The clock source used on wake-up depends on the current mode of operation:

- Stop or Sleep mode：the clock source is RC oscillator
- Sleep mode：clock source is the clock used when entering into sleep mode

Wake-up time in the low-power mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Awaken from sleep mode	16	HCLK(2)
t_{WUSTOP}(1)	Awaken from stop mode	20	us
t_{WUPD}(1)	Awaken from stanby mode	55	us

1. The awaken time counts from the beginning of the wake up event until the user program reads the first instruction;
2. HCLK is the AHB clock frequency.

1.15 PLL characteristics

Controller internal PLL characteristics

Symbol	Parameter	Num.			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock (2)	4	8	20	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	48	-	72	MHz
t_{LOCK}	PLL Ready indicates signal output time	-	-	50	μs
Jitter	TIE RMS Jitter	-	40	-	pS
Ipll	Operating Current of PLL @48 MHz VCO frequency.	-	300	500	uA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Need to pay attention to using the correct frequency multiplication factor, so that f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

1.16 FLASH characteristics

FLASH characteristics

Symbol	Parameter	Condition	Min(1)	Typ(1)	Max(1)	Unit
t_{prog}	Word programming time(32-bit)	TA = -40~85 ℃	-	175	-	μs
t_{ERASE}	Page erase time(512Bytes)	TA = -40~85 ℃	-	2.27	-	ms
t_{ME}	Mass erase time	TA = -40~85 ℃;	-	34.1	-	ms
I_{DD}	Supply current (1)	Read, f_{HCLK}=48 MHz，VDD=3.3 V	-	2	2.4	mA
		Write, f_{HCLK}=48 MHz，VDD=3.3 V	-	-	1.2	mA
		Erase, f_{HCLK}=48 MHz，VDD=3.3 V	-	-	0.6	mA
		PD mode， VDD=3.3~3.6 V	-	-	150	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Flash memory life and data retention period

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance (Note: erasing and writing cycle)	TA = -40~85°C；	100	kcycles
t_{RET}	Data retention	TA = 85°C，after 1000 erasing and cycle	10	years

1. Guaranteed by design and comprehensive evaluation, not tested in production.

1.17 I/O port characteristic

- Generic input/output characteristics

All of the I/O ports are compatible with CMOS and TTL.

I/O static characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
VIH	Low level input voltage	3.3	-	-	0.8	V
		1.8	-	-	0.2×VDD	
VIH	High level input voltage	3.3	-	2.0	-	
		1.8	-	0.8×VDD	-	
Vhys	I/O Schmitt trigger voltage Hysteresis (1)	3.3/1.8	-	0. 1×VDD	---	V
Ilkg (2)	Input leakage current IIH	3.3/1.8	-	---	1	μA
	Input leakage current IIL	3.3/1.8	-	-1	-	
VOH	Output high level voltage	3.3	High driving Imin=8 mA low driving Imin=4 mA	2.4	-	V
		1.8	High driving Imin=4 mA low driving Imin=2 mA	VDD-0.45	-	
VOL	Output low level voltage	3.3	High drivingImin=8 mA low driving Imin=4 mA	-	0.45	
		1.8	High driving Imin=4 mA low driving Imin=2 mA	-	0.4	
RPU	Internal pull-up resistor	3.3/1.8	-	40	100	kΩ
RPD	Internal pull-down resistor	3.3/1.8	-	40	100	kΩ
CIO	I/O pin capacitance	3.3/1.8	-	-	10	pF

1. The hysteresis voltage of the Schmitt trigger switching level. Guaranteed by design and comprehensive evaluation, not tested in production.

2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take most of the strict CMOS process or TTL parameters into account.

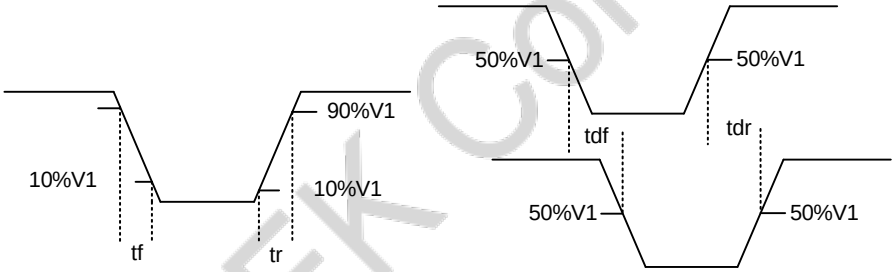
- Input and output AC characteristics

The parameters and definition of I/O AC are shown as followed.

I/O AC characteristics

VDD	Condition			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
3.3V (2.7~3.6)	Low (DR=1)	Slow (SR=1)	25	4	5.5	11	6.6	10	20
			50	7.5	9.5	18	8.5	12	24
			100	15	17	32	13	16	31
		Fast (SR=0)	25	3.8	4.9	9.2	5.9	8.8	18
			50	7.3	8.8	16.2	7.8	10.8	21.2

VDD	Condition			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
			100	14.2	16.7	30.5	12	15	29
	High (DR=0)	Slow (SR=1)	25	2.4	3.7	7.2	5.5	8.5	17.1
			50	3.9	5.5	10.5	6.5	9.6	19.2
			100	7.3	9.3	17.2	8.4	12	23
		Fast (SR=0)	25	2	3.1	5.9	4.9	7.6	16
			50	3.7	4.9	9.5	5.8	8.7	18
			100	7.2	8.8	17	7.7	11	22
1.8V (1.62~1.98)	Low (DR=1)	Slow (SR=1)	25	8	12	22	14	23	44
			50	15	20	36	18	27	52
			100	29	36	65	26	36	66
		Fast (SR=0)	25	7.5	10.5	16.4	12.25	20	40
			50	14.5	18.5	33	16.5	24.2	47
			100	28	35	62	24	33	62
	High (DR=0)	Slow (SR=1)	25	4.6	8	15.4	12	20.2	40
			50	7.6	11.8	22	14	22.5	44
			100	11.5	19.5	36	17.5	26.7	52
		Fast (SR=0)	25	4	6.9	14	10.5	18	36
			50	7.3	11	20	12.3	20	40
			100	15	18.5	33	16	25	47



I/O AC characteristic definition

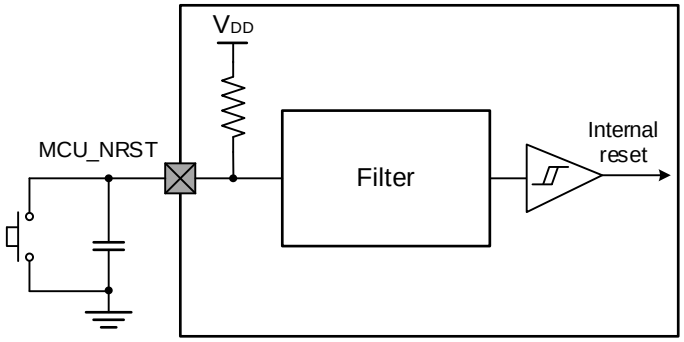
1.18 MCU_NRST Pin Characteristics

NRST pin input driver uses CMOS technology. MCU_NRST pin is connected to a pull-up resistor that cannot be disconnected.

NRST Pin Characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST low level input voltage	1.8 V~3.6 V	-	-	0.3 VDD	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	1.8 V~3.6 V	0.7VDD	-	-	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	1.8 V~3.6 V	-	220	-	mV
R_{PU}	Internal pull-up resistor(2)	1.8 V~3.6 V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	1.8 V~2 V	-	-	100	ns
		3 V~3.6 V	-	-	100	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	1.8 V~2 V	650	-	-	ns
		3 V~3.6 V	300	-	-	

Symbol	Parameter	VDD	Min	Typ	Max	Unit
1. The reset network is to prevent parasitic reset. 2. Users must ensure that the potential of the NRST pin can be lower than the maximum VIL (NRST), otherwise the MCU cannot be reset.						



NRST pin protection recommended circuit design

1.19 TIM characteristic

TIMx(1) Characteristic

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$= 48 MHz	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48 MHz	20.8	-	ns
f_{EXT}	Timer external clock frequency from CH1 to CH2	$f_{TIMxCLK}$= 48 MHz	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	$f_{TIMxCLK}$= 48 MHz	-	16	bit
$t_{COUNTER}$	Select the internal clock, 16-bit counter clock cycle	$f_{TIMxCLK}$= 48 MHz	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48 MHz	0.0208	1365	μs
t_{MAX_COUNT}	Maximum count	$f_{TIMxCLK}$= 48 MHz	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48 MHz	-	89.478	s
1. TIMx is a common name and stands for TIM1~TIM8.					

1.20 I2C Characteristic

The I2C interface complies with the standard I2C communication protocol while SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD will be turned off, but still exists.

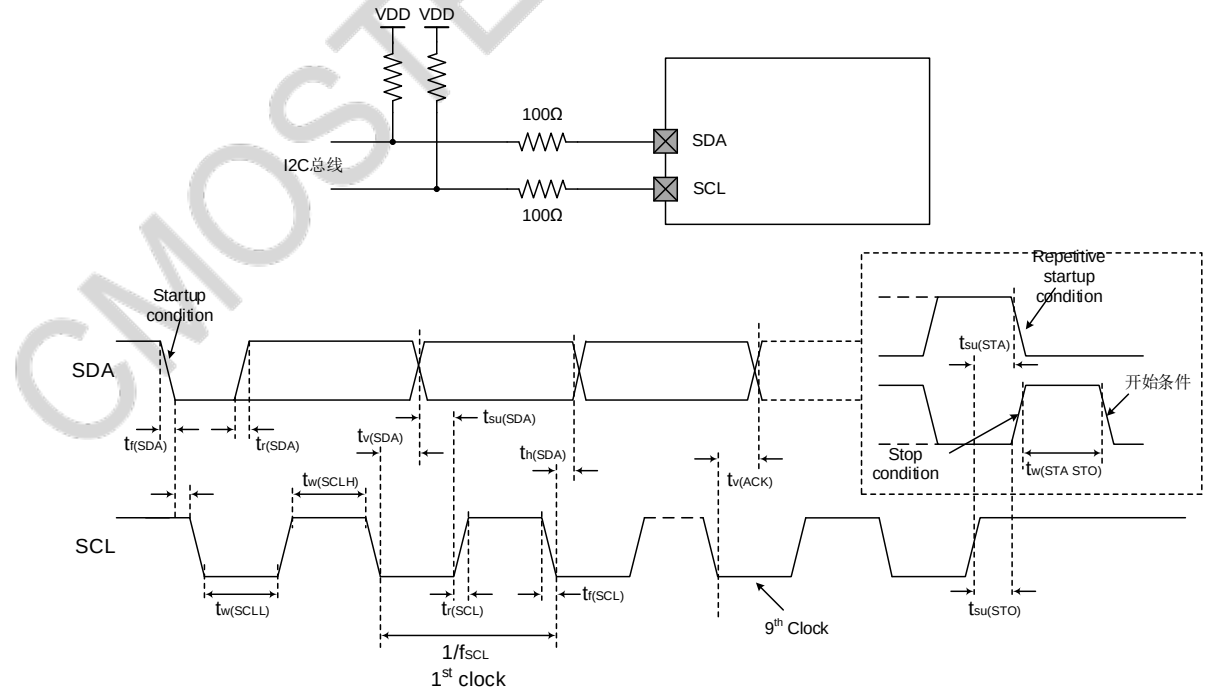
The I2C interface characteristic is shown as the following table. As for the specification of I/O reset function pins (SDA and SCL), please refer to chapter 1.17.

I²C Characteristics

Symbol	Parameter	Standard model		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz
$th_{(STA)}$	Start condition holding time (1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL Clock Low Time (1)	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time (1)	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Establishment time of repeated starting conditions (1)	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data retention time (1)	-	3.4	-	0.9	-	0.4	μs
$t_{su(SDA)}$	Establishment time of SDA (1)	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (1)	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (1)	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Establishment time of stop condition(1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
Cb	Capacity load per bus (1)	-	400	-	400	-	200	pf
$t_{v(SDA)}$	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs
$t_{v(ACK)}$	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.

2. To achieve the maximum frequency of standard mode I2C, FPCLK1 must be greater than 2 MHz.To achieve the maximum frequency of fast mode I2C, FPCLK1 must behigher than 4 MHz.



I²C Bus AC waveform and measurment circuit (1)

1. The measuring point is set at CMOS level: 0.3 VDD and 0.7 VDD.

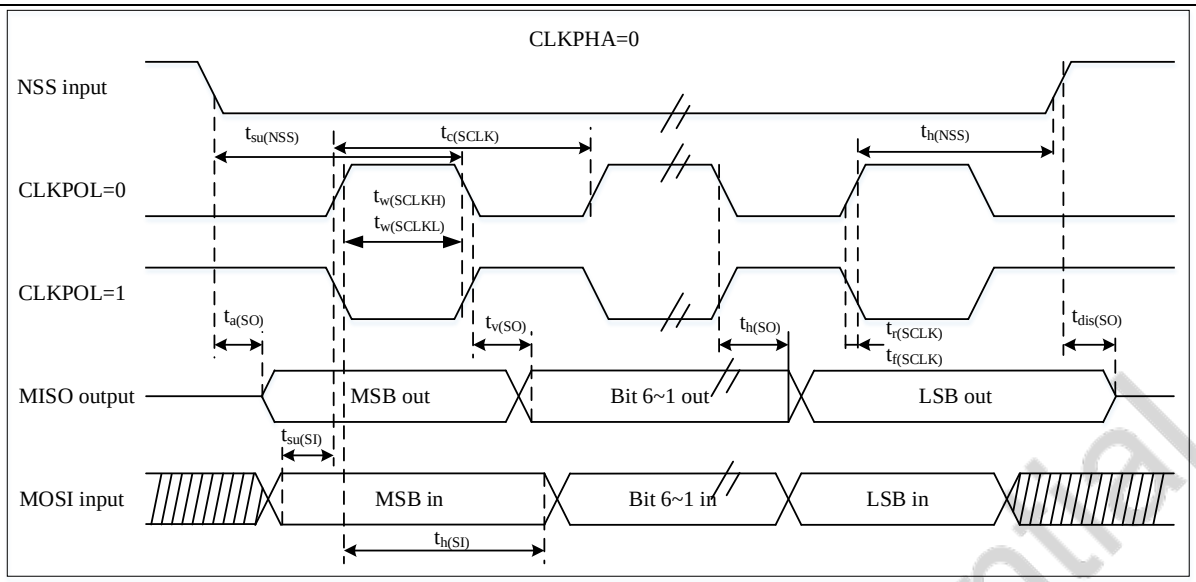
1.21 SPI/I2S Characteristic

For feature details of the input and output multiplexing pins (WS, CLK, SD of NSS, SCLK, SPI, MOSI, MISO, I2S,), see Section 1.17.

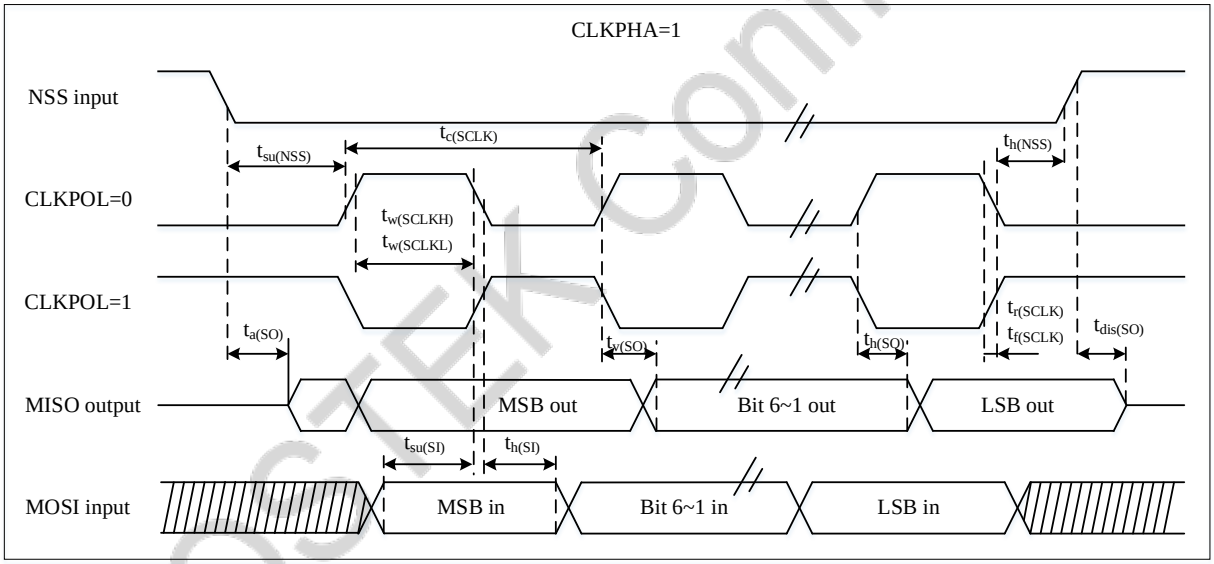
SPI Characteristics(4)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCLK}	SPI clock frequency	Master mode		-	18	MHz
$1/t_{c(SCLK)}$		Slave mode		-	18	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30 pF		-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI Slave mode		30	70	%
$t_{su(NSS)}$(1)	NSS establishment time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS retention time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}	t_{PCLK}+ 2	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	SPI 1	19.84	-	ns
			SPI 2	20.5	-	
$t_{su(SI)}$(1)		Slave mode	SPI 1	4.16	-	
			SPI 2	4.16	-	
$t_{h(MI)}$(1)	Data input retention time	Master mode		0	-	ns
$t_{h(SI)}$(1)		Slave mode		4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode， f_{PCLK} = 20 MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Disabled time for data output	Slave mode		2	10	ns
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after the enabled edge)	SPI 1	-	32	ns
			SPI 2	-	30	
$t_{v(MO)}$(1)		Mastermode (after theenabled edge)	SPI 1	-	28	
			SPI 2	-	28	
$t_{h(SO)}$(1)	Data output retention time	Slave mode (after the enabled edge)		0	-	ns
$t_{h(MO)}$(1)		Master mode (after the enabled edge)		0	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.
3. The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data line in the high resistance state.
4. Test voltage is 3.3 V.

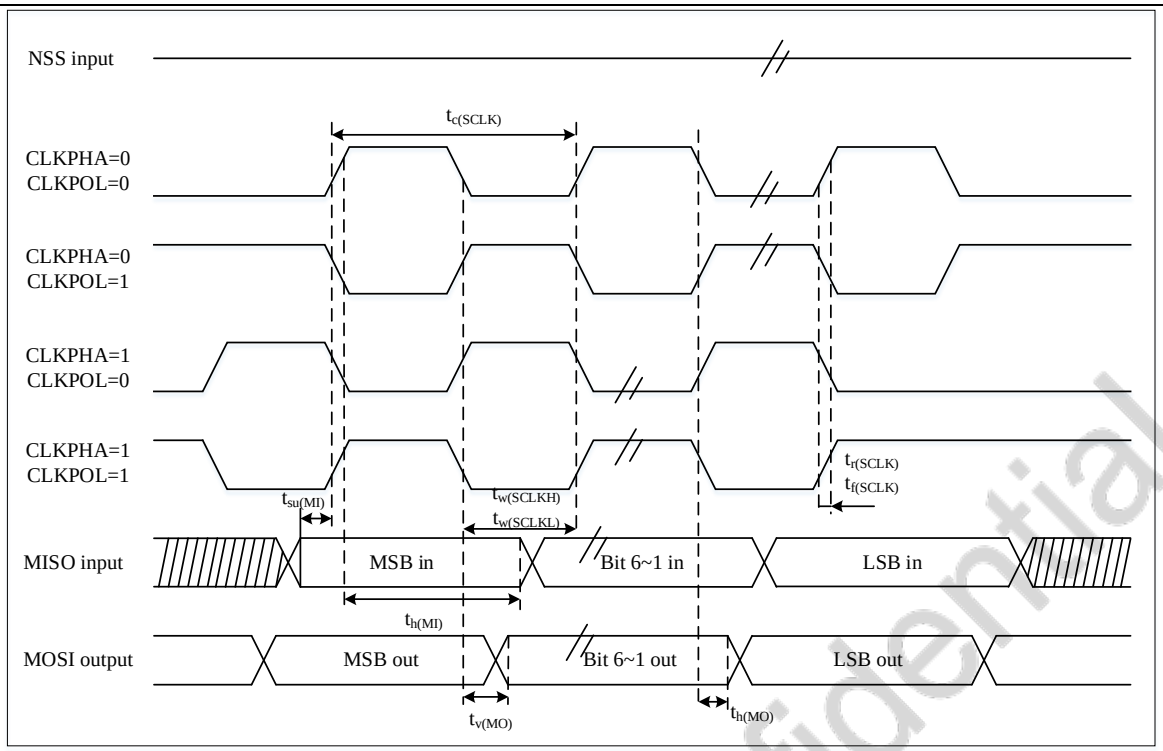


SPI sequence diagram – slave mode and CPHA=0



SPI sequence diagram - slave model and CPHA=1(1)

1. The measurement points are set at CMOS level: 0.3 VDD and 0.7 VDD.



SPI Sequnece diagram – master mode(1)

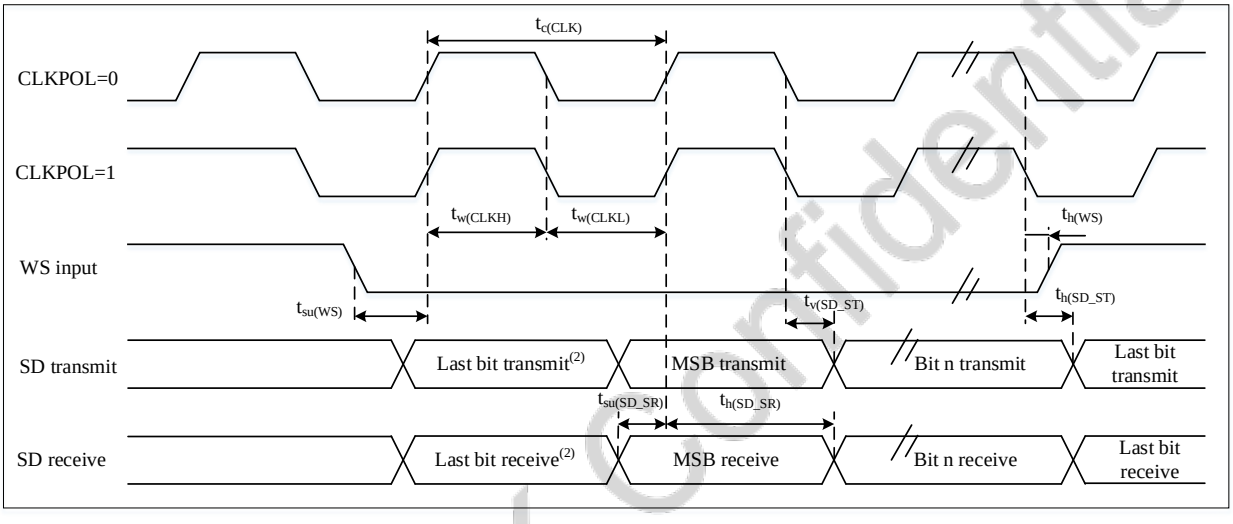
1. The measurement points are set at CMOS level: 0.3 VDD and 0.7 VDD.

I²S Charateristic(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DuCy (SCK)	I2S from the input clock duty cycle	I2S Slave mode	30	50	70	%
f_{CLK} $1/t_{c(CLK)}$	I2S clock frequency	Master mode (16 bit)	-	2*Fs(3) *16	-	Hz
		Master mode (16 bit)	-	2*Fs(3) *16	-	
		Master mode (32 bit)	-	2*Fs(3) *32	-	
		Slave mode (32 bit)	-	2*Fs(3) *32	-	
$t_{r(CLK)}$	I2S clock up and down time	Load capacitance: CL = 50 pF	-	-	8	ns
$t_{v(WS)}$ (1)	WS validity time	Master mode	13.5	-	-	
$t_{h(WS)}$(1)	WS retention time	Master mode	0	-	-	
$t_{su(WS)}$(1)	WS establishment time	Slave mode	4	-	-	
$t_{h(WS)}$(1)	WS retention time	Slave mode	0	-	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, f_{PCLK} = 16 MHz, audio 48 kHz	312.5	-	-	
$t_{w(CLKL)}$(1)			345	-	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	master receiver	3.6	-	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	3.5	-	-	

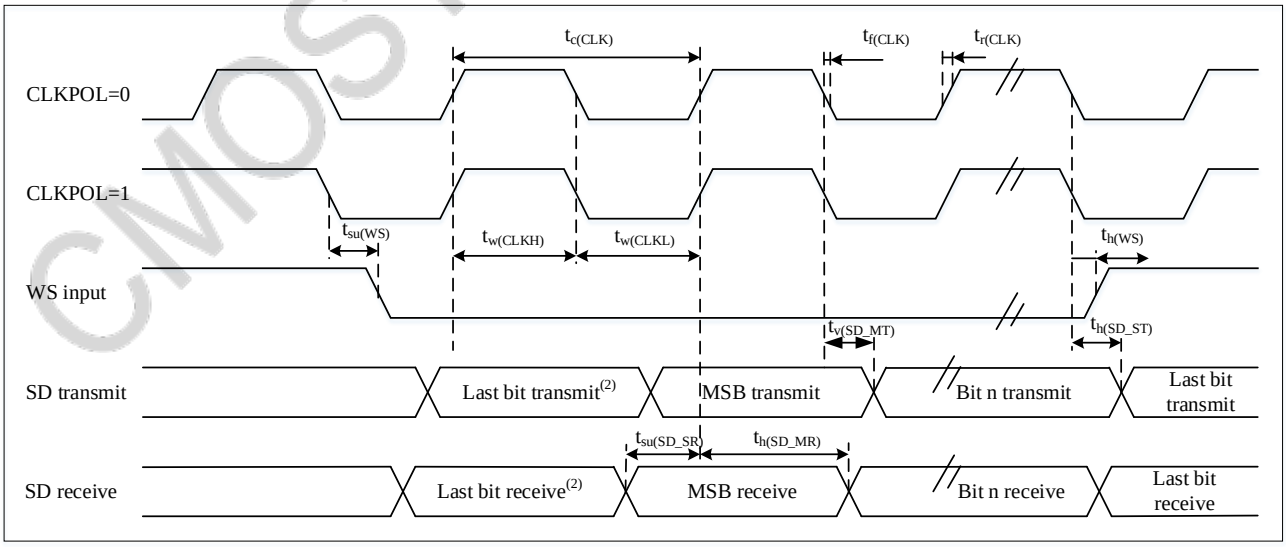
$t_{h(SD\_MR)}$(1)(2)	Data entry retention time	master receiver	0	-	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0	-	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after the enabled edge)	-	-	29.76	ns
$t_{h(SD\_ST)}$(1)	Data output retention time	Slave generator (after the enabled edge)	0	-	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	master generator (after the enabled edge)	-	-	13.6	
$t_{h(SD\_MT)}$(1)	Data output retention time	master generator (after the enabled edge)	-6.5	-	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Relying on f_{PCLK} . For example, if f_{PCLK} =8 MHz, then T_{PCLK}=1/f_{PCLK}=125 ns.
3. FS value audio sampling frequency, frequency range 8 KHz ~ 96 KHz.



I²S slave mode timing diagram (Philipsprotocol)(1)

1. The measuring point is set at the CMOS level: 0. 3 V_{DD} and 0. 7 V_{DD}.
2. Send/receive the lowest bit of the previous byte. There is no send/receive at the lowest level until the first byte.



I²S master mode timing diagram (Philipsprotocol)(1)

1. The measuring point is set at the CMOS level: 0.3 V_{DD} and 0.7 V_{DD} .

2. Send/receive the lowest bit of the previous byte. There is no send/receive at the lowest level until the first byte.

1.22 ADC Characteristic

ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.4	3.3	5.5	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	-	-	18	MHz
f_s(1)	Sampling rate	-	-	0.89	1.33	Msps
V_{AIN}	Conversion voltage range (2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC input resistance	V_{DDA} =3.0 v	-	1500	-	Ω
C_{ADC}(1)	Internal sample and holding capacitor	-	-	13	15	pF
SNDR	Signal noise distortion ration	V_{DDA} =3.3 v	-	68	-	dB
t_S(1)	Sampling time	-	6	-	-	$1/f_{ADC}$
t_{STAB}(1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV}(1)	Conversion time	-	12			$1/f_{ADC}$

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. VREF+ is internally connected to VDDA。

Formula 1：maximum RAIN formula

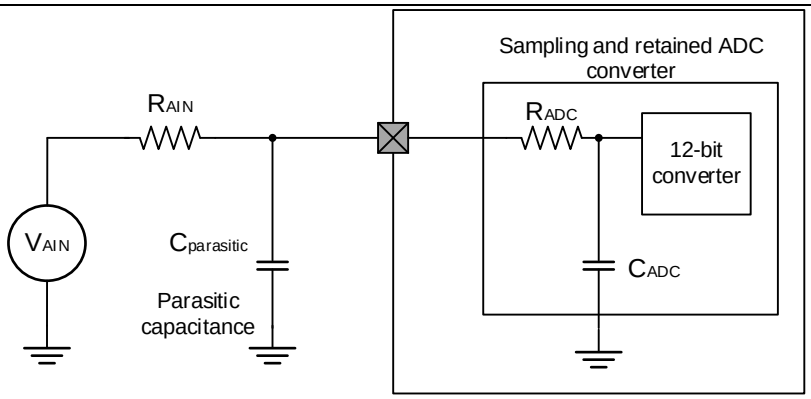
$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula is used to determine the maximum impedence so that the error can be less than 1/4 LSB, where N=12(representing 12 bit resolution).

ADC Accuracy(1)(2)

Symbol	Parameter	Conditions	Typ	Max	Unit
EG	Gain error	V_{REF+} = 3.3 V， T_A = 25 °C， Vin = 0.05 V_{DDA}~ 0.95 V_{DDA}	±2	±5	LSB
EO	Offset error		±0.5	±2.0	
ED	Differential linearity error		±0.6	1.5	
EL	Integral linearity error		±1.5	2.5	
ENOB	Effective number of bits		11	-	Bits

1. DC numerical accuracy of the ADC is measured after internal calibration.
2. Relationship between the reverse injection current and ADC accuracy: it is needed to avoid reverse current injected on any standard analog input pin, as this will significantly reduce conversion accuracy of the other ongoing analog input pin . It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current.
3. Guaranteed by design and comprehensive evaluation, not tested in production.



ADC typical connection diagram

1.23 Operational Amplifier (OPAMP) Characteritic

OPAMP Characteritic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	2.4	-	5.5	V
CMIR	Common mode voltage input range	-	0	-	VDDA	V
VIOFFSET	Input offset voltage	-	-	4	-	mV
ILOAD	Drive current	-	-	0.5	-	mA
IDDA	OPAMP current consumption Common mode rejection ratio	No load, quiescent mode	-	0.5	-	mA
CMMR	Power supply rejection ratio	-	-	70	-	dB
PSRR	Gain bandwidth	-	-	60	-	dB
GBW	Conversion rate	-	-	2.5	-	MHz
SR	Minimum impedance load	-		3	-	V/us
RLOAD	Maximum capacitive load	-	10	-	-	KΩ
CLOAD	Startup time	-	-	-	25	pF
TSTARTUP	Analog supply voltage	CLOAD ≤ 25 pf, RLOAD ≥ 10 kΩ, Follower configuration	-	3	5	μs
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 25 pF, Rload = 10 KΩ	-	1	-	MHz
		GA Gain = 4, Cload = 25 pF, Rload = 10 KΩ	-	0.5	-	
		GA Gain = 16, Cload = 25 pF, Rload = 10 KΩ	-	0.125	-	
		GA Gain = 32, Cload = 25 pF, Rload = 10 KΩ	-	0.0625	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

1.24 COMP Characteristic

COMP Characteristic

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VDDA	Analog supply voltage	-		2.2	-	5.5	V
VIN	Input voltage range	-		0	-	VDDA	
TSTART	Comparator startup time	normal mode		-	-	5	us
		low speed mode		-	-	15	
td	Propagation delay for 200 mV step with 100 mV overdrive	VDDA>=2.2 V normal mode		-	100	-	ns
		low speed mode		-	520	-	
VOFFSET	Comparator input offset error	Full common mode range		-	±4	±20	mV
Vhys	Comparison of hysteresis voltage (high speed/low power consumption)	No hysteresis		-	0	-	mV
		Low hysteresis		-	10/8	-	
		Medium hysteresis		-	20/15	-	
		High hysteresis		-	30/25	-	
IDDA	Comparator current consumption	High speed mode	Static	-	35	-	µA
			With 50 kHz ±100 mV overdrive square signal	-	36	-	
		Low speed mode	Static	-	5	-	
			With 50 kHz ±100 mV overdrive square signal	-	6	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

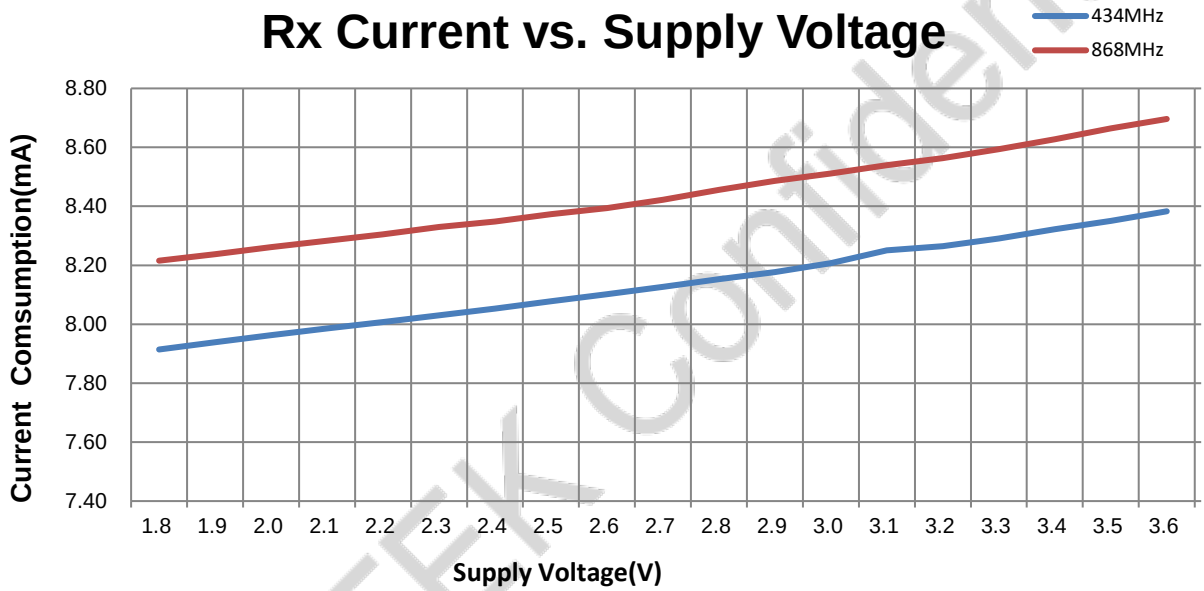
1.25 Temperature Sensor (TS) Characteristics

Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±2	-	ºC
Avg Slope(1)	Average slope	-	3.9	-	mV/ºC
V_{25}(1)	Voltage at 25ºC	-	1.3	-	V
t_{START}(1)	Startup time	-	11	22	μs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	-	1.87	6.43	μs

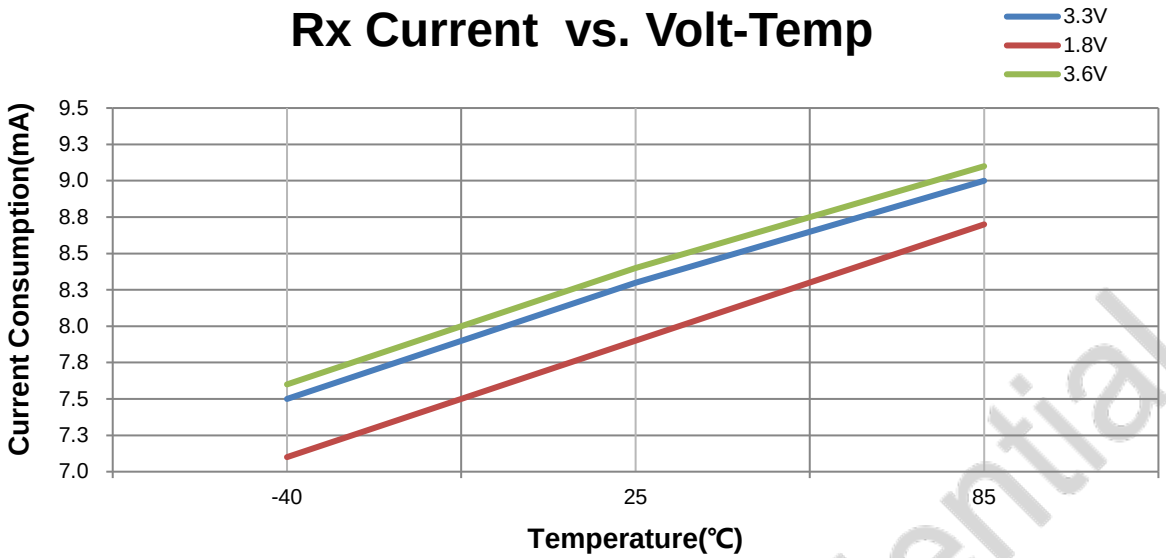
1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The shortest sampling time can be determined by the application through multiple cycles.

1.26 Rx Current VS. Supply Voltage

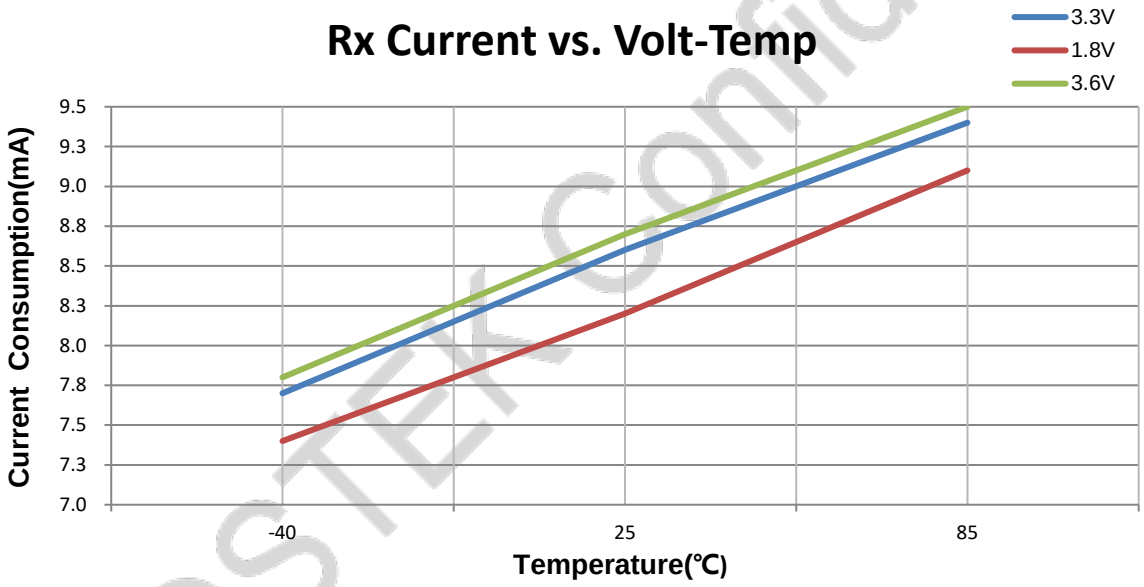


Test Condition：Freq=434 MHz / 868 MHz, Fdev=10 KHz, BR=10 Kbps

1.27 Rx Current/Voltage vs. Temperature

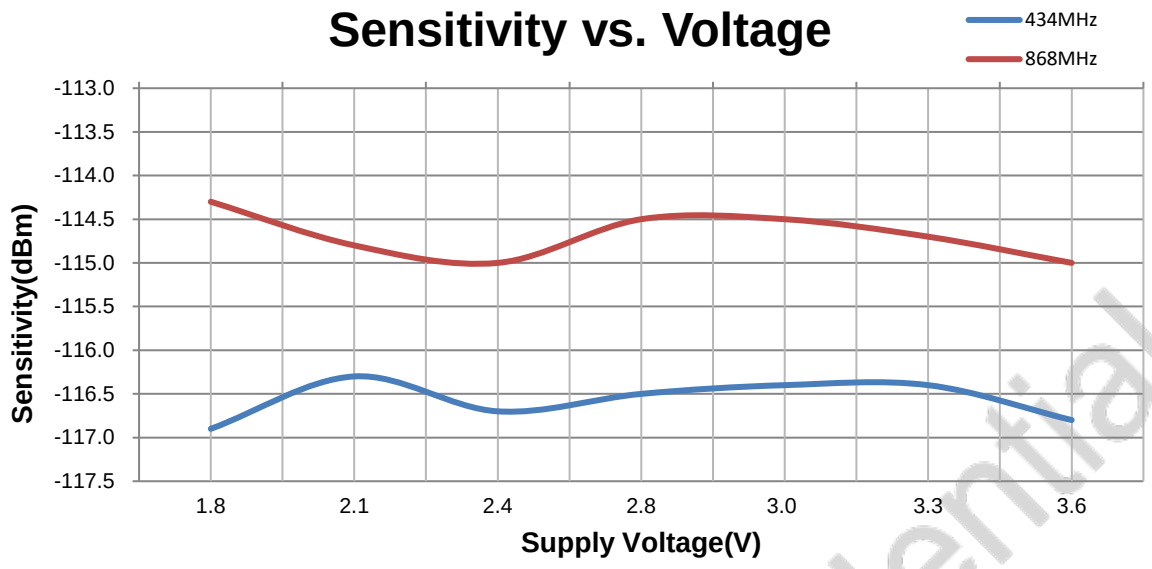


Test Condition：Freq = 434 MHz, Fdev = 10 KHz, BR = 10 Kbps



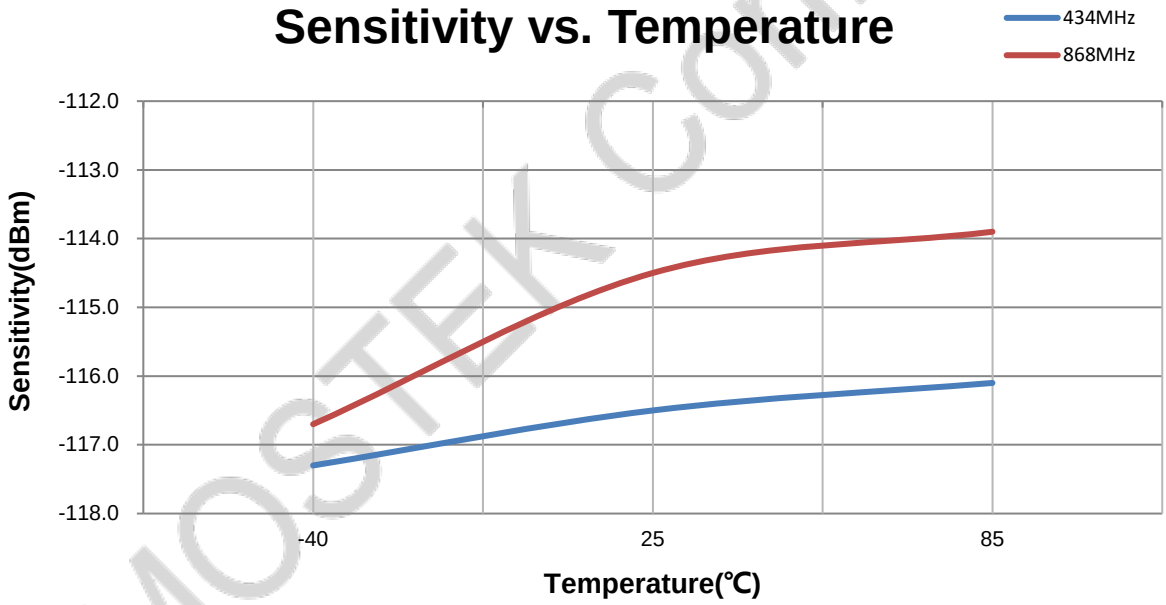
Test Condition：Freq = 868 MHz, Fdev = 10 KHz, BR = 10 Kbps

1.28 Sensitivity vs. Supply Voltage



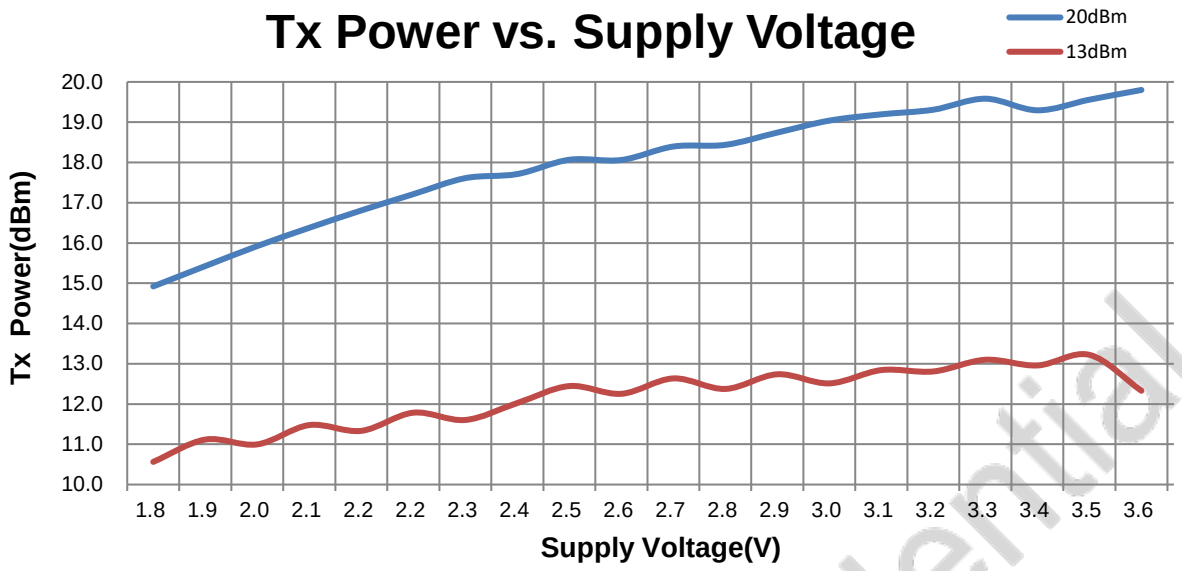
Test Condition：FSK modulation, DEV = 10 KHz, BR = 10 Kbps

1.29 Sensitivity vs. Tmeperature

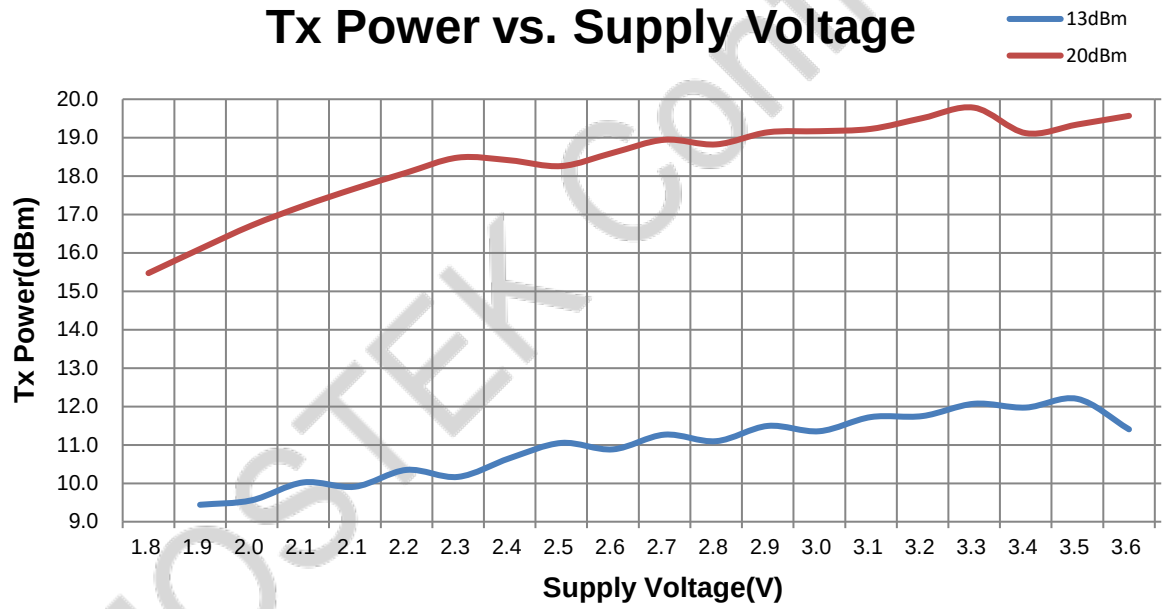


Test Condition：FSK modulation, DEV = 10 KHz, BR = 10 Kbps

1.30 Tx Power vs. Supply Voltage

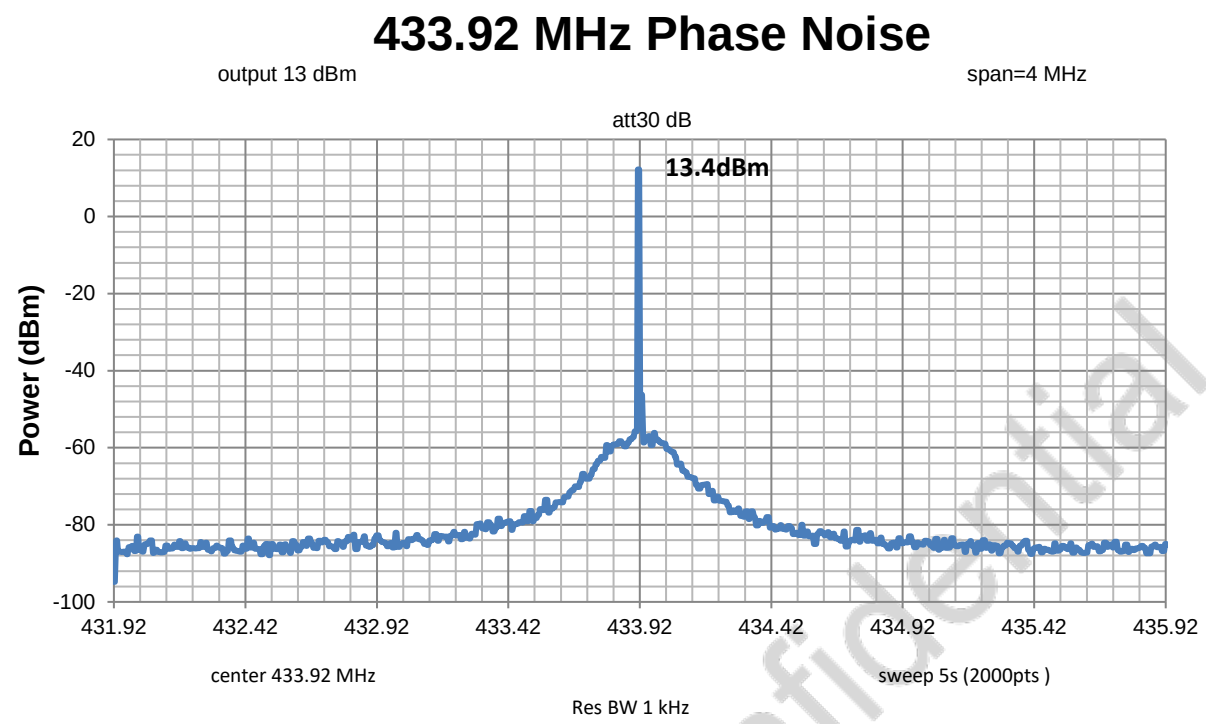


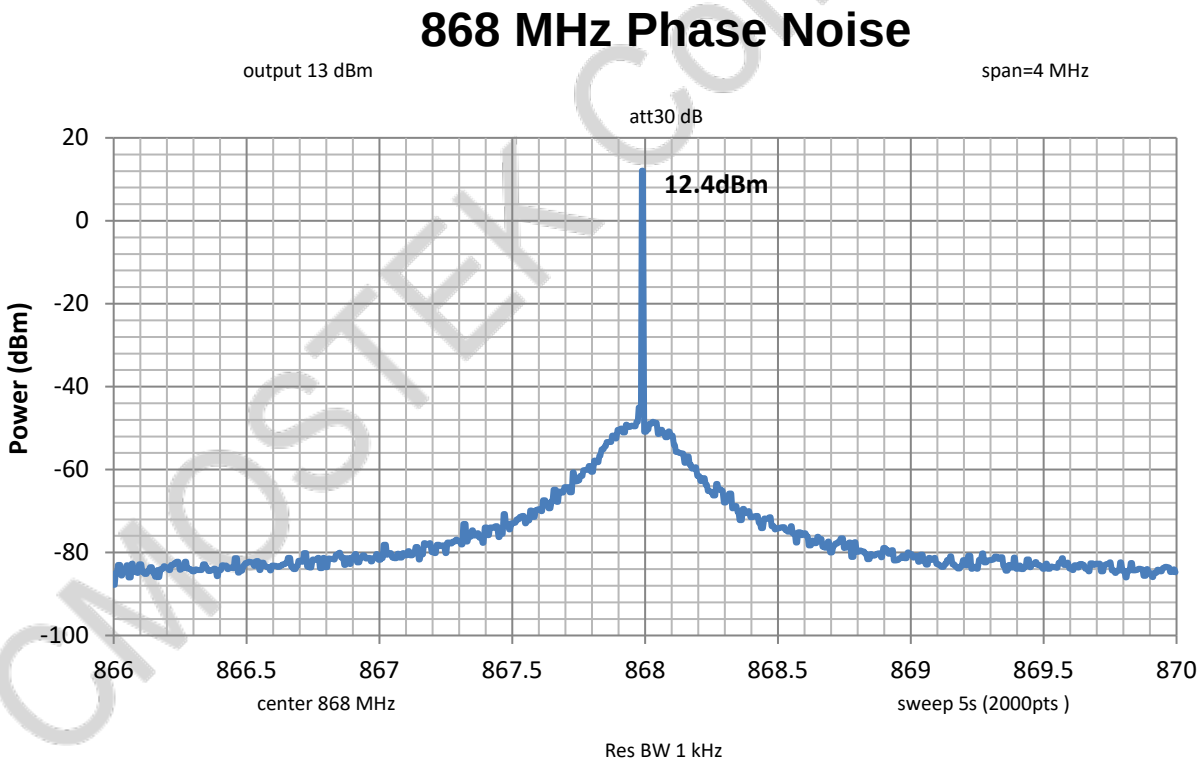
Test Condition：Freq = 434 MHz, 20 dBm / 13 dBm matching network



Test Condition：Freq = 868 MHz, 20 dBm / 13 dBm matching network

1.31 Tx Phase Noise





2 Pin Description

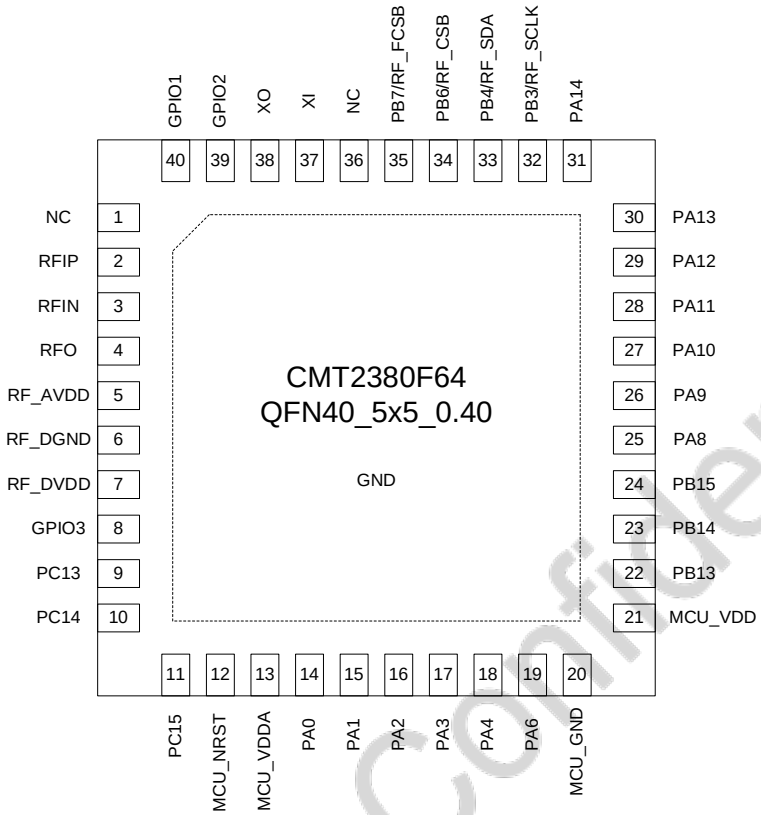


Figure 1. CMT2380F64 Pin Diagram

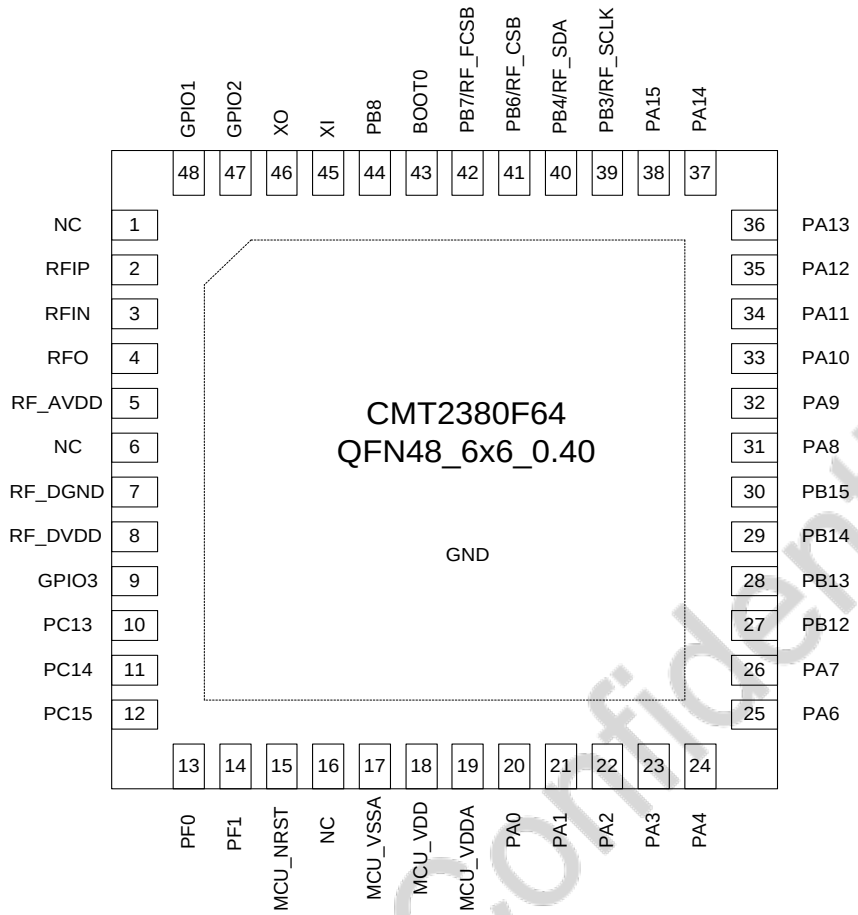


Figure 2. CMT2380F64 QFN48 Pin Diagram

Table 2. CMT2380F64 (QFN40/QFN48) Pin description

Pin name	Pin number		I/O	Description
	QFN 40	QFN 48		
GND	0	0	Analog	Chip substrate, connected to GND
NC	1	1	-	No connection
RFIP/RFIN	2 - 3	2 - 3	Analog	RF signal input port
RFO	4	4	Analog	PA output
RF-AVDD	5	5	Analog	RF circuit VDD, required to connect to supply voltage of 1.8-3.6 V
RF-DGND	6	7	Digital	RF module digital GND
NC	-	6	-	No connection
RF-DVDD	7	8	Digital	RF module digital VDD, required to connected to supply voltage of 1.8-3.6 V
GPIO3	8[2]	9[2]	IO	RF module GPIO 3，it can be configured as： CLKO，DOUT/DIN，INT2，DCLK (TX/RX)
PC13	9	10	IO	MCU port PC 13
RTC_TAMP1			I	RTC invasive event detect input 1
RTC_TS			I	RTC event input

RTC_OUT			O	RTC Output function (256 Hz or 1 Hz)
WKUP1			I	MCU enters into PD mode and awakens input signal 1
PC14	10	11	IO	MCU port PC 14
OSC32_IN			Analog	MCU external 32768 Hz crystal input pin
PC15	11	12	IO	MCU port PC 15
OSC32_OUT			Analog	MCU external 32768 Hz crystal output pin
PF0	-	13	IO	MCU port PF0
I2C1_SDA			IO	I2C1 serial data signal
OSC_IN			I	Crystal input pin
OPAMP_VINP			Analog	Positive operational amplifier input
I2C1_SCL			O	I2C1 serial clock signal
USART1_CK			O	USART 1 synchronously transmitted clock output signal
USART2_CK			O	USART 2 synchronously transmitted clock output signal
OSC_OUT			O	Crystal output pin
MCU_NRST	12	15	I	MCU reset ports, low level valid
NC	-	16	-	No connection
MCU_VSSA	-	17	S	Analog ground
MCU_VDD	-	18	S	Complementary power supply
MCU_VDDA	13	19	Analog	MCU analog power supply +
PA0	14	20	IO	MCU port PA0
USART1_CTS			I	Clearing signal is received in USART 1 flow control
USART2_CTS			I	Clearing signal is received in USART 2 flow control
USART2_RX			I	RxD of USART 2
LPUART_TX			O	TxD of LPUART
LPUART_RX			I	RxD of LPUART
SPI1_SCK			IO	SPI 1 clock signal
I2S_CLK			IO	I2S serial clock signal
LPTIM_IN1			I	LP Timer input signal channel 1
TIM8_CH1			IO	Timer8 I/O channel 1
RTC_TAMP2			I	RTC intrusion event detect input 2
WKUP0			I	MCU enters PD mode and awakens the input signal 0
COMP_INM			Analog	Comparator negative input port
COMP_OUT			Analog	Comparator output
ADC_IN0			Analog	ADC input channel 0
OPAMP_VINP			Analog	Operational amplifier input positive
PA1	15	21	IO	MCU port PA1
USART1_RTS			O	Flow control of USART 1 transmitting query signal
USART2_RTS			O	Flow control of USART 2 transmitting query signal
EVENT_OUT			O	Event output
SPI1_NSS			IO	SPI 1 chip selected signal
I2S_WS			IO	I2S channel selected signal
I2C1_SMBA			I	I2C1 Warning signal in SMBus mode (optional)
LPTIM_IN2			I	Input signal channel 2 of LP Timer

LPUART_TX			O	TxD of LPUART
TIM8_CH2			IO	Timer 8 I/O channel 2
TIM3_ETR			I	Timer 3 External trigger input signal
COMP_INP			Analog	Comparator positive input port
ADC_IN1			Analog	ADC input channel 1
OPAMP_VINP			Analog	Operational amplifier positive input
PA2	16	22	IO	MCU port PA 2
USART1_TX			O	TxD of USART 1
USART2_TX			O	TxD of USART 2
TIM8_CH3			IO	Timer 8 I/O input channel 3
SPI1_MOSI			IO	SPI 1 Master output / slave input signal
I2S_SD			IO	I2S serial data signal
TIM1_BKIN			I	Timer 1 brake input signal
WKUP2			I	MCU enters PD mode and awakens the input signal 2
ADC_IN2			Analog	ADC input channel 2
OPAMP_VINM			Analog	Operational amplifier input negative
PA3	17	23	IO	MCU port PA 3
USART1_RX			I	RxD of USART 1
USART2_RX			I	RxD of USART 2
TIM8_CH4			IO	Timer8 I/O input channel 4
TIM1_CH2			IO	Timer1 I/O input channel 2
SPI1_MISO			IO	SPI1 Master input / slave output signal
I2S_MCLK			O	I2S main clock signal
LPUART_RX			I	RxD of LPUART
COMP_INP			Analog	Comparator positive input port
ADC_IN3			Analog	ADC input channel 3
PA4	18	24	IO	MCU port PA 4
SPI1_MISO			IO	SPI 1 Master input / slave output signal
I2S_MCLK			O	I2S main clock signal
USART1_CK			O	USART 1 synchronously clock output signal
USART2_CK			O	USART 2 synchronously clock output signal
TIM3_CH1			IO	Timer 3 I/O channel 1
TIM1_CH1			IO	Timer 1 I/O channel 1
SPI1_NSS			IO	SPI 1 chip selected signal
I2S_WS			IO	I2S channel selected signal
I2C1_SCL			O	I2C1 serial clock signal
TIM8_ETR			I	Timer 8 external trigger input signal
LPUART_TX			O	TxD of LPUART
COMP_INM			Analog	Comparator negative input port
ADC_IN4			Analog	ADC input channel 4
OPAMP_VINP			Analog	Operational amplifier input positive
PA6	19	25	IO	MCU port PA 6
SPI1_MISO			IO	SPI 1 Master input / slave output signal

TIM3_CH1			IO	Timer 3 I/O channel 1
TIM1_BKIN			I	Timer1 break input signal
TIM8_CH1			IO	Timer 8 I/O channel 1
EVENT_OUT			O	Event output
LPUART_CTS			I	Clearing signal is received in flow control of LPUART
LPUART_TX			O	TxD of LPUART
I2C2_SCL			O	I2C2 serial clock signal
LPTIM_ETR			I	LP Timer external trigger input
BEEPER_OUT			O	Beeper output
COMP_OUT			Analog	Comparator output port
ADC_IN6			Analog	ADC input channel 6
OPAMP_VOUT			Analog	Operation amplifier output
PA7	-	26	IO	MCU port PA 7
SPI1_MOSI			IO	SPI1 Master output / slave input signal
SPI2_NSS			IO	SPI 2 selected signal
I2S_SD			IO	I2S serial data signal
TIM3_CH2			IO	Timer 3 I/O channel 2
TIM1_CH1N			O	Timer 1 channel 1 reverse output
TIM8_CH2			IO	Timer 8 I/O channel 2
EVENTOUT			O	Event output
LPUART_RX			I	RxD of LPUART
I2C2_SDA			IO	I2C2 serial data signal
BEEPER_N_OUT			O	Beeper output
USART2_CTS			I	Clearing signal of USART 2 flow control
ADC_IN7			Analog	ADC input channel 7
OPAMP_VINP			Analog	Positive operational amplifier input
COMP_INP			Analog	Positive input port of comparator
PB12	-	27	IO	MCU port PB12
SPI1_NSS			IO	SPI1 selected signal
I2S_WS			IO	I2S sound channel selected signal
SPI2_NSS			IO	SPI2 selected signal
TIM1_BKIN			I	Timer 1 brake input signal
EVENTOUT			O	Event output
TIM8_CH1			IO	Timer 8 I/O channel 1
MCU-GND	20	-	Analog	MCU GND
MCU_VDD	21	-	Analog	MCU positive digital power supply (includes VDDD)
PB13	22	28	IO	MCU port PB13
SPI1_SCK			IO	SPI 1 clock signal
I2S_CLK			IO	I2S serial clock signal
SPI2_SCK			IO	SPI2 clock signal
I2C2_SCL			O	I2C2 serial clock signal
TIM1_CH1N			O	Reverse output of Timer 1 channel 1
LPUART_CTS			I	Clearing signal is received in flow control of LPUART

TIM8_CH2			IO	Timer 8 I/O channel 2
PB14	23	29	IO	MCU port PB14
SPI1_MISO			IO	SPI 1 master input/ slave output signal
SPI2_MISO			IO	SPI 2 master input/ slave output signal
I2C2_SDA			IO	I2C2 serial data signal
TIM1_CH2N			O	Reverse output of Timer 1 channel 2
TIM8_CH3			IO	Timer 8 I/O channel 3
LPUART_RTS			O	LPUAR flow control transmitting query signal
OPAMP_VINP			Analog	Operation amplifier input positive
PB15	24	30	IO	MCU port PB15
SPI1_MOSI			IO	SPI 1 master output/ slave input signal
SPI2_MOSI			IO	SPI 2 master output/ slave input signal
I2S_SD			IO	I2S serial data signal
TIM1_CH3N			O	Reverse output of Timer 1 channel 3
TIM8_CH3N			O	Reverse output of Timer 8 channel 3
TIM8_CH4			IO	Timer 8 I/O channel 4
RTC_REFIN			I	RTC reference clock input (50Hz or 60Hz)
PA8	25	31	IO	MCU port PA 8
USART1_CK			O	USART 1 synchronous clock output signal
TIM1_CH1			IO	Timer 1 I/O channel 1
EVENT_OUT			O	Event output
MCO			O	Clock output signal
SPI2_NSS			IO	SPI 2 chip selected signal
TIM8_CH2N			O	Reverse output of Timer 8 channel 2
PA9	26	32	IO	MCU port PA 9
USART1_TX			O	TxD of USART 1
TIM1_CH2			IO	Timer 1 I/O channel 2
TIM8_BKIN			I	Timer 8 break input signal
I2C1_SCL			O	I2C1 serial clock signal
I2C2_SCL			O	I2C2 serial clock signal
SPI2_SCK			IO	SPI 2 clock signal
TIM8_CH1N			O	Reverse output of Timer 8 channel 1
LPTIM_OUT			O	LP Timer output signal
USART2_TX			O	TxD of USART 2
MCO			O	Clock output signal
PA10	27	33	IO	MCU port PA10
USART1_RX			I	RxD of USART1
TIM1_CH3			IO	Timer 1 I/O channel 3
TIM8_BKIN			I	Timer 8 break input signal
I2C1_SDA			IO	I2C1 serial clock signal
I2C2_SDA			IO	I2C2 serial clock signal
SPI2_MISO			IO	SPI 2 master input /slave output signal
USART2_RX			I	RxD of USART 2

RTC_REFIN			I	RTC reference clock input (50 Hz or 60 Hz)
PA11	28	34	IO	MCU port PA11
USART1_CTS			I	Clearing signal is received in flow control of USART1
TIM1_CH4			IO	Timer1 I/O channel 4
EVENT_OUT			O	Event output
I2C2_SCL			O	I2C2 serial clock signal
SPI2_MOSI			IO	SPI 2 master output /slave input signal
COMP_OUT			Analog	Comparator output port
PA12	29	35	IO	MCU port PA12
USART1_RTS			O	USART 1 flow control transmitting query signal
TIM1_ETR			I	Timer 1 external trigger input signal
EVENT_OUT			O	Event output
I2C2_SDA			IO	I2C2 serial data signal
SPI2_MISO			IO	SPI2 master output /slave input signal
COMP_OUT			Analog	Comparator output port
PA13	30	36	IO	MCU port PA13
USART1_TX			O	TxD of USART 1
USART1_RX			I	RxD of USART 1
USART2_RX			I	RxD of USART 2
I2C1_SDA			IO	I2C1 serial data signal
SPI1_SCK			IO	SPI1 clock signal
I2S_CLK			IO	I2S serial clock signal
SWDIO			IO	SWD debug interface for serial data signal
PA14	31	37	IO	MCU port PA 14
USART1_TX			O	TxD of USART 1
USART2_TX			O	TxD of USART 2
I2C1_SMBA			I	I2C1 warning signal in SM Bus mode (optional)
SPI1_MISO			IO	SPI 1 master input /slave output signal
SWCLK			O	SWD debug interface for serial clock signal
PA15	-	38	IO	MCU port PA15
SPI1_NSS			IO	SPI1 selected signal
I2S_WS			IO	I2S sound channel selection signal
USART1_RX			I	RxD of USART 1
USART2_RX			I	RxD of USART 2
LPUART_RTS			O	Flow control query signal of LPUAR
EVENTOUT			O	Event output
RF_SCLK	32[3]	39[3]	I	RF SPI clock
PB3			IO	MCU port PB3
SPI1_SCK			IO	SPI 1 clock signal
I2S_CLK			IO	I2S serial clock signal
EVENT_OUT			O	Event output
LPUART_TX			O	TxD of LPUART

TIM3_ETR			I	Timer 3 external trigger input signal
RF_SDA	33[3]	40[3]	IO	RFSPI data I/O, external requires10 kΩ pull-up resistance or MCU port configuration internal pull-up
PB4			IO	MCU port PB 4
SPI1_MISO			IO	SPI1 master input /slave output signal
TIM3_CH1			IO	Timer 3 I/O channel 1
EVENT_OUT			O	Event output
TIM8_BKIN			I	Timer 8 break input signal
LPUART_RX			I	RxD of LPUART
LPTIM_OUT			O	LP Timer output signal
RF_CSB	34[3]	41[3]	I	RF SPI access register selection
PB6			IO	MCU port PB 6
I2C1_SCL			O	I2C1 serial clock signal
USART1_TX			O	TxD of USART1
TIM8_CH1N			O	Reverse output of Timer 8 channel 1
TIM8_CH3			IO	Timer8 I/O channel 3
LPTIM_ETR			I	LP Timer external trigger signal
RF_FCSB	35[3]	42[3]	I	RF SPI access FIFO selection
PB7			IO	MCU port PB7
I2C1_SDA			IO	I2C1 serial data signal
USART1_RX			I	RxD of USART1
TIM8_CH2N			O	Reverse output of Timer 8 channel 2
LPUART_CTS			I	Clearing signal is received in flow control of LPUART
LPUART_RX			I	RxD of LPUART
LPTIM_IN2			I	LP Timer input signal channel 2
TIM8_CH4			IO	Timer8 I/O channel 4
BOOT0	-	43		Boot memory selection
PB8	-	44	IO	MCU port PB13
I2C1_SCL			O	I2C1 serial clock signal
TIM8_CH1			IO	Timer8 I/O channel 1
NC	36	-	-	No connection
XI	37	45	I	26 MHz crystal circuit input
XO	38	46	O	26 MHz crystal circuit output
GPIO2	39[2]	47[2]	IO	RFmodule GPIO 2, configuredas ： INT 1，INT 2，DOUT/DIN，DCLK(TX/RX), RF_SWT
GPIO1	40[2]	48[2]	IO	RF module GPIO 1, configuredas ： DOUT/DIN，INT 1，INT 2，DCLK (TX/RX), RF_SWT

Notes：

[1]. INT1 and INT2 are RF interrupts; DOUT is demodulation data output; DIN is the modulation data input; DCLK is a modulation or demodulation data rate synchronization clock that can automatically switches whenever TX/RX mode.

[2]. GPIO0, GPIO1, and GPIO2 of RF module are not connected to MCU ports. Users need to select suitable MCU ports for off-chip connection according to the requirements of the system scheme (that is, connecting on PCB board);

[3]. The SPI of RF module (RF_FCSB, RF_CSB, RF_SDA, RF_SCLK) is connected to MCU ports (PB7, PB6, PB4, PB3). It is recommended that users do not reuse these four ports and only operate as SPI of RF. If the reuse of these MCU ports is considered, the impacts of SPI ports of RF modules should be considered and analyzed in combination with actual scenarios.

3 Chip Frame

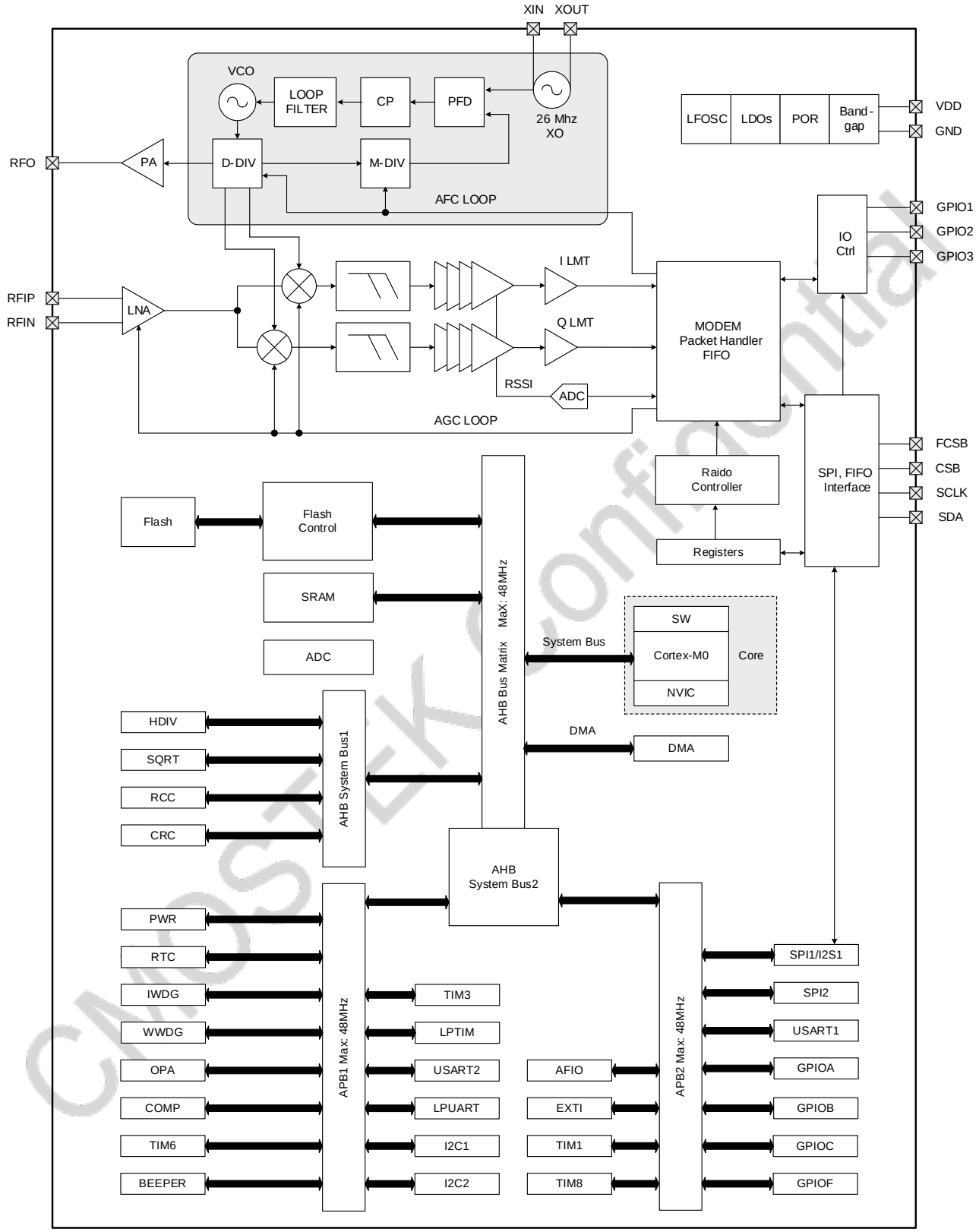


Figure 3-1. Functional Block Diagram

CMT2380F64 is an integrated Sub-G high-performance wireless transceiver single chip. The internal system block diagram of CMT2380F64 is shown in the above figure 3-1.

- **Low power high performance Sub-G transceiver**

Sub-G wireless transceiver supports 127 to 1020 MHz, OOK, (G)FSK,(G)MSK and other modulation modes, low power consumption, high performance, suitable for all kinds of wireless communication applications. The product belongs to CMOSTEK Next GenRFTM series, which includes transmitters, receivers and transceivers and other complete product series.

- **ARM Cortex-M0 high performance 32e bit micro-processor**

The CMT2380F64 controller uses a 32-bit ARM Cortex®-M0 kernel, with a maximum operating frequency of 48MHz, up to 64 KB encrypted Flash memory integrated, and a maximum of 8KB SRAM. Built-in a high-speed AHB bus, two low-speed peripherals APB and bus matrix, support up to 23 general I/O, provide a wealth of high-performance analog interface, including a 12-bit 1Msps ADC, Supports up to 12 external input channels, 1 independent operational amplifier, 1 high-speed comparator, and provides a variety of digital communication interfaces, including 3 U(S)ART, 2 I2C, 2 SPI, and 1 I2S.

CMT2380F64 resources are shown as the following table.

Table 3-1. CMT 2380F64 External Resources Table

Project Name		CMT2380F64 External Resources	Notes
Flash capacitance(KB)		64	
SRAM capacitance(KB)		8	
CPU kernal and frequency		ARMCortex-M0 @ 48MHz	
Operating environment		1.8~3.6V / -40~+85℃	
Timer	General	3	
	High level	16 interrupt source, 4 level priority	
	Basic	Enhance serial port	
	LPTIM	Support	
	RTC	Support	
Communication interface	SPI	Support	
	I2S	Support	
	I2C	Support	
	USART	Support	
	LPUART	17	
GPIO		23	4 of them are connected to the RF of SPI
DMA		5 channel	
12 bit ADC		6-ch	1Msps
OPA/ COMP		1 / 1	
Beeper		1	TWI&STWI
Algorithmic support		CRC16 / CRC32	
Security protect		Read/write protect (RDP / WRP), Storage encryption	

4 Sub-G Transceiver

4.1 Transmitter

The transmitter is based on direct frequency synthesis technology. The carrier is generated by a low noise fractional-N frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via registers, step by step from -20 dBm to +20 dBm with 1 dB.

When the PA is switched fast, the varying input impedance will disturb the output frequency of the VCO instantaneously. The effect is called VCO pulling. It will generate the spurious and spurson the spectrum around the desired carrier. The PA spurs can be reduced to a minimum instantaneously by the PA output power ramping. CMT2380F64 has a built-in PA ramping mechanism. When the PA Ramp is turned on, the PA output power can ramp the desired amplitude in a pre-configuredrate, so as to reduce the spurs. In FSK mode, the signal can be filtered by a Gaussian Filter before transmitted, e.g. GFSK, which can reduce the spectral width and interference with neighboring channels.

According to different application requirements, the user can design a Pa matching network to optimize the transmitting efficiency.
The typical application schematic and the required BOM is shown in Chapter 3 "Typical application schematic". For more schematic details and layout guidelines, please refer to *"AN141 CMT2380F64 Schematic and PCB Layout Design Guideline".*

The transmitter can operate in directmode and packagemode. In the direct mode, the data to betransmitted can besent to thechip by the DIN pinand transmitted directly. In the package mode, the data can be pre-loaded into theTX FIFO in STBY state, and transmitted together with other package elements.

4.2 Receiver

CMT2380F64 has a built-in ultra-low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation is done by the digital demodulator. The AGC loop adjust the system gain by the broad band power detector and attenuation network nearby LNA, so as to obtain the best system linearity,selectivity, sensitivity and other performance.

Leveraging CMOSTEK's low power design technology, the receiver consumes only a very low power when it is turned on.The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

Similar to the transmitter, the CMT2380F64 receiver can operate in direct mode and packet mode. In the direct mode,the demodulator output data can be directly output through the DOUT pin of the chip.DOUT can be assigned to GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet handler, get decoded and is filled in the FIFO. MCU can read the FIFO by the SPI interface.

4.3 Power-on Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2380F64 system. After the POR, the MCU must go through the initialization process and re-configure the CMT2380F64. There are two circumstances which will lead to the generation of POR.
The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9V +/-20% (e.g.0.72V–1.08V) within 2us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD as shown in the below figure.

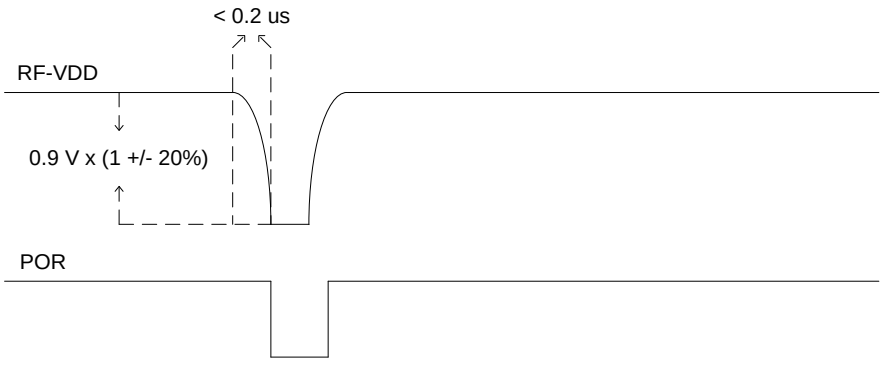


Figure 4-1. POR Reset Causing from Sudden Decreasing

The second case is,a slow decrease of the VDD. The POR triggering conditionis, RF-VDD decreases to 1.45 V+/-20% (e.g.1.16 V–1.74 V) within no less than 2us. To be noticed, it detects absolute value of RF-VDD rather than decreasing amplitude. This situation is shown as below:

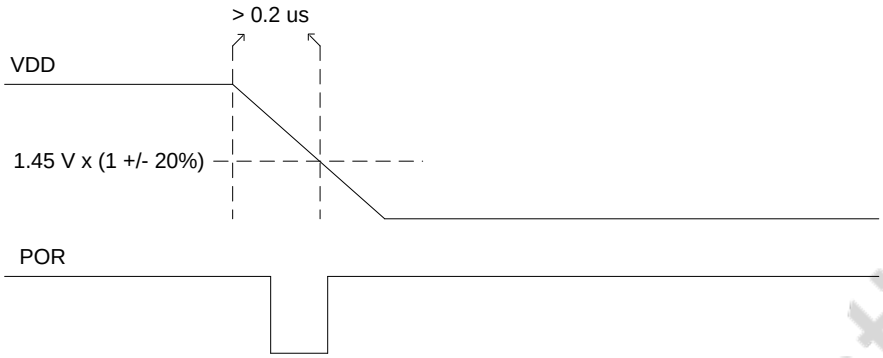


Figure 4-2. POR Reset Causing from Slow Decreasing

4.4 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CLto make the crystal accurately oscillate at 26 MHz.

$$C_L = \frac{1}{1/C15 + 1/C16} + C_{par} + 2.5pF$$

C15 and C16 are the load capacitances at both ends of the crystal. Cpar is the parasitic capacitance on the PCB. Each crystal pin has 5pF internal parasitic capacitance, together is equivalent to 2.5pF. The equivalent series resistance of the crystal must be within the specifications so that the crystal can have a reliable vibration. Also, an external signal source can be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300mV to 700mV. The clock is coupled to XI pin via a blocking capacitor.

4.5 Low power frequency oscillator (LPOSC)

The CMT2380F64 rf system integrates a sleep timer driven by a 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer periodically wakes the chip from sleep. When the chip is operating in periodic operation mode, the sleep time can be configured from 0.03125 ms to 41,922,560 ms Since the frequency of the low power oscillator will drift with temperature and voltage changes, it will be automatically calibrated during the power-up phase and will be periodically calibrated. These calibration will keep the frequency tolerance of the oscillator within 1%

4.6 Internal Low Power Detection

The chip sets up low voltage detection. When the chip is tuned to a certain frequency, the test is performed once. Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The result can be read by the LBD_VALUE register.

4.7 Received Signal Strength Indicator (RSSI)

RSSI is used to evaluate the signal strength inside the channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The logarithmic amplifier of I channels and Q channel contains the received signal indicator, in which the DC voltage is generated is proportional to the input signal strength. The output of RSSI is the sum of the values of the two channels' signals. The output has 80 dB dynamic range above the sensitivity. After the RSSI output is sampled by the ADC and filtered by a SAR filter and an average filter. The order of the average filter can be set by RSSI_AVG_MODE<2:0>. The code value

is translated into dBm value after filtering.Users can read the register RSSI_CODE<7:0> to obtain the RSSI code value,or RSSI_DBM<7:0> to obtain the dBm value. By setting the register RSSI_DET_SEL<1:0> Users can determine whetherthe RSSI is output to the MCU in real time,or latched at the instance when the preamble,sync,or the whole packet is received.

Also,CMT2380F64 allows the user to setup a threshold by RSSI_TRIG_TH<7:0> to compare with the real-time RSSI value. If the RSSI is larger than the threshold it outputs logic1, otherwise outputs logic 0. The output can be used as a source of the RSSIVLD interrupt of the receive time extending condition in the super-low power (SLP)mode.

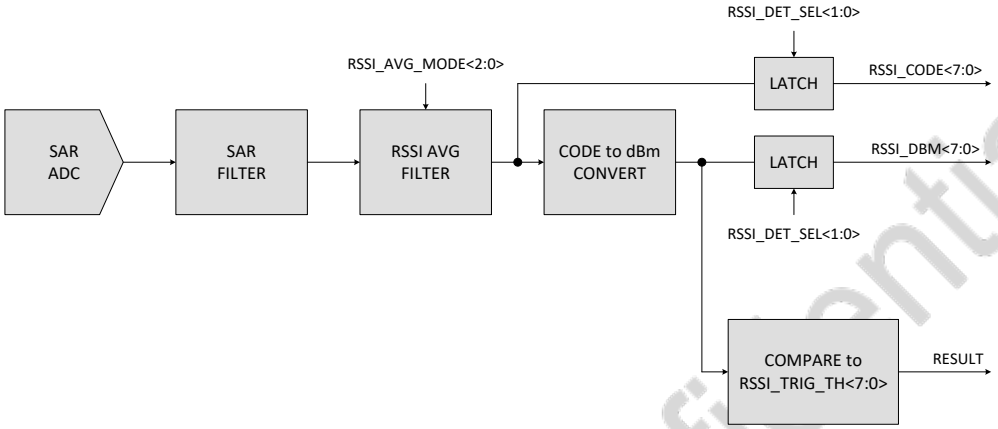


Figure 4-3. RSSI detection and comparison circuit

CMT2380F64 has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, the user needs to recalibrate the RSSI circuit in their dedicated applications. For further information, please refer to the *AN144-CMT2300A RSSI Usage Guideline.*

4.8 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in FSK demodulation, it can automatically observe the phase jump characteristics of the received signal to determine whether it is awanted signal or an unwanted noise.

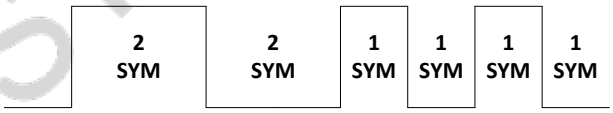


Figure 4-4. Received signal jump diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD_WIN_SEL<1:0> to determine the number of detected jumps for the PJD to identify a wanted signal. As shown in the above figure, in total 8 symbols are received. But the phase jump only appeared 6 times. Therefore, the number of jumps is not equal to the number of symbols. Only when a preamble is received they are equal. In general, the more jumps are used to identify the signal, the more reliable the result is; the less jumps are used, the faster the result is obtained. If the RX timeis set to are latively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, e.g.the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa will not treat a wanted signal as noise.

Detecting the phase jump of a signal, is identical to detect whether the signal is the expected data rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is valid, as well as to see if the SNR is over 7 dB. According to detect result of the data rate and the Deviation as well as SNR, if it is detected as a reliable signal, it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in thesuper low power (SLP)mode. In direct data mode, by setting the DOUT_MUTE register bit to 1, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, but more reliable. While users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.9 Clock Data Recovery（CDR）

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate, while receiving the data. Not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data. So CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.

CMT2380F64 has designed three types of CDR systems, as followed:

- **COUNTING system** – The system is designed for the symbol rates to be more accurate. If the symbol rate is100% aligned, the unlimited length of 0 can be received continuously without error.
- **TRACING system** – The system is designed to correct the symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted byTX, and adjust quickly the local symbol rate of RX at the sametime, so as to minimize the error between them. The system can withstand up to 15.6% symbol rate error. Other similar products in the industry cannot reach this level.
- **MANCHESTER system**–This system evolves from the COUNTING system. The basic feature is the same. The only difference is that the system is specially designed for Manchester codec. Special processing can be done when the TX symbol rate has unexpected changes

4.10 Fast Frequncy Hopping

The mechanism of fast frequency hopping is, based on the frequency configured on the RFPDFK, for instance 433.92 MHz, during applications the MCU can simply change 1 or 2 registers to quickly switch to another frequency points. This simplify theway of change the RX or TX frequency in multiple channels application.

$$\mathbf{FREQ = Base\ Freq + 2.5\ kHz \times FH\_OFFSET<7:0> \times FH\_CHANNEL<7:0>}$$

In general, users can configure FH_OFFSET<7:0>during the chip initialization process. And then in the application, users can switch the channel by changing FH_CHANNEL<7:0>.

When users need to use the fast frequency hopping in the RX mode, in some particular frequency points, one parameter of theAFC circuit must be re-configured. Please refer to *AN197-CMT2300A-CMT2119B-CMT2219B fast frequency hopping* and *CMT2300A-CMT2219B frequency hopping calculation tool* for more details.

4.11 Chip Operation

4.11.1 SPI Interface

The chip communicates with the outside through the 4-wire SPI interface (FCSB、CSB 、SDA、SCLK).The CSB is the active-low chip select signal for accessing to the registers. The FCSB is the active-low select signal for accessing to the FIFO.They cannot be set to low at the same time. The SCLK is the serial clock. Its highest speed is 5MHz.The chip itself and the external MCU send the data at the falling edge of SCLK and capture the data at the rising edge of SCLK. The SDIO is a bidirectional pin for input and output data. The address and data are transferred starting from the MSB.

When accessing to the register, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down the CSB, it must wait for at least half a SCLK cycle, and then send the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pull the CSB high.

To be noticed, when reading a register, both of the controller and the transceiver will switch the IO (SDA) port between address 0 and data 7. In this case, the SDA switches the I/O port from input to output, and the controller switches the corresponding I/O port from output to input. Note the dotted line in the middle. It is strongly recommended that the controller switch the I/O port to input before sending out the falling edge of the SCLK. The transceiver does not switch the IO to output until it sees the falling edge. This avoids the electrical conflict caused by both setting SDA as output.

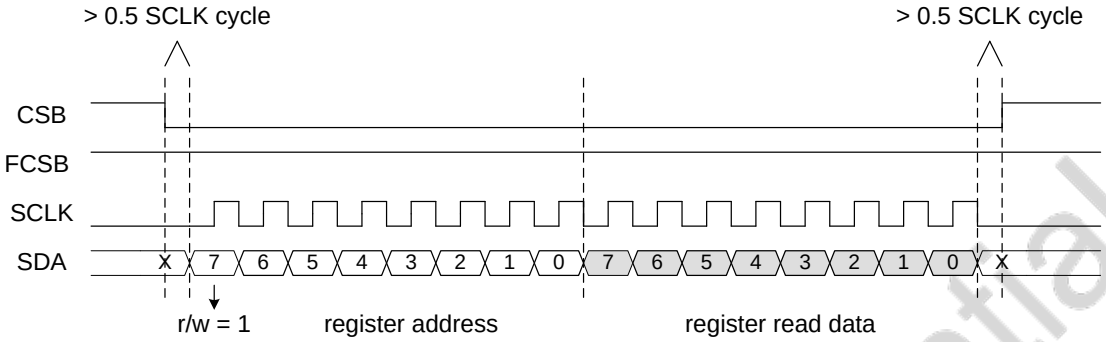


Figure 4-5. SPI read register timing

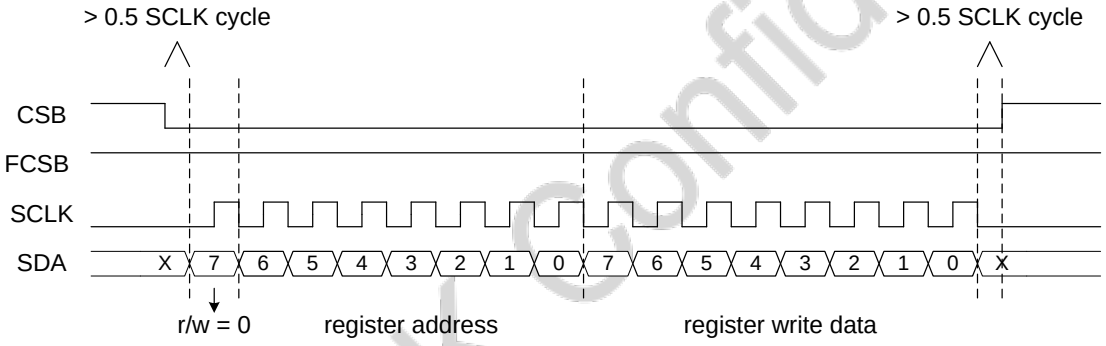


Figure 4-6. SPI write register timing

4.11.2 FIFO Interface

CMT2380F64 provides two separated 32-byte FIFO by defaul for RX and TX respectively. RX FIFO is used to store the received data in RX mode and TX FIFO is used to store the transmitting data in TX mode. Users can also set FIFO_MARGE_EN to1 to merge the two separated FIFO into one 64-byte FIFO. It can be used both underTX and RX. By configuring the FIFO_RX_TX_SEL to indicate whether it is currently used as TX FIFO or RX FIFO. When the two FIFO are not merged, users can fill in the next time 32 byte TX FIFO while the 32 byte RX FIFO is filled in the RX mode to save operation time.

The FIFO can be accessed via the SPI interface. The user can clear the FIFO by setting FIFO_CLR_TX or FIFO_CLR_RX to 1. Also, the user can re-send the old data in the TX FIFO by setting FIFO_RESTORE to 1, without the need of re-filling the data.

When the MCU accesses to the FIFO, the user must first configure a few registers to set up the FIFO read/write mode, as well as some other working mode. The details are introduced in *"AN143-CMTT2380F64 FIFO and Data Packet Usage Guideline"*. Here is the read-write timing diagram. Note that there is a slight difference in the control of the FCSB for accessing to the FIFO and the control of the CSB for accessing to the register. When the MCU starts to access to the FIFO, FCSB must be pulled down 1-clock cycle at first, and then send the rising edge of SCL. After the last falling edge of SCL is sent, the MCU must wait at least 2 us to pull up the FCSB. Between the adjacent read/write operations, the FCSB must be pulled high for 4us at least. When writing the FIFO, the first bit data must be ready 0.5 clock cycles before sending the first rising edge of SCL.

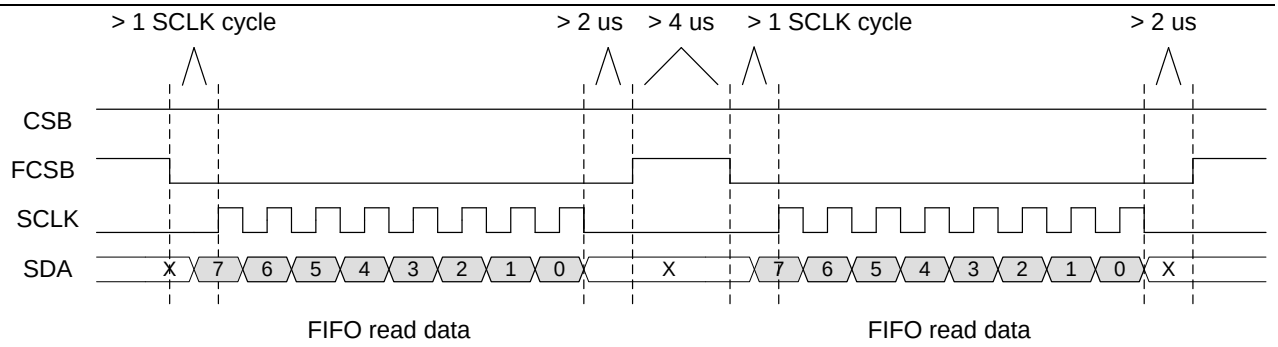


Figure 4-7. SPI read FIFO timing

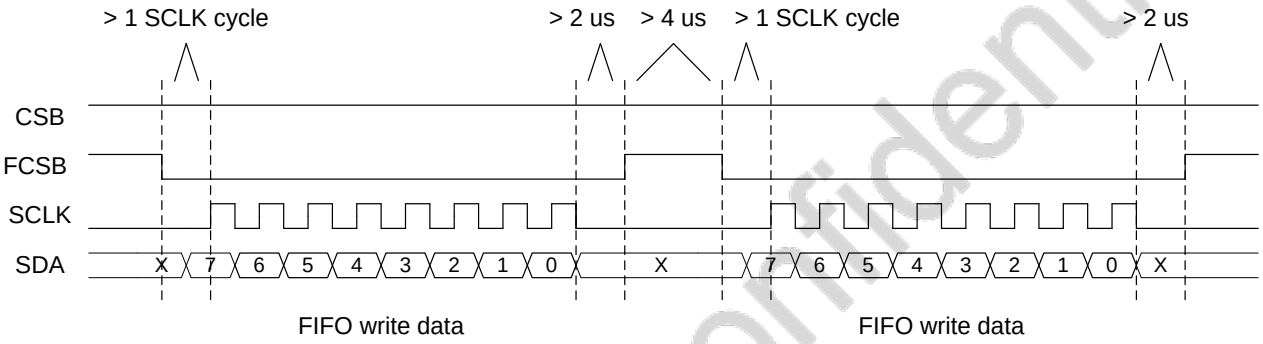


Figure 4-8. SPI write FIFO timing

Transceivers provide a wealth of FIFO related interrupt sources as auxiliary means for efficient chip operation. The FIFO interrupt timing sequence related to Rx and Tx is shown in the figure below.

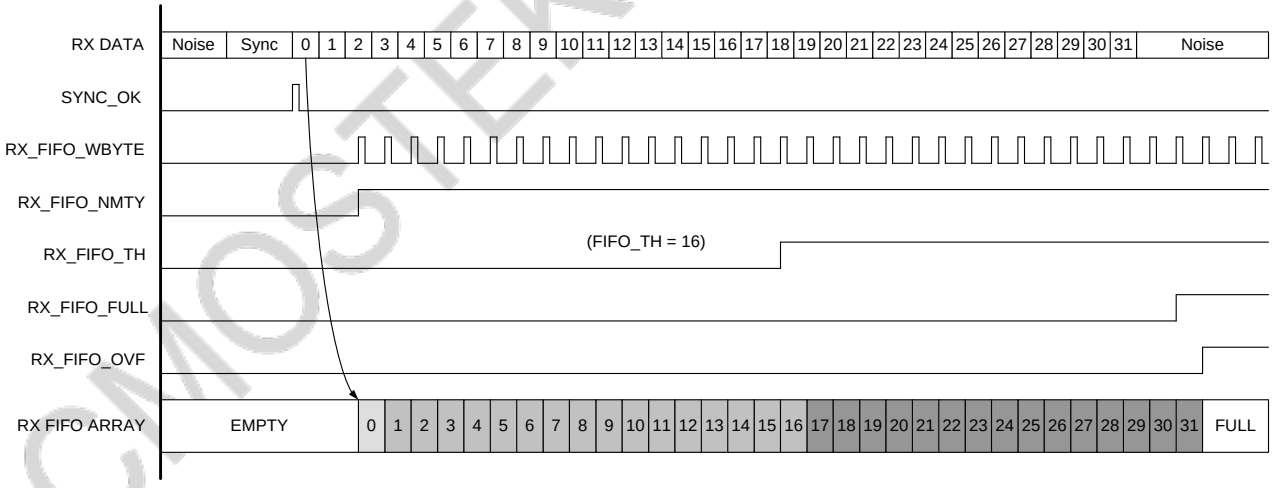


Figure 4-9. Transceiver RX FIFO Interrupt Sequence Diagram

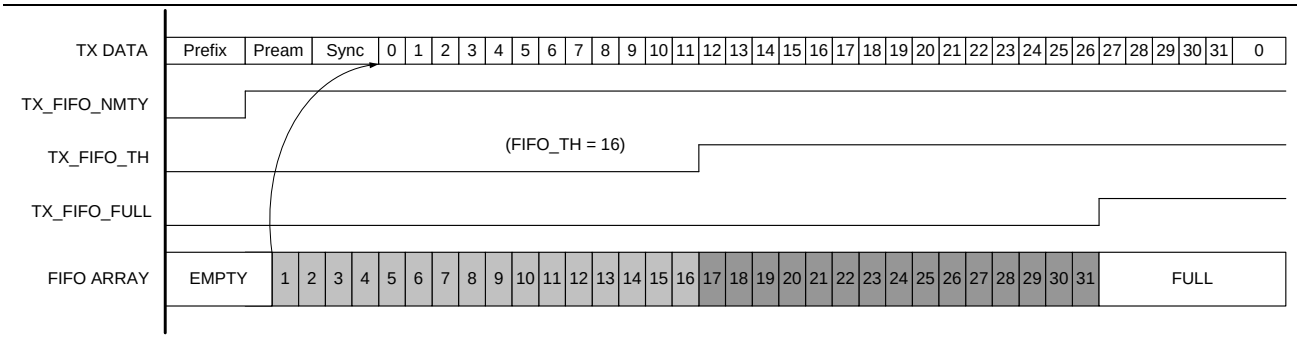


Figure 4-9. Transceiver TX FIFO Interrupt Sequence Diagram

4.11.3 Transceiver working status, timing and power consumption

- Startup time

After the transceiver is powered on RF-VDD, it usually needs to wait for about 1ms until POR released. After the RELEASE of POR, the crystal will also start. The startup time is assumed to be N ms, which depends on the characteristics of the crystal itself. After startup, it is necessary to wait for the crystal to stabilize the system before starting to work. The default stability time is 2.48 ms, which can be written to XTAL_STB_TIME <2:0>; After modification, the chip will stay in IDLE state until the crystal is stable. After the crystal is stable, the chip will leave IDLE and start to do the calibration of each module. After the calibration, the chip will stay in SLEEP, waiting for the user to initialize the chip. The chip returns to IDLE and starts the power-on process again

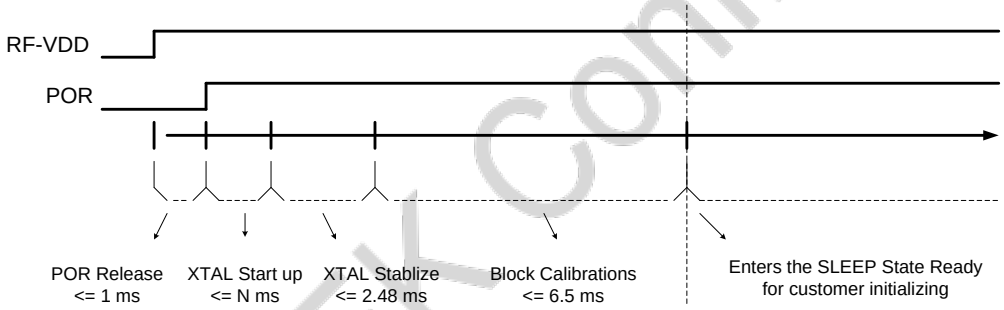


Figure 4-11. Power on timing

The chip enters SLEEP state after calibration. And then, the MCU can control the chip to switch to different operation states through setting the register CHIP_MODE_SWT<7:0>.

- Operation State

CMT2380F64 has 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown below.

：

Table 4-1.CMT 2380F64 state and corresponding active module

State	Binary code	Switch command	Active module	Optional module
IDLE	0000	soft_rst	SPI, POR	无
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
RFS	0011	go_rfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
RX	0101	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+IF, FIFO	CLKO, RX Timer
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

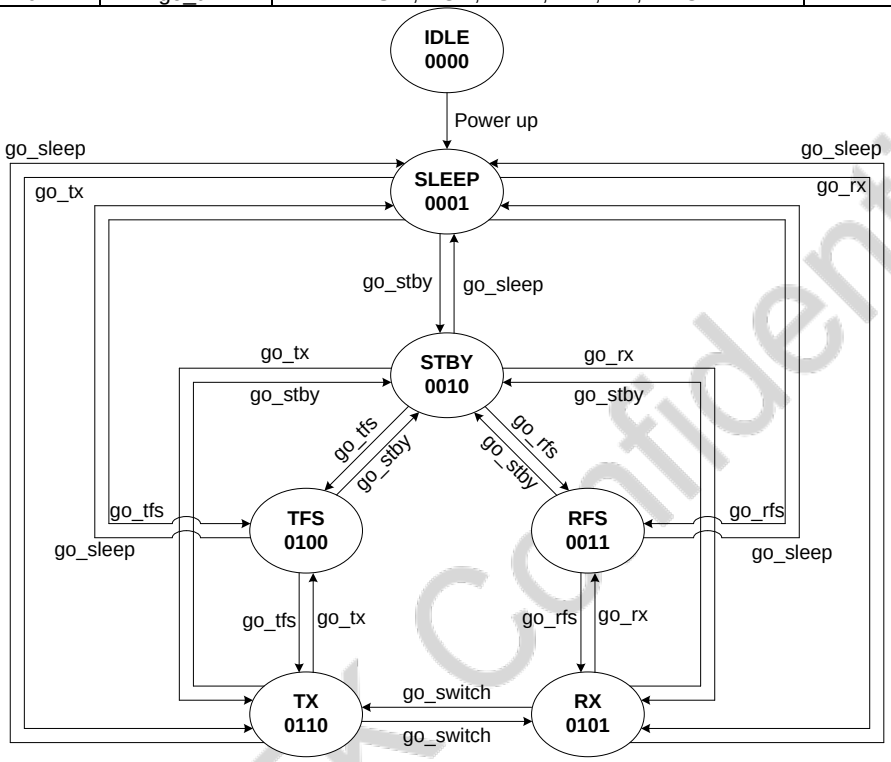


Figure 4-12. State Switch Diagram

➢ SLEEP State

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged.

However, the user cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

➢ STBY State

In STBY state, the crystal is turned on, the LDO of the digital circuit will also be turned on, the current will be slightly increased, and the FIFO can be operated. The user can choose whether to output CLKO (system clock) to PIN. Because the crystal and LDO is turned on, compared to the SLEEP, the time switching from the STBY to transmitting or receiving will be relatively short. Switching from SLEEP to STBY will be completed after the crystal is turned on and settled. Switching from other state to STBY will be completed immediately.

➢ RFS State

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the RX frequency, RFS cannot switch to TX. Switching from STBY to RFS probably requires PLL calibration and stability time of 350 us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

➢ TFS State

TFS is a transition state before switching to TX. Except that the transmitter RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the TX frequency, TFS cannot switch to RX. Switching from STBY to TFS probably requires PLL calibration and stability time of 350us. Switching from SLEEP to TFS needs to add the crystal start-up and settled time. Switching from other state to TFS will be completed immediately.

➢ RX State

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20 us. Switching from STBY to RX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to RX needs to add the crystal start-up and settled time. TX can be quickly switched to RX by sending go_switch command. Whether the TX and RX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

➢ TX State

All modules on the transmitter will be opened in TX state. Switching from TFS to TX requires only 20 us. Switching from STBY to TX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to TX needs to add the crystal start-up and settled time. RX can be quickly switched to TX by sending go_switch command. Whether the RX and TX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

4.11.4 GPIO Function and Interrupt Mapping

CMT2380F64 has 3 GPIO ports. Each GPIO can be configured as a different input or output. CMT2380F64 has 2 interrupt ports. They can be configured to different GPIO mapping output.

Table 4-2. CMT2380F64 GPIO

Pin No.	Name	I/O	Function
48	GPIO1	IO	Configurable as：DOUT/DIN，INT1，INT2，DCLK (TX/RX)，RF_SWT
47	GPIO2	IO	Configurable as：INT1，INT2，DOUT/DIN，DCLK (TX/RX)，RF_SWT
9	GPIO3	IO	Configurable as：CLKO，DOUT/DIN，INT2，DCLK (TX/RX)

Below shows the Interrupt mapping in table 4-3. INT 1 and INT 2 mapping is the same. Take INT 1 as an example.

Table 4-3. CMT 2380F64 interrupt mapping

Name	INT1_SEL	Descriptions	Clearing methods
RX_ACTIVE	00000	Indicates the chip is entering RX and already in RX. It is 1 in PLL tuning and RX state while 0 in other states.	Auto
TX_ACTIVE	00001	Indicates the chip is entering TX and already in TX. It is 1 in PLL tuning and RX state while 0 in other states.	Auto
RSSI_VLD	00010	Indicates whether the RSSI is active.	Auto
PREAM_OK	00011	Indicates that the Preamble is received successfully.	by MCU
SYNC_OK	00100	Indicates that the Sync Word is received successfully.	by MCU
NODE_OK	00101	Indicates that the Node ID is received successfully.	by MCU
CRC_OK	00110	Indicates that the CRC for the current packet is correct.	by MCU
PKT_OK	00111	Indicates that a packet has been received.	by MCU
SL_TMO	01000	Indicates that the SLEEP counter timed out.	by MCU
RX_TMO	01001	Indicates that the RX counter timed out.	by MCU
TX_DONE	01010	Indicates that the TX operation is completed.	by MCU
RX_FIFO_NMTY	01011	Indicates that the RX FIFO is not empty.	Auto
RX_FIFO_TH	01100	Indicates the number of unread bytes of the RX FIFO is over FIFO TH	Auto
RX_FIFO_FULL	01101	Indicates RX FIFO is full.	Auto
RX_FIFO_WBYTE	01110	Indicates each time a byte is written to the RX FIFO.It is a pulse.	Auto
RX_FIFO_OVF	01111	Indicates RX FIFO is overflow	Auto
TX_FIFO_NMTY	10000	Indicates that TX FIFO is not empty	Auto
TX_FIFO_TH	10001	Indicates the number of unread bytes of the TX FIFO is over FIFOTH.	Auto
TX_FIFO_FULL	10010	Indicates TX FIFO is full.	Auto
STATE_IS_STBY	10011	Indicates that the current state is STBY.	Auto
STATE_IS_FS	10100	Indicates that the current state is RFS or TFS.	Auto
STATE_IS_RX	10101	Indicates that the current state is RX.	Auto
STATE_IS_TX	10110	Indicates that the current state is TX.	Auto
LBD	10111	Indicates that low battery is detected (VDD is lower than TH)	Auto
TRX_ACTIVE	11000	Indicates the chip is entering TX or RX and is already in TX or RX. It is 1 in PLL tuning, TX or RX state while it is 0 in the otherstates.	Auto
PKT_DONE	11001	Indicates that the current packet has been received, covering 4 possible different situations. 1. The packet is received completely and correctly. 2. Manchester decoding error. Decoder is automatically reset. 3. NODE ID receiving error. Decoder is automatically reset. Signal collision occurred. Decoder is not reset, waiting for MCU to response.	by MCU

By default, interrupt is active high (logic1 is valid). Users can set the INT_POLAR register bit to 1 to make all interrupts active low (logic 0 is valid). Taking INT 1 as an example, the control and sources selection of all the available interrupts is shown below. The control and mapping of INT 1 and INT 2 are the same.

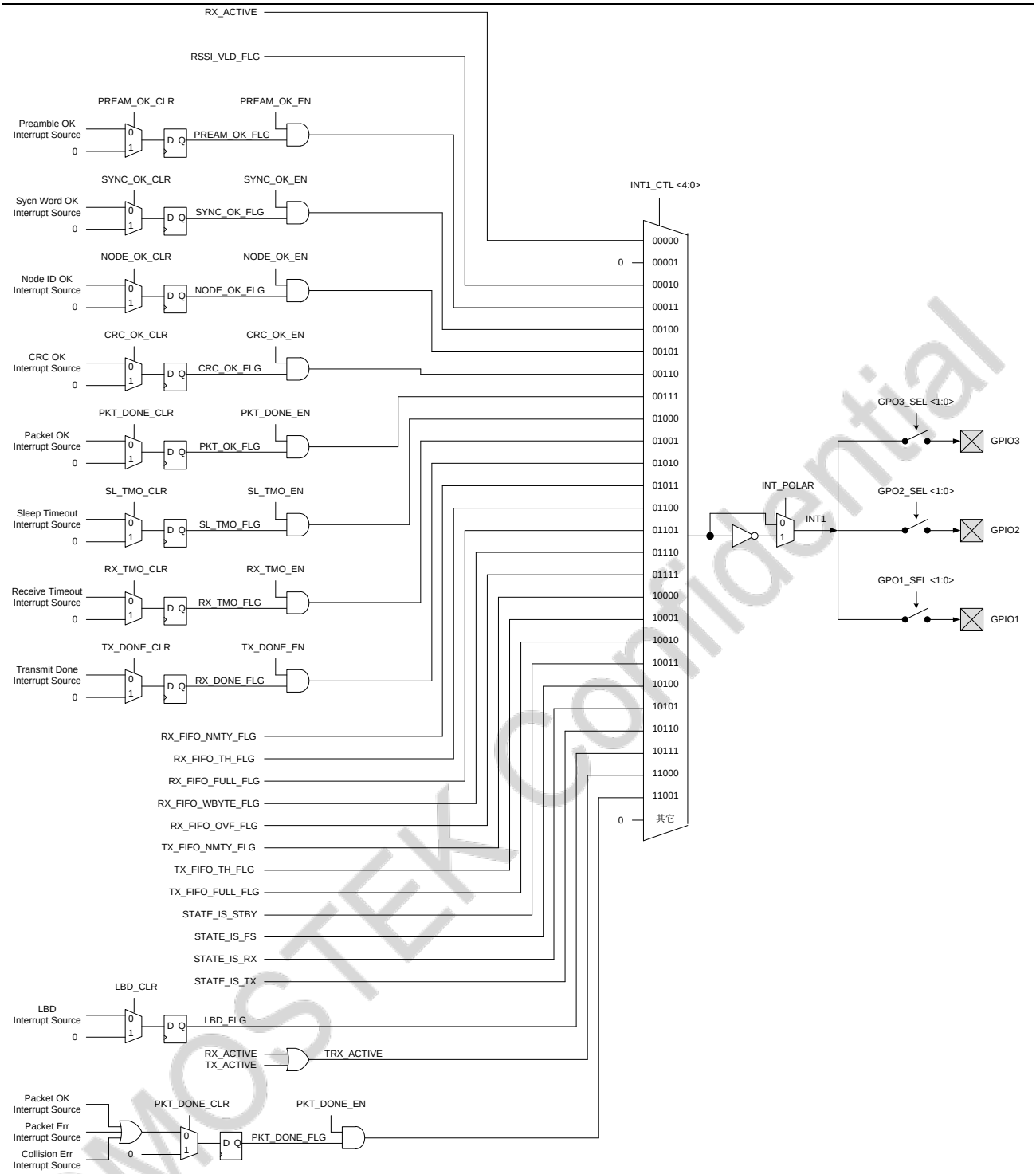


Figure 4-13. CMT2300A INT 1 Interrupt mapping

5 Function Description

5.1 Memory

CMT2380F64 include embedded encrypted flash memory (Flash) and embedded SRAM, Figure 5-1 below shows the memory address map.

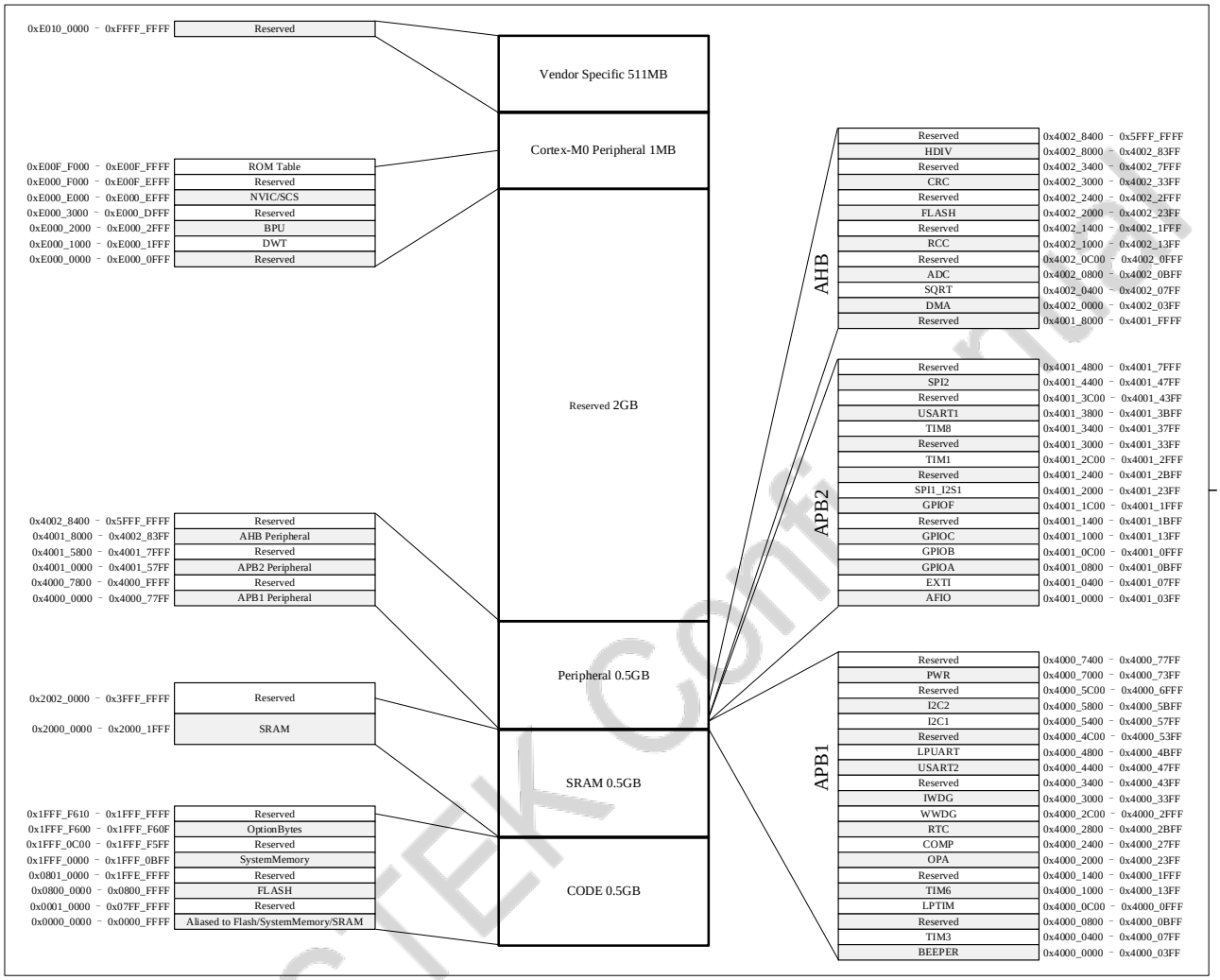


Figure 5-1. Memory address map

5.1.1 Embedded flash memory

The chip integrates 64K bytes of embedded flash memory (FLASH) for storing programs and data. The page size is 512 byte and supports page erase, word write, word read, half-word read, and byte read operations. Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operations).

5.1.2 Embedded SRAM

Up to 8K bytes of built-in SRAM is integrated on-chip, and data can be maintained in the STOP mode.

5.1.3 Nested vectored interrupt controller（NVIC）

The Nested Vectored Interrupt Controller (NVIC) is closely connected to the interface of the processor core, which can realize low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 32 maskable interrupt channels(not including 16 Cortex®-M0 interrupt lines）;
- 4 programmable priority levels (using 2-bit interrupt priority levels);
- Low-latency exception and interrupt handling;
- Power management control;
- Realization of system control register;

The module provides flexible interrupt management functions with minimal interrupt delay.

5.2 Extended interrupt/ event controller (EXTI)

The extended interrupt/event controller includes 24 edge detection circuits that generate interrupts/event triggers. Each input line can be independently configured as an event or interrupt, as well as three trigger types of rising edge, falling edge or both edges, and can also be independently shielded. The suspend register holds the interrupt request of the status line, and the corresponding bit of the suspend register can be cleared by writing '1'.

5.3 Clock System

The clock of the device includes internal high-speed RC oscillator HSI (8 MHz), internal low-speed clock LSI (30 KHz), external low-speed clock (32.768 KHz), PLL.

The system clock (SYSCLK) can choose the following clock sources:

- HIS oscillator clock
- PLL clock
- LSI oscillator clock
- LSE oscillator clock

2 secondary clock source:

- 30 Khz low-speed internal RC，which can be used as the clock source of IWDG, RTC, LPTIMER and LPUART. Used to automatically wake up the system from STOP mode.
- 32.768 KHz low-speed external crystal can be used as the clock source of RTC、LPTIMER and LPUART.
- When not in use, any clock source can be independently startup or shutdown to reduce system power consumption.

The HSI clock is selected as the default system clock during reset. When needed, it is possible to take safe interrupt management of the PLL clock (for example, when the indirect external oscillator fails).

Users can configure the frequency of AHB and APB (APB1 and APB2) domains through multiple prescalers. The maximum allowable frequency of AHB domain, APB 1 domain and APB 2 domain is 48MHz.Figure 5-2 is a clock block diagram tree.

Clock Tree

HSE = High-speed external clock signal(CMT2380F64 not support)
HIS = High-speed internal clock signal
LSE= Low-speed external clock signal
LSI = Low-speed internal clock signal

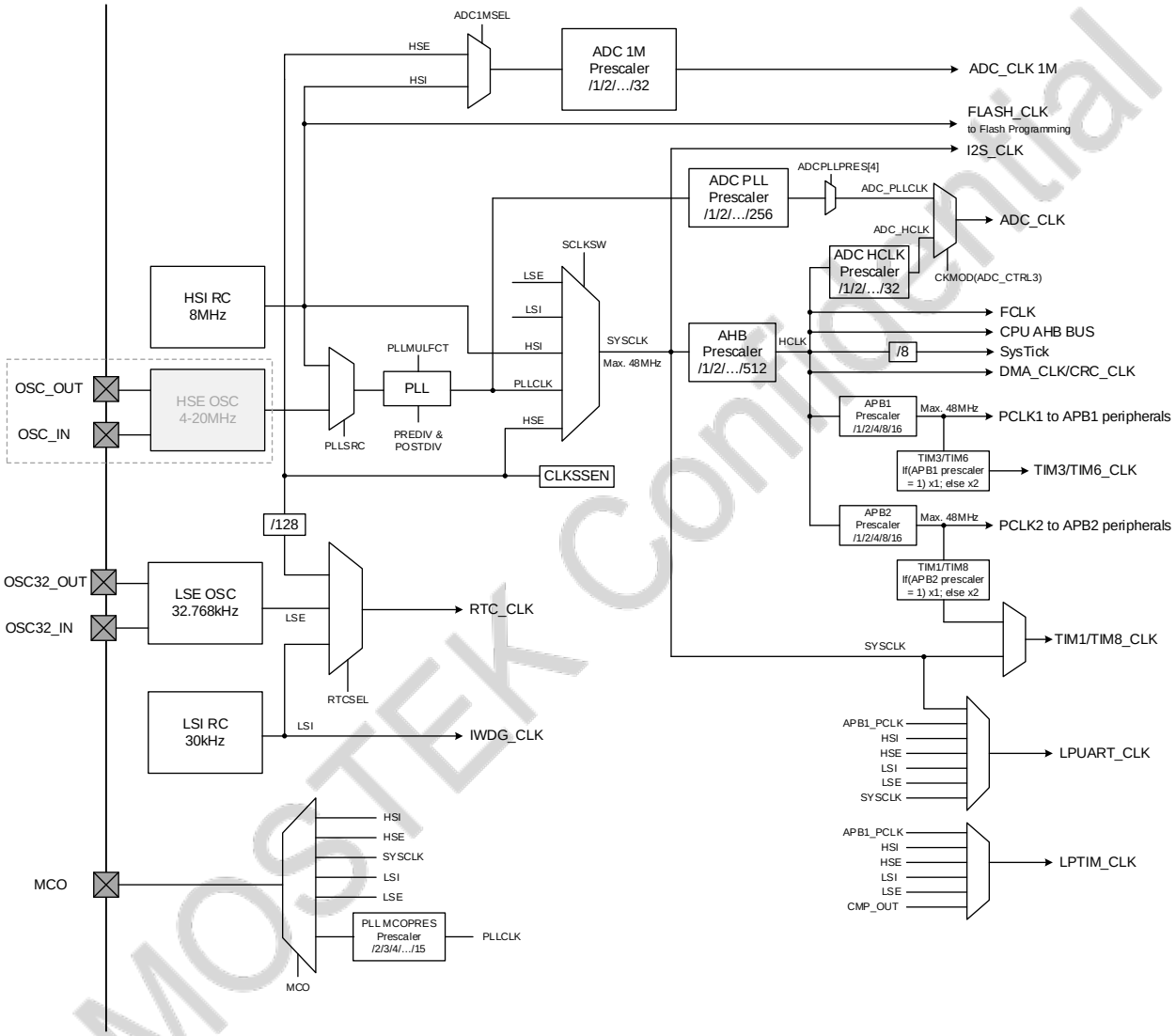


Figure 5-2. Clock Tree

5.4 Boot Modes

At startup, BOOT0 pin and Flash system configuration bits can be selected from one of the three boot options:

- Boot from FLASH Memory
- Boot from System Memory
- Boot from on-chip SRAM

The Bootloader is located in the internal system memory.

5.5 Power supply scheme

- VDD area：The voltage input range is 1.8 V~3.6 V，which mainly provides power input for Main Regulator, IO and clock reset system.

- VDDA area：The voltage input range is 1.8 V~3.6 V，which supplies power for most of the external analog peripherals. For more information, please refer to the electrical characteristics section of the relevant data manual.
- VDDD area：The voltage regulator supplies power for CPU, AHB, APB, SRAM, FLASH and most of the digital peripheral interfaces.
- PWR is the power control module of the entire device, its main function is to control CMT2380F64 to enter different power modes and can be awakened by other events or interrupts. CMT2380F64 supports RUN, LPRUN, SLEEP, STOP and PD modes.

5.6 Programmable voltage monitor

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 1.8 V. When VDD is lower than the set threshold (VPOR/PDR), the device remains in the reset state. The device has a programmable voltage monitor (PVD), which monitors the MCU_VDD/ MCU_VDDA power supply and compares it with the threshold VPVD. When VDD is lower or higher than the threshold VPVD, it will generate an interrupt. The PVD function is turned on by software.

For the values of VPOR/PDR and VPVD, please refer to the table for Embedded Reset and Power Control Module Features

5.7 Low Power Mode

CMT2380F64 is in operation mode after system reset or power-on reset. When the CPU does not need to run(for example, waiting for external events）, users can choose to enter a low-power mode to save power.

CMT2380F64 has the following four low-power modes：

- LPRUN mode（low-power operation mode，the system is in 32.768 KHz low-frequency operation mode）
- SLEEP mode（the core is stopped, all peripherals including Cortex®-M0 core peripherals (such as NVIC, SysTick are still running）
- STOP mode（most of the clocks are turned off, the voltage regulator is still running in low power consumption mode）
- PD mode（VDDD power-down mode，VDD hold，3 WAKEUP IO and NRST can be wake up）
- In addition，the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses
  - Optional configuration of PWR_CTRL4.STBFLH in RUN mode allows FLASH to enter deep standby mode; when exiting, the system needs to wait about 10 us before re-accessing FLASH

5.8 Direct Memory Access（DMA）

Integrated 1 general purpose 5-channel DMA controller to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral data transfer; Each channel has a dedicated hardware DMA request logic, and each channel can be triggered by the software. The transmission length of each channel, source address and destination address of transmission can be set separately by software.

DMA can be used for the main peripherals: SPI, I2C, USART, Universal, Basic and Advanced Control Timers TIMx, I2S, ADC.

5.9 Real Time Clock（RTC）

Real Time Clock (RTC) has a set of BCD timers/counters that count independently and continuously. Under the corresponding software configuration, it can provide calendar function. The RTC can also provides two programmable clock interrupts.

Two 32-bit registers contain decimal format (BCD) for subseconds, seconds, minutes, hours (in 12 or 24 hour format), days of the week, days (date), months, and years.

Subsecond values are provided in binary format as separate 32-bit registers. Additional 32-bit registers containprogrammable seconds, minutes, hours, days of the week, days, months, and years.

RTC provides automatic wake up in low power mode. When a timestamp function event or intrusion detection event is enabled on GPIO, the current calendar is saved in a register.

5.10 Timer and Watch Dog

CMT2380F64 supports 2 advanced-control timers, 1 general-purpose timer, 1 basic timer and 1 low-power timer, as well as 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced-control timers, general-purpose timers and basic timers:

Table 5-1. Timer function comparison

Timer	Counter resolution	Counter type	Prescaler	Generate DMA request	Capture/ Compare channel	Complementary output
TIM1 TIM8	16 bits	Up Down Up/Down	Any integer between 1~65536	support	4	support
TIM3	16 bits	Up Down Up/Down	Any integer between 1~65536	support	4	unsupport
LPTIM	16 bits	Up	2^N, N represents for any integer between 0~7	unsupport	2	unsupport
TIM6	16 bits	Up	Any integer between 1~65536	support	0	unsupport

5.10.1 Basic timer TIM6

The basic timer (TIM6) contains a 16-bit auto-load counter, driven by a programmable prescaler. It can provide a time base for general-purpose timers.

The main functions of the basic timer are as follows:

- 16 bit automatic reload accumulating counter;
- 16 bit programmable (can be modified in real time) prescaler, used to divide the input clock by coefficient between 1 and 65536;
- Interrupt / DMA request is generated when an update event (counter overflow) occurs.

5.10.2 General purpose timer TIM3

CMT2380F64 has a built-in general-purpose timer (TIM3) that can run synchronously. The timer has a 16-bit auto-loading up/down counter, a 16-bit prescaler and 4 independent channels. Each channel can be used for input capture (for measuring pulse width), output comparison, PWM and single pulse mode output.

The main functions of the general-purpose timer include:

- 16 bit up,down, up/down automatic loading counter;
- 16 bit programmable (can be modified in real time) prescaler, the frequncy division coefficient of the counter clock frequncy is any value between 1～65536;
- 4 independent channels:
  - Input capture;
  - Output comparision;
  - PWM generation (edge or center alignment mode);
  - Single pulse mode output;
- Use external signals to control the timer or the synchronization circuit when multiple timers are interconnected;
- Interrupt /DMA is generated when the following events occur:
- Update: counter overflow/downflow, counter initialization (trigger through software or internal/external);

- Trigger events(counter start, stop, initialization or count by internal/external trigger) ；
- Input capture；
- Output comparision；
- Supports incremental(quadrature) encoder and Hall sensor circuits positioning；
- Trigger input as an external clock or current management by cycle

5.10.3 Low power timer (LPTIM)

LPTIM is a 16-bit timer that can work with extremely low power consumption. Thanks to the diversity of clock sources, LPTIM can operate in all power modes except PD mode. Since LPTIM can run without an internal clock source, it can be used as a "pulse counter", which is very useful in some applications. In addition, LPTIM has the ability to wake up the system from low-power consumption mode, which makes it suitable for implementing "timeout function" monitoring with extremely low power consumption. LPTIM introduces a flexible clock scheme that provides the required functions and performance while minimizing power consumption.

The main functions of low-power timers include:

- 16 bit upward automatic loading counter；
- 3 bit prescaler, 8 kinds of frequency division factors（1、2、4、8、16、32、64、128）；
- Abundant clock source：
  - Internal clock source：HSI，HSE，LSI，LSE，APB1 and CMP_OUT six clock sources；
  - External clock source input through LPTIM（no LP oscillator runs during operation, used for pulse counter applications）；
- 16 bit ARR automatic loading register；
- 16 bit comparator register；
- Continuous or single trigger mode；
- Optional software and hardware input trigger；
- Programmable digital anti-shake filter；
- Configurable IO level polarity；
- Configurable single pulse or PWM output；
- Sopport encoder mode；

5.10.4 Adcanced control timer (TIM 1/TIM 8)

Two independent advanced timers (TIM1/TIM8), each timer is composed of a 16-bit auto-loading counter driven by a programmable prescaler. Supports multiple functions, including measuring pulse width of the input signal (input capture), or generating output waveform (output comparison, PWM, complementary PWM outputembedded in dead time, etc.). By using timer prescaler and RCC clock control prescaler, pulse width and waveform period can be adjusted from several microseconds to several milliseconds. Each timer is completelyindependent and does not share any resources with each other.

The main functions of the advanced timer include:

- 16-bit up, down, up/down automatic loading counter
- 16-bit programmable (can be modified in real time) prescaler, the frequency division coefficient of the counter clock frequency is any value between 1 and 65536
- Supports up to 48Mhz as the timer input clock
- Up to 4 independent channels :
  - Input capture
  - Output comparision
  - PWM generation (edge or center alignment mode)
  - Single pulse mode output
- PWM trigger ADC sampling
- The trigger time point can be configured by software in the entire PWM cycle
- Complementary output with programmable dead time
- Use external signals to control the timer or the synchronization circuit when multiple timers are interconnected
- Allow to update the repeat counter of the timer register after a specified number of counter cycles
- Break input signal can put the timer output signal in a reset state or a known state
- Interrupt/DMA is generated when the following events occur:
  - Update：counter overflow/downflow, counter initialization (through software or internal/ external trigger)
  - Trriger events (counter start, stop, initialization or count by internal/ external trigger)

- Input capture
- Output comparision
- Break signal input

- Supports incremental (quadrature) encoder and Hall sensor circuits for positioning
- Trigger input as an external clock or current management by cycle

In debug mode, the counter can be frozen and the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Many of the functions are the same as the standard TIM timer, and they also have the same internal structure, so the advanced control timer can operate in collaboration with the TIM timer through the timer link function to provide the synchronization or event link function.

5.10.5 Systick

This timer is specific used for real-time operating system and can also be used as a standard decrement counter.

It has the following characteristics:

- 24 bit decrement counter
- Automatic reload function
- A maskable system interrupt can be generated when the counter is 0
- Programmable clock source

5.10.6 Watchdog Timer (WDG)

Two watchdogs are supported, Independent Watchdog (IWDG) and Window Watchdog (WWDG).Two watchdogs provide increased security, timing accuracy and flexibility in use.

- **Independent watchdog（IWDG）**

The independent watchdog is based on a 12-bit decline counter and an 8-bit prescaler, driven by an independent low- speed RC oscillator that remains effective in the event of a master clock failure and operates in STOP mode. Once activated, IWDG generates a reset when the counter counts to 0x000if the dog is not fed within the set time (clearing the watchdog counter). It can be used to reset the entire system in the event of an application problem, or as a free timer to provide timeout management for the application. The option byte can be configured to be software or hardware enabled watchdog. Reset and low power wake-up are available.

- **Window watchdog（WWDG）**

Window watchdogs are usually used to monitor software failures caused by external interference or unforeseen logic conditions that cause the application to deviate from the normal operating sequence. Unless the value of the down counter is refreshed before the T6 bit becomes 0, the watchdog circuit will generate an MCU reset when the preset time period is reached. Before the down counter reaches the window register value, if the 7-bit down counter value (in the control register) is refreshed, an MCU reset will also be generated. This indicates that the down counter needs to be refreshed in a limited time window.

Main features:

- WWDG is driven by the clock after the APB 1 clock is divided;
- Progranmable free running decrement counter;
- Conditional reset;
- When the decrement counter value is less than 0x40，(if the watchdog is started) a reset is generated;
- Reset when the decrement counter is reloaded outside the window (if the watchdog is activated);
- If the watchdag is enabled and interrupts are allowed, an early wake-up interrupt (EWI) is generated when the decrements counter equals 0x40, which can be used to reload the counter to aviod a WWDG reset.

5.11 I2C Bus Interface

Two independent I2C bus interfaces that provide multi-host functionality to control all I2C bus specific timing, protocol, mediation, and timing.Supports multiple communication rate modes (up to 1MHz), supports DMA operation, and is compatible with SMBUS 2.0.The I2C module has a variety of uses, including CRC code generation and

verification, SMBUS (System Management Bus) and PMBUS (Power Management Bus).

The main functions of I2C interface are described as follows:

- Multi-host function: the module can be used as a master device or a slave device;
- I2C master device function:
  - Generate clock;
  - Generate start and stop signals;
- I2C slave device function:
  - Progranmable address detection;
  - The I2C interface supports 7 bit or 10 bit addressing and supports dual slave address response in 7 bit slave mode;
  - Stop bit detection;
- Generate and detect 7 bit /10 bit addresses and broadcast calls;
- Support diferent communication speeds:
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz)；
  - Fast + (up to 1 MHz)；
- Status flag:
  - Transmitter/ receiver mode falg;
  - Byte end flag;
  - I2C bus busy sign;
- Error flag:
  - Arbitration lost in master mode;
  - Response（ACK）error after address/data transmission;
  - Misaligned start or stop conditions detected;
  - Prohibit overflowing or underflowing when elongating the clock function;
- 2 interrupt vectors:
  - 1 interrupt for address/data communication successful;
  - 1 interrupt for error;
- Optional elongated clock feature;
- DMA with a single byte cache;
- Generate or verify configurable PEC (packet error detection):
  - The PEC value can be sent as the last byte in transmission mode
  - A PEC error check for the last received byte
- SMBus 2.0 compatible
  - Low timeout delay for 25 ms clock
  - 10 ms master device cumulative clock low expansion time
  - 25 ms slave device cumulative clock low expansion time
  - Hardware PEC generation/verification with ACK control
  - Support for address resolution protocol (ARP)
- SMBus compatible

5.12 Universal synchronous asynchronous receiver transmitter（USART）

In CMT2380F64, three serial transceiver interfaces are integrated, including two universal synchronous/asynchronous transceivers (USART1, USART2) and one universal asynchronous transceiver (LPUART) supporting low power mode operation. These three interfaces provide synchronous/asynchronous communication, support for IrDA SIR ENDEC transport codec, multi-processor communication mode, single-wire semi-duplex communication mode, and LIN master/slave functionality.

The USART 1 and USART 2 interfaces have hardware CTS and RTS signal management, ISO7816 compatible smart card mode and SPI-like communication mode, all interfaces can use DMA operation.

The main features of USART are as follows:

- Full-duplex, asynchronous communication;
- NRZ standard format;
- Fractional baud rate generator system, baud rate programmbale for sending and receiving up to 3M bits/s
- Programmbale data word length (8 or 9 bits)
- Configurable stop bits, supporting 1 or 2 stop bits

- The ability of LIN to send a synchronous break and LIN to detect a slave break. When the USART hardware is configured to LIN, the 13 bit break is generated and the 10/11 bit break is detected
- Output the sending clock for step transmission
- IRDA SIR encoder/decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function
  - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3standard；
  - 0.5 and 1.5 stop bits for smart cards；
- Single-wire half-duplex communication；
- Configurable DMA multi-buffer comminucation, receiving/sending bytes in SRAM with centralized DMA buffer
- Separate transmitter and receiver enabling bits
- Detection mark
  - Receive buffer full
  - Send bufffer empty
  - End of transmission flag
- Check control
  - Sending check bit
  - Check the received data
- Four error detection flags
  - Overflow error
  - Noise error
  - Frame error
  - Check error
- 10 USART interrupt source with flag
  - CTS change
  - LIN break character detection
  - Tx data register empty
  - Tx complete
  - Receive data register full
  - Bus detected as idle
  - Overflow error
  - Noise error
  - Frame error
  - Check error
- Multi-processor communication, if the address does not match, then into silent mode
- Wake up from silent mode (Detect by idle bus or address flag detection)
- There are two ways to wake up the receiver: address bit (MSB. 9th bit), and bus idle
- Mode configuration

USART modes	USART1	USART2	LPUART
Asynchronous mode	√	√	√
Hardware flow control	√	√	√
Multi-cache Communication (DMA)	√	√	√
Multiprocessor communication	√	√	×
Synchronous	√	√	×
Smart card	√	√	×
Half duplex (single wire mode)	√	√	×
IrDA	√	√	×
LIN	√	√	×

5.13 Serial Perigheral Interface（SPI）

Support 2 SPI interfaces, SPI allows the chip to communicate with external devices in half/full duplex, synchronous, serial mode. This interface can be configured to be in master mode and provide a communication clock (SCK) for external slave devices.The

interface can also work in a multi-master configuration.It can be used for a variety of purposes, including dual wire simplex synchronous transmission using a two-way data line, and reliable communication using CRC calibration.

The main functions of the SPI interface are as follows:

- Full-duplex synchronous transmission
- Double wire simplex synchronous transmission with or without a third two-way data line
- 8 or 16 bit transmission frame format selection
- Support master mode or slave mode
- Support multi-master mode
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master mode and slave mode: dynamic change of master/slave operation mode
- Programmable clock polarity and phase;
- Programmable data order, MSB before or LSB before;
- Dedicated send and receive flags that trigger interrupts;
- SPI bus busy status flag;
- Hardware CRC to support reliable communication:
  - In send mode, the CRC value can be sent as the last byte;
  - In full duplex mode, CRC check is automatically carried out on the last byte received;
- Main mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffers that support DMA functionality: Generates send and receive requests
- Maximum interface speed: 18Mbps

5.14 Synchronous Serial Interchip Sound（I2S）

I2S is a 4-pin synchronous serial interface communication protocol that can operate in master or slave mode. It can be configured for 16-bit, 24-bit, or 32-bit transmission, as well as input or output channels, and supports audio sampling frequencies from 8 kHz to 96 kHz. It supports four audio standards, including the Philips I2S standard, the MSB and LSB alignment standard, and the PCM standard.

It can work in both master and slave modes in half duplex communication. When it is the master device, it provides a clock signal to an external slave device through the interface.

The main functions of I2S interface are as follows:

- Half-duplex communication (only send or receive at the same time);
- Master or slave operation;
- 8-bit linear programmable pre-divider for accurate audio sampling frequency (8kHz to 96kHz);
- The data format can be 16-bit, 24-bit, or 32-bit;
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame);
- Programmable clock polarity (stable state);
- Overflow flag bits in send mode and overflow flag bits in master/slave receive mode;
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel;
- Supported I2S protocols:
- I2S Philips standard
- MSB alignment standard (left alignment)
- LSB alignment standard (right alignment)
- PCM standard (16-bit channel frames with long or short frame synchronization or 16-bit data framesextended to 32-bit channel frames)
- Data direction is always MSB first;
- Both sending and receiving have DMA capability

- The master clock can be output to external audio devices, fixed frequency is 256xFs (Fs is the audio sampling frequency)

5.15 General purpose input/output（GPIO）

GPIO (General Purpose Input/Output) stands for Generic I/O, AFIO (Alternate-Function Input/Output) stands for Multiplexed Function I/O.The chip supports up to 23 GPIOs and is divided into 3 groups (GPIOA/GPIOB/GPIOC), group A has 13 ports per group, group B has 7 ports(among which 4 of them are SPI multiplexing to RF) and group C has 3 ports.GPIO ports share pins with other reusable peripherals, and users can configure them flexibly according to their needs.Each GPIO pin can be independently configured as an output, input, or multiplexed peripheral function port.Except for analog input pins, all other GPIO pins have high current flow capability.

The main characteristics of GPIO are described as follows:

- GPIO ports can be configured separately by the software in the following modes:
  - Input floated
  - Input pull-up
  - Input pull down
  - Analog function
  - Open drain output and up/down can be configured
  - Push-pull output and up/down configurable
  - Push-pull multiplexing function and up/down configurable
  - Open drain multiplexing function and up/down configurable
- Separate bit setting or bit clearing
- All IO support external interrupt functionality
- All IO support low-power mode wake-up, with rising or falling edges configurable
- Sixteen EXITs can be used for SLEEP or STOP mode wake up, and all I/O can be reused as EXTI
- PA 0/ PC 13/ PA 2 three wake-up IO can be used for PD mode wake-up, I/O filtering time is 1us maximum
- Supports software remapping the I/O reusing function
- Support GPIO locking mechanism, reset mode to clear the locked state
- Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit half-word or 8-bit byte access is not allowed).

5.16 Analog to digital converter（ADC）

12-bit ADC is a high-speed successive approximation analog-to-digital converter. It has up to 6 channels and can measure 6 external and 3 internal signal sources. The A/D conversion of each channel can be executed in single, continuous, scanning or discontinuous mode. The ADC result can be left-aligned or right-aligned stored in the 16-bitdata register; ADC input clock must not exceed 18 MHz.

The main characteristics of ADC are described as follows:

- Support 1 ADC, single-ended input, can measure 12 external and 4 internal signal sources
- Support 12-bit resolution, the highest sampling rate is 1 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - Only AHB_CLK can be configured as a working clock source, up to 48 MHz
  - PLL can be configured as a sampling clock source, up to 18 MHz, supportfrequency division 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256
  - AHB_CLK can be configured as the sampling clock source, up to 18 MHz, support frequency division 1, 2, 4, 6, 8, 10, 12, 16, 32
  - The timing clock is used for internal timing functions, and the frequency must be configured to 1 MHz.
- Support timer trigger ADC sampling
- Interrupts are generated at the end of conversion, the end of injection conversion, and the occurrence of analog watchdog events
- Single and continuous conversion mode
- Auto scan mode from channel 0 to channel N
- Data alignment with embedded data consistency
- Sampling interval can be programmed separately per channel

- Both rule conversion and injection conversion have external trigger options
- Discontinuous mode
- ADC power supply requirements: 2.4 V to 3.6 V
- ADC input range: 0 ≤ VIN ≤ VDDA
- During regular channel conversion, a DMA request is generated.

5.17 Operational Amplifier（OPAMP）

Built-in an independent operational amplifier with multiple working modes such as external amplification, internal follower and programmable amplifier (PGA) (or both internal amplification and external filtering).

The main functions are as follows:

- Support rail-to-rail input
- OPA linear output range 0.4 V~VDDA-0.4 V
- Can be configured as independent operational amplifier and programmable gain operational amplifier;
- Forward and reverse input multiple selection；
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)；
  - PGA mode, programmable gain is set to 2X, 4X, 8X, 16X, 32X
  - Follower mode；
- The internally connected ADC channel is used to measure the output signal of the operational amplifier

5.18 Analog Comparator（COMP）

Built-in 1 comparator, which can be used as a separate device (all ports of the comparator are led to I/O), or it can be used in combination with a timer. In motor control applications, it can be used in conjunction with the PWM output from the timer to form a cycle-by-cycle current control.

The main functions of the comparator are as follows:：

- 1 independent comparator COMP, and it is a low-power comparator (can work in LPRUN, SLEEP and STOP modes)
- Built-in a 64-level programmable reference input voltage source VREF
- Support filter clock, filter reset
- Output polarity can be configured high and low
- Hysteresis configuration can be configured without, low, medium, high
- The comparing results can be output to the I/O port or the trigger timer for capturing events, OCREF_CLR events, braking events, and generating interrupts
- Input channel can be multi-selected I/O port, VREF
- It can be equipped with read-only or read-write, and it needs to be reset to unlock when locked
- Support blanking (Blanking), the blanking source can be configured to generate Blanking
- COMP can wake up the system from low power consumption mode by generating an interrupt, and COMP has the ability to wake up the system from STOP
- Configurable filter window size
- Configurable filter threshold size
- Configurable sampling frequency for filtering

5.19 Temperature Sensor（TS）

The temperature sensor generates a voltage that changes linearly with temperature, and the conversion range is between 1.8 V < VDDA < 3.6 V. The temperature sensor is internally connected to the input channel of ADC_IN12 to convert the output of the sensor to a digital value.

5.20 BEEPER

The BEEPER module supports complementary outputs and can generate periodic signals to drive external passive beeper. Used to generate prompt sound or alarm sound.

5.21 HDIV/ SQRT

The divider (HDIV) and square root (SQRT) are mainly used in some scenarios with high requirements for computing energy efficiency, and are used to partially supplement the deficiencies of the microcontroller in computing. The divider and square root calculator can perform division or square root calculation of unsigned 32-bit integers.

The main features of HDIV and SQRT are as follows:

- Only support word operation
- 8 clock cycles to complete an unsigned integer division operation
- 32-bit dividend, 32-bit divisor, output 32-bit quotient and 32-bit remainder
- Divisor is zero warning flag, division operation end flag
- 32-bit unsigned square root integer, 16-bit root root output
- Complete an unsigned integer square root operation in 8 clock cycles
- You can judge whether the calculation is complete by setting the interrupt enable or query the relevant register bits

5.22 Cyclic Redundancy Check Calculation Unit（CRC）

Integrating CRC 32 and CRC 16 functions, the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335- 1 standard, it provides a means to detect flash memory errors. The CRC calculation unit can be used to calculate the signature ofthe software in real time and compare it with the signature generated when the software is linked and generated

The main characteristics of CRC are as follows:

- CRC 16：Support polynomial X16+X15+X2+X0
- CRC 32：Support polynomial X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 +X2 + X +1
- CRC calculation time： 4 AHB clock cycles (HCLK)
- The initial value of cyclic redundancy calculation can be configured
- Support DMA mode

5.23 Unique device ID（UID）

CMT2380F64 have built-in two unique device ID of different lengths, 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory. The information contained in them is programmed at the factory, and is guaranteed to be unique to any micro-controller under any circumstances. User applications or external devices can be read through the CPU or SWD interface and cannot be modified.

The UID is 96 bits, usually used as a serial number or as a password. When programming the flash memory, this unique identification is combined with the software encryption and decryption algorithm to further improve the security ofthe code in the flash memory. It can also be used for activation with security Functional bootloader (Secure Bootloader).

The UCID is 128 bits and complies with the definition of the chip serial number which contains information on chip production and version.

5.24 Serial wire SWD debug port（SWD）

The ARM SWD Interface is embedded.

6 Order Information

Table **6-1.CMT2380F64 order information**

Type	Description	Package	Packet Option	Operation Condition	MOQ
CMT2380F64-EQR[1]	CMT2380F64, low power consumption Sub- 1GHz RF transceiverSoC	QFN40 (5x5)	Make up with disk	1.8 to 3.6 V, -40 to 85℃	3,000

Remarks:

[1]. “E” represents the extended industrial product grade，with supported temperature range from -40 to +85 ℃.

“Q” represents package type of QFN40.

“R” represents the tape and tray type with MOQ as 3,000.

For more information, please refer to official website: www.cmostek.com

For purchasing or pricing requirements, please contact sales@cmostek.com or your local sales representatives.

7 Package Outline

Package information of CMT2380F64 is shown as followed.

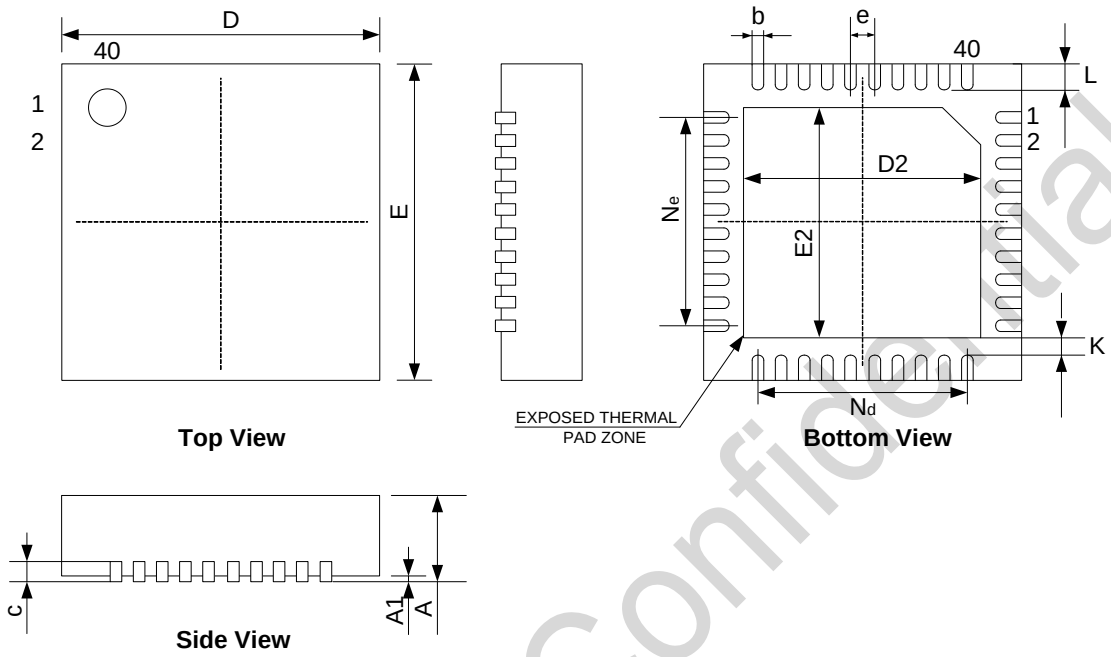


Figure 7-1. QFN40 5x5 package

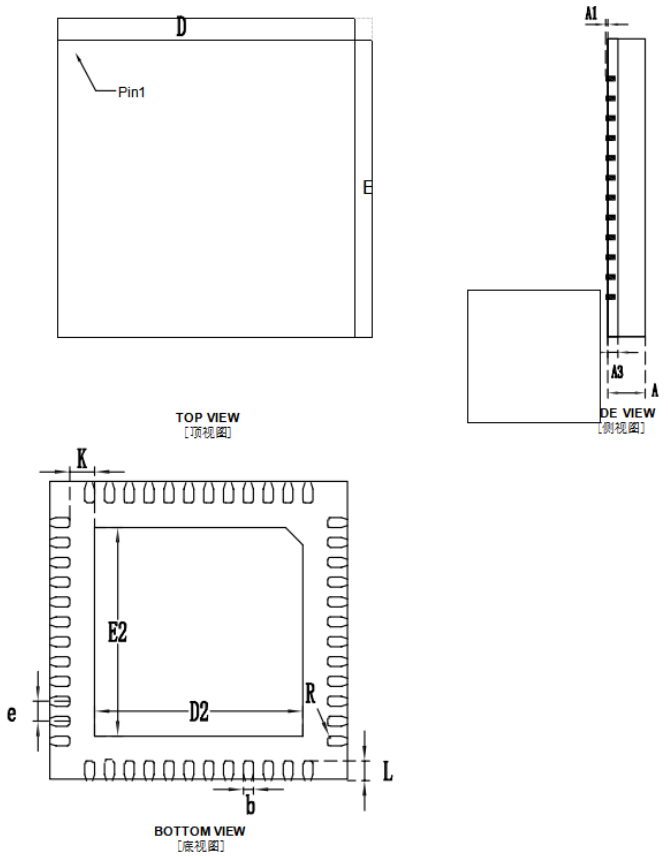


Figure 7-2. QFN48 6x6 package

Table 7-1. QFN40 5x5 package size

Symbol	Size (millimeter mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
C	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.40 BSC		
Ne	3.60 BSC		
Nd	3.60 BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.35	0.40	0.45
L1	0.10REF		
K	0.20	-	-
h	0.30	0.35	0.40

Table 7-2. QFN48 6x6 package size

Symbol	Size (mm)		
	Min.	Typ.	Max.
A	0.65	0.75	0.85
A1	0	0.02	0.05
A3	——	0.203	——
b	0.175	0.20	0.225
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e		0.40	
D2	——	4.20	——
E2	——	4.20	——
L	——	0.40	——
K	——	0.50	——
R	——	0.05	——

8 Silk Printing Information

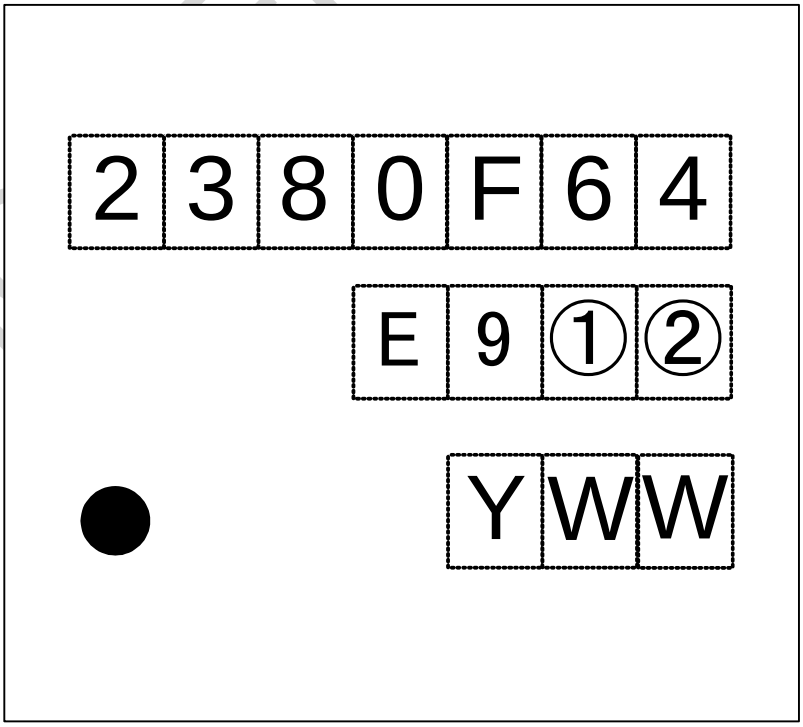


Figure 8-1. CMT2380F64 Top mark

Table 8-1. CMT2380F64 top mark description

Printing method	Laser
Pin1 marking	Circle diameter = 0.3 mm
Font size	0.5 mm, right alignment
First line silk printing	2380F64, Representative model CMT2380F64
Second line silk printing	E9①②Internal tracking code
Third line silk printing	Date code, assigned by packaging plant, Y represents the last digit of the year and WW represents the working week

9 Relevant Documents

Table 9-1. Other related application documents

Number	File Name	Description
AN141	*CMT2300A Schematic Diagram and PCB Map Guide*	*CMT2380F17 RF match design guidelines*
AN142	*CMT2300A Quick User Guide*	*CMT2380F17 Radio frequency quick entry*
AN143	*CMT2300A FIFO and Packet Format User Guide*	*CMT2380F17 Guide to the use of RF sending and receiving messages*
AN144	*CMT2300A RSSI User Guide*	*CMT2380F17 The RF Rssi usingguide*
AN146	*CMT2300A Low Power Consumption User Guide*	*CMT2380F17 RF Low power design guidelines*
AN147	*CMT2300A Special Function User Guide*	*CMT2380F17RF feature function description*
AN149	*CMT2300ARF Parameter Configuration Guide*	*CMT2380F17 Description of matching parameters of RF frequency points*
AN150	*CMT2300ALow-voltage TXPower Compensation*	*CMT2380F17 Description of the RF lowtransmission power compensation*
AN197	*CMT2300A-CMT2119B-CMT2219BFast Manual Hopping*	*CMT2380F17 Quick manual frequency hopping instructions*
AN198	*CMT2300A-CMT2119B-CMT2219B Precautions for status switch*	*CMT2380F17 RF state switching considerations*
AN199	*CMT2300A-CMT2119B-CMT2219B RF frequency calculation Guide*	*CMT2380F17 Description of the RF frequency calculation*

10 Revision History

Table 10-1. Revision history

Version	Chapter	Modify	Date
0.1	All	Initial	2022-05-13
0.2	All	Added the QFN48 top view and package information	2022-07-11
0.3	1.12	Update the controller external clock source description.	2022-07-15

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