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N725

Hardware User Guide

Issue 2.1 Date 2022-11-04

Notice

This document provides guide for users to use N725.

This document is intended for system engineers (SEs), development engineers, and test engineers.

THIS GUIDE PROVIDES INSTRUCTIONS FOR CUSTOMERS TO DESIGN THEIR APPLICATIONS. PLEASE FOLLOW THE RULES AND PARAMETERS IN THIS GUIDE TO DESIGN AND COMMISSION. NEOWAY WILL NOT TAKE ANY RESPONSIBILITY OF BODILY HURT OR ASSET LOSS CAUSED BY IMPROPER OPERATIONS.

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About This Document

Scope

This document is applicable to the N725 series.

It defines the features, indicators, and test standards of the N725 module and provides reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2022-05	Initial draft	Zou Shiqiang
2.0	2022-08	• Updated “N725-CA” to “N725” • Updated the typical voltage of VBAT from 3.8 V to 3.6 V • Updated Figure 4-1 • Updated content layout of Section 5.2	Zou Shiqiang
2.1	2022-10	• Updated current data in Chapter 2.3 • Updated RGMII/RMII power domain description in Table 4-2 • Updated frequencies in Table 6-2 • Updated eCall temperature data in Table 6-3	Zou Shiqiang

Conventions

Symbol	Indication
	Indicates danger or warning. This information must be followed. Otherwise, a catastrophic module or user device failure or bodily injury may occur.
	Indicates caution. This symbol alerts the user to important points about using the module. If these points are not followed, the module or user device may fail.
	Indicates instructions or tips. This symbol provides advices or suggestions that may be useful when using the module.

Related Documents

Neoway_N725_Datasheet

Neoway_N725_Product_Specifications

Neoway_N725_AT_Commands_Mannual

Neoway_N725_EVK_User_Guide

1 Safety Recommendations

Ensure that this product is used in compliance with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or workplace:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, and so on.

  If the product is used in a place with flammable gas or dust such as propane gas, gasoline, or flammable spray, the product will cause an explosion or fire.

- Do not use this product in environments such as hospital or airplane where it might interfere with other electronic equipment.

  If the product is used in medical institutions or on airplanes, electromagnetic waves emitted by this product may interfere with surrounding equipment.

Please follow the requirements below in design and use of the application for this module:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Please design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Please connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not insert/remove a USIM card or move a memory card from the module while it is still powered on.

2 About N725

This chapter introduces product overview, block diagram, and basic features of N725.

2.1 Product Overview

N725 is an industry-grade cellular module that supports FDD-LTE (Cat. 4), TDD-LTE (Cat. 4), WCDMA, and GSM. It has dimensions of (30.00±0.10) mm × (28.00±0.10) mm × (2.80±0.20) mm and supports rich hardware interfaces. It is suitable for developing IoT communication devices such as wireless meter reading terminals, vehicle/handheld POS, industrial routers and so on.

N725 has the following characteristics:

- ARM Cortex-A7, 1.2 GHz main frequency, 32 kB L1 cache at most.
- Supported network modes: LTE Cat. 4, WCDMA, GSM.
- Supported interfaces: USIM, I2S/PCM, UART, USB, RMII/RGMII, SD/MMC, SDIO, I2C, SPI, *PCIe, and GNSS (optional).

Table 2-1 lists the variants and frequency bands that N725 supports.

Table 2-1 Variants and frequency bands

Variant	Region	Category	Band	GNSS[1]	Codec
CA	Chinese mainland	Cat.4	FDD-LTE: B1, B3, B5, B8 TDD-LTE: B34, B38, B39, B40, B41 WCDMA: B1, B5, B8 GSM/GPRS/EDGE: 900/1800 MHz	Supported	Not supported
EA	Europe/Middle East/Africa	Cat.4	FDD-LTE:B1, B3, B5, B7, B8, B20, B28 TDD-LTE: B38, B40, B41 WCDMA: B1, B5, B8 GSM/GPRS/EDGE: 900/1800 MHz	Supported	Not supported

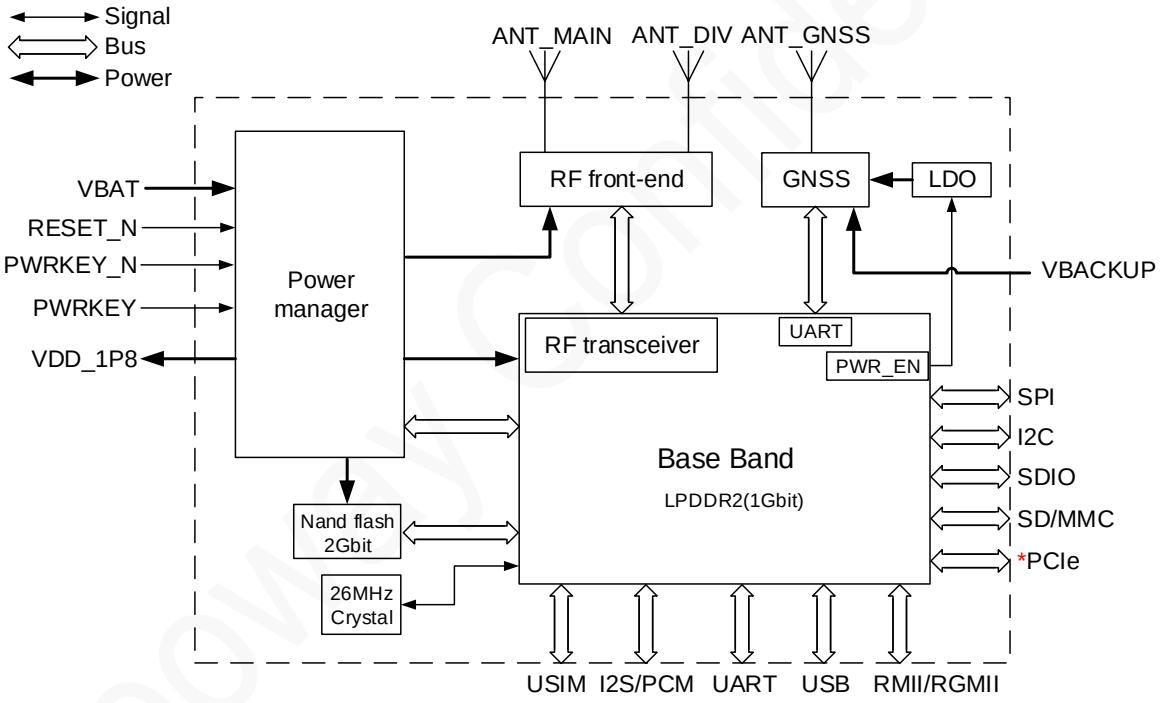
[1] GNSS is optional.

2.2 Block Diagram

N725 consists of the following functionality units:

- Baseband
- 26 MHz crystal
- Power management
- Radio frequency
- Flash
- GNSS
- Digit interfaces (USIM, I2S/PCM, UART, USB, RMII/RGMII, SD/MMC, SDIO, I2C, SPI, *PCIe)

Figure 2-1 Block diagram



2.3 Basic Features

Parameter	Description
Physical features	• Dimensions: (30.00±0.10) mm × (28.00±0.10) mm × (2.80±0.20) mm • Package: 100-pin LGA • Weight: about 5.20 g
Temperature	Operating: -30°C to +75°C

ranges	Extended[2]: -40°C ~ +85°C Storage: -40°C to +90°C
Operating voltage (DC)	VBAT: 3.4 V- 4.2 V, typical value: 3.6 V
Operating current	Sleep mode[3]: ≤ 3 mA
	Standby mode[4]: ≤ 20 mA (USB disconnected)
	Operating[5] (LTE mode):≤ 650 mA
Application processor	ARM Cortex-A7, 1.2 GHz main frequency, 32 kB L1 cache at most.
Memory	RAM: 128 MB ROM: 256 MB
Band	See Table 2-1.
Wireless rate	GPRS: Max 85.6 Kbps (DL)/Max 85.6 Kbps (UL) EDGE: Max 236.8 Kbps (DL)/Max 236.8 Kbps (UL) WCDMA: HSPA+, Max 21 Mbps (DL)/Max 5.76 Mbps (UL) LTE-FDD: Cat4, no-CA, Max 150 Mbps (DL)/Max 50M bps (UL) LTE-TDD: Cat4, no-CA, Max 130 Mbps (DL)/Max 30 Mbps (UL)
Transmit power	EGSM900: +33 dBm (Power Class 4) DCS1800: +30 dBm (Power Class 1) EDGE 900 MHz: +27 dBm (Power Class E2) EDGE1800 MHz: +26 dBm (Power Class E2) WCDMA: +23 dBm (Power Class 3) LTE: +23 dBm (Power Class 3)
Application interfaces	2G/3G/4G antenna, diversity antenna, GNSS antenna. All of each has a characteristic impedance of 50 Ω.
	Three UART (one of which is a Debug UART)
	One USIM interface, 1.8 V/3.0 V adaptive
	One USB 2.0 interface
	One SDIO interface
	One SD/MMC interface

Extended[2]: The module can be registered on the network, but some indicators cannot meet 3GPP standards.

Sleep mode[3] the module enters a low power consumption state. In this state, the peripheral interface of the module is disabled, but the radio frequency (RF) is functioning properly. The module will exit the sleep mode when there is an incoming call or SMS message, and will re-enter the sleep mode at the end of the incoming call or conversation.

[4]Standby mode: the module is in normal working state, but there is no on-going data service.

[5]Operating mode: operating current of the module when there is data communication. Only the currents in LTE mode are listed here. For details about currents under other network standards, see the N725 current test report.

	One PCM/I2S interface
	One RMII/RGMII interface
	One SPI interface, host mode only
	One I2C interface, master mode only
	One PCIe Gen1 interface, supporting only RC mode
AT commands	3GPP Release 9 Neoway extended commands
SMS	PDU, TXT
Data	PPP, RNDIS
Protocol	TCP/TCPS, UDP, HTTP/HTTPS, FTP, MQTT
Certification approval	CCC, SRRC, CTA, RoHS

"extended[2)]" The module can be registered on the network, but some indicators cannot meet 3GPP standards.

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"Standby mode[4)]": the module is in normal working state, but there is no on-going data service.

"Operating mode[4)]": operating current of the module when there is data communication. Only the currents in LTE mode are listed here. For details about currents under other network standards, see the N725 current test report.

3 Reference Standards

N725 is designed by referring to the following standards:

- 3GPP TS 36.521-1 V9.10.0 User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Radio Resource Management (RRM) conformance testing
- 3GPP TS 21.111 V9.0.0 USIM and IC card requirements
- 3GPP TS 31.102 V9.19.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V9.12.2 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V9.9.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V9.0.1 Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

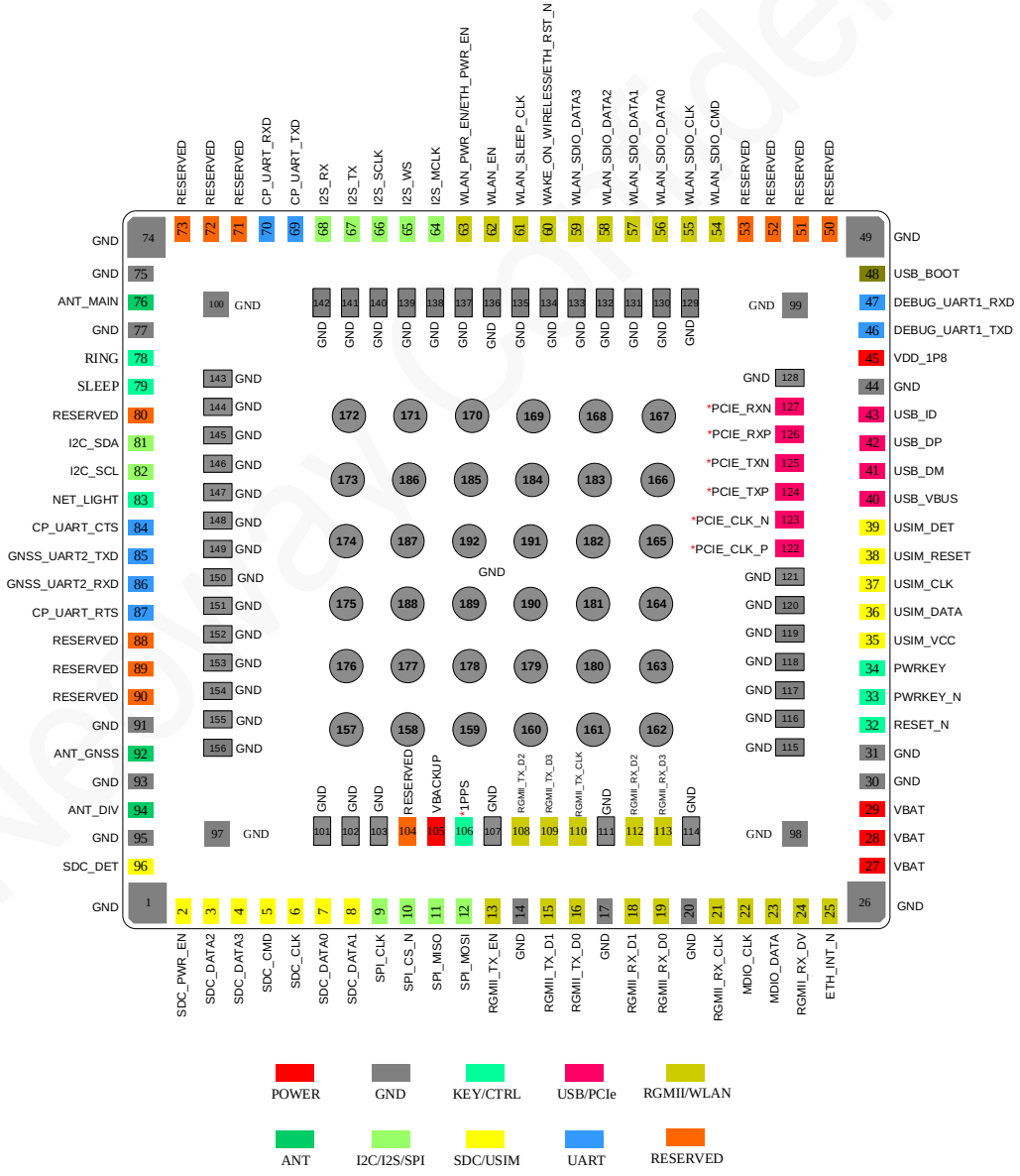
4 Module Pins

There are 192 pins on N725 and their pads are introduced in LGA package.

4.1 Pin Layout

The following figure shows the pad layout of N725.

Figure 4-1 N725 pin definition (top view)



*PCIe: in development

*1PPS: in development

N725 does not support GNSS_UART2 and USB_ID by default.

4.2 Pin Description

Table 4-1 lists the IO definitions and DC characteristics.

Table 4-1 Pin description

IO type	Pin description
AI	Analog input
AO	Analog output
AIO	Analog input/output
B	Digital input/output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output

- Do Not pull down the USB_BOOT pin before the initialization is completed.
- SD/eMMC supports 1.8 V level by default. If supporting 3.0 V level is required, the firmware should be configured; ensure whether it is configured before using the pin.
- The RMII and RGMII pins only support 1.8 V level.
- All the RESERVED and Ground pins must be left floating.

Table 4-2 Level feature

Interface type	Power domain	Power domain description	Power domain features	Logic level
USIM	P1	USIM interface	1.8 V/3.0 V self-adaptive	1.8 V level feature: V_{IH} = 0.7 x V_{DD_P1} ~ V_{DD_P1} + 0.2V V_{IL} = -0.3 V ~ 0.3 x V_{DD_P1} V_{OH} = V_{DD_P1} - 0.2V ~ V_{DD_P1} V_{OL} = 0V ~ 0.1 x V_{DD_P1} 3.0V level feature: V_{IH} = 0.7 x V_{DD_P1} ~ V_{DD_P1} + 0.3V V_{IL} = -0.3V ~ 0.3 x V_{DD_P1} V_{OH} = 0.7 x V_{DD_P1} ~ V_{DD_P1} V_{OL} = 0V ~ 0.1 x V_{DD_P1}
SD/eMMC	P2	SD/MMC power domain	1.8 V or 3.0 V	1.8 V level feature: V_{IH} = 0.7 x V_{DD_P2} ~ V_{DD_P2} + 0.2V V_{IL} = -0.3V ~ 0.3 x V_{DD_P2} V_{OH} = V_{DD_P2} - 0.2V ~ V_{DD_P2} V_{OL} = 0V ~ 0.1 x V_{DD_P2} 3.0 V level feature: V_{IH} = 0.7 x V_{DD_P2} ~ V_{DD_P2} + 0.3V V_{IL} = -0.3V ~ 0.3 x V_{DD_P2}

				V_{OH} = 0.7 x V_{DD_P2} ~ V_{DD_P2} V_{OL} = 0V ~ 0.1 x V_{DD_P2}
GPIO	P3	Digital I/O power domain	1.8 V power	Input: V_{IH} = 0.7 x V_{DD_P3} ~ V_{DD_P3} + 0.2V V_{IL} = -0.3V ~ 0.3 x V_{DD_P3} Output: V_{OH} = V_{DD_P3} - 0.2V ~ V_{DD_P3} V_{OL} = 0V ~ 0.1 x V_{DD_P3}
RMII	P4	RMII interface	1.8 V	1.8 V level feature: V_{IH} = 0.7 x V_{DD_P4} ~ V_{DD_P4} + 0.2V V_{IL} = -0.3V ~ 0.3 x V_{DD_P4} V_{OH} = V_{DD_P4} - 0.2V ~ V_{DD_P4} V_{OL} = 0V ~ 0.1 x V_{DD_P4}

Table 4-3 Pin description

Signal	Pin	I/O	Function description	Level feature	Remarks
Power interface					
VBAT	27, 28, 29	PI	Main power supply of the module	V_{min} = 3.4 V V_{norm} = 3.6 V V_{max} = 4.2 V	The external power supplies at least 2.5 A current to VBAT.
VDD_1P8	45	PO	1.8 V power output	V_{norm} = 1.8 V I_{max} = 50 mA	Used only for level shifting. Leave this pin floating if it is not used.
VBACKUP	105	PI	GNSS backup power supply	V_{min} = 1.65 V V_{norm} = 1.8 V V_{max} = 3.6 V	Used for GNSS hot start function. This pin can be connected to a 3.0 V/3.3 V button battery or a farad capacitor. Connecting this

					pin through a capacitor (≥1 uF) to ground if VBACKUP is not used.
GND	1, 14, 17, 20, 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97 - 103, 107, 111, 114 - 121, 128 - 192				Ensure that all GND pins are grounded.
Control interfaces					
RESET_N	32	DI	Used to reset the module.	-	Low pulse trigger
PWRKEY_N	33	DI	Used to power on/off the module.	-	The default pull-up power supply is VBAT.
PWRKEY	34	DI	Startup control	-	Power-on of the module is triggered by high-level. Leave this pin floating if it is not used.
USB_BOOT	48	DI	Forcible download/upgrade control pin	P3	Pulling down this pin to GND can trigger the module to enter USB download mode. Leave this pin floating if it is not used.
RING	78	DO	Incoming call indicator control	P3	Leave this pin floating if it is not used.
SLEEP	79	DI	Sleep and wakeup control	P3	Leave this pin floating if it is not used.
NET_LIGHT	83	DO	Network indicator control	P3	Leave this pin floating if it is not used.
SD/eMMC interface					
SDC_PWR_EN	2	DO	Control of the external power supply for SD/MMC	P3	Leave this pin floating if it is not used.
SDC_DATA_2	3	B	SD/MMC data 2	P2	Leave this pin floating if it is not used.
SDC_DATA_3	4	B	SD/MMC data 3	P2	Leave this pin floating if it is not used.
SDC_CMD	5	DO	SD/MMC command control	P2	Leave this pin floating if it is not used.
SDC_CLK	6	DO	SD/MMC clock	P2	Leave this pin floating if it is not used.

SDC_DATA_0	7	B	SD/MMC data 0	P2	Leave this pin floating if it is not used.
SDC_DATA_1	8	B	SD/MMC data 1	P2	Leave this pin floating if it is not used.
SDC_DET	96	DI	SD/MMC detect input	P3	Leave this pin floating if it is not used.
SPI interface					
SPI_CLK	9	DO	Clock signal	P3	Leave this pin floating if it is not used.
SPI_CS_N	10	DI	Chip select signal of the slave device	P3	Leave this pin floating if it is not used.
SPI_MISO	11	DI	Input of the master device and output of the slave device	P3	Leave this pin floating if it is not used.
SPI_MOSI	12	DO	Output of the master device and input of the slave device	P3	Leave this pin floating if it is not used.
RGMII interface					
RGMII_RX_D0	19	DI	Data receiving bit 0	P3	Leave this pin floating if it is not used.
RGMII_RX_D1	18	DI	Data receiving bit 1	P3	Leave this pin floating if it is not used.
RGMII_RX_D2	112	DI	Data receiving bit 2	P3	Leave this pin floating if it is not used.
RGMII_RX_D3	113	DI	Data receiving bit 3	P3	Leave this pin floating if it is not used.
RGMII_RX_DV	24	DI	Valid when receiving data	P3	Leave this pin floating if it is not used.
RGMII_RX_CLK	21	DI	Receiving clock	P3	Leave this pin floating if it is not used.
RGMII_TX_D0	16	DO	Data sending bit 0	P3	Leave this pin floating if it is not used.
RGMII_TX_D1	15	DO	Data sending bit 1	P3	Leave this pin floating if it is not used.
RGMII_TX_D2	108	DO	Data sending bit 2	P3	Leave this pin floating if it is not used.
RGMII_TX_D3	109	DO	Data sending bit 3	P3	Leave this pin floating if it is not used.
RGMII_TX_CLK	110	DO	Sending clock	P3	Leave this pin floating if it is not used.

RGMII_TX_EN	13	DO	Enable data sending	P3	Leave this pin floating if it is not used.
ETH_INT_N	25	DI	Interrupt signal input	P3	Leave this pin floating if it is not used.
WAKE_ON_WIRELESS/ETH_RST_N	60	DO	Reset signal output	P3	Leave this pin floating if it is not used.
WLAN_PWR_EN/ETH_PWR_EN	63	DO	Control of enabling the power supply for external PHY chips	P3	Leave this pin floating if it is not used.
RMII interfaces					
RMII_RX_D0	19	DI	Data receiving bit 0	P4	Leave this pin floating if it is not used.
RMII_RX_D1	18	DI	Data receiving bit 1	P4	Leave this pin floating if it is not used.
RMII_RX_DV	24	DI	Valid when receiving data	P4	Leave this pin floating if it is not used.
RMII_CLK	21	DI	Data clock	P4	Leave this pin floating if it is not used.
RMII_TX_D0	16	DO	Data sending bit 0	P4	Leave this pin floating if it is not used.
RMII_TX_D1	15	DO	Data sending bit 1	P4	Leave this pin floating if it is not used.
RMII_TX_EN	13	DO	Enable data sending	P4	Leave this pin floating if it is not used.
ETH_INT_N	25	DI	Interrupt signal input	P4	Leave this pin floating if it is not used.
WAKE_ON_WIRELESS/ETH_RST_N	60	DO	Reset signal output	P3	Leave this pin floating if it is not used.
WLAN_PWR_EN/ETH_PWR_EN	63	DO	Control of enabling the power supply for external PHY chips	P3	Leave this pin floating if it is not used.
MDIO interface					
MDIO_CLK	22	DO	MDIO clock	P3	Leave this pin floating if it is not used.
MDIO_DATA	23	B	MDIO data	P3	Connecting a 4.7 kΩ external pull-up resistor is required.

					Leave this pin floating if it is not used.
USIM interface					
USIM_VCC	35	PO	USIM power output	P1	I_{omax}=50 mA
USIM_DATA	36	B	USIM data input and output	P1	Connecting a 4.7 kΩ pull-up resistor to USIM_VCC is required.
USIM_CLK	37	DO	USIM clock output	P1	Leave this pin floating if it is not used.
USIM_RESET	38	DO	USIM reset	P1	Leave this pin floating if it is not used.
USIM_DET	39	DI	USIM detection	P3	It is recommended to connect this pin to VDD_1P8 through a 47 kΩ pull-up resistor if it is not used.
USB interface					
USB_VBUS	40	PI	Voltage detection	3.5 V to 5.2 V, typical value: 5.0 V	Used for software download and data transmission. DM and DP adopt differential routing, and the differential impedance must be 90 Ω. Leave this pin floating if it is not used.
USB_DM	41	IO	USB data negative signal	-	
USB_DP	42	IO	USB data positive signal	-	
USB_ID	43	DI	Master/slave detect	P3	Not supported by default Leave this pin floating if it is not used.
UART interfaces					
DEBUG_UART1_TXD	46	DO	Data transmitting	P3	Only used for debug. Leave this pin floating if it is not used.
DEBUG_UART1_RXD	47	DI	Data receiving	P3	
CP_UART_TXD	69	DO	Data transmitting	P3	It is used for data transmission and supports hardware flow control. Leave this pin floating if it is not used.
CP_UART_RXD	70	DI	Data receiving	P3	
CP_UART_CTS	84	DI	The user allows the module to	P3	

			send data.		
CP_UART_RTS	87	DO	The module requests the user to send data.	P3	
GNSS_UART2_TXD	85	DO	Data transmitting	P3	N725 does not support GNSS_UART2 by default.
GNSS_UART2_RXD	86	DI	Data receiving	P3	
WLAN interface					
WLAN_SDIO_CMD	54	B	SDIO command	P3	Leave this pin floating if it is not used.
WLAN_SDIO_CLK	55	DO	SDIO clock	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA0	56	B	SDIO data bit 0	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA1	57	B	SDIO data bit 1	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA2	58	B	SDIO data bit 2	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA3	59	B	SDIO data bit 3	P3	Leave this pin floating if it is not used.
WAKE_ON_WIRELESS/ETH_RST_N	60	DO	WLAN wakeup control/ETH reset control	P3	Leave this pin floating if it is not used.
WLAN_SLEEP_CLK	61	DO	Wi-Fi sleep clock	P3	Clock frequency: 32 kHz Leave this pin floating if it is not used.
WLAN_EN	62	DO	WLAN enable control	P3	Leave this pin floating if it is not used.
WLAN_PWR_EN/ETH_PWR_EN	63	DO	Control of the external power supply for WLAN/ETH power supply enable control	P3	Leave this pin floating if it is not used.
I2S/PCM interface					
I2S_MCLK	64	DO	I2S master clock	P3	The default frequency is 26 MHz.
I2S_WS	65	B	I2S/PCM synchronization	P3	Leave this pin floating if it is not used.

			signal		
I2S_SCLK	66	DO	I2S/PCM data clock	P3	Leave this pin floating if it is not used.
I2S_TX	67	DO	I2S/PCM data sending	P3	Leave this pin floating if it is not used.
I2S_RX	68	DI	I2S/PCM data receiving	P3	Leave this pin floating if it is not used.
I2C interface					
I2C_SDA	81	B	I2C data	P3	Supporting only host mode; connecting this pin to VDD_1P8 through a 4.7 kΩ pull-up resistor externally is required.
I2C_SCL	82	DO	I2C clock	P3	
***1PPS**					
1PPS	106	DO	GNSS timing service output	P3	The 1PPS function is in development.
***PCIe interface**					
PCIE_WAKE_IN	54	DI	Input signal for wakeup	P3	PCIE_WAKE_IN and PCIE_RST_N are multiplexing pins that can be multiplexed as SDIO signals. The original function cannot be used with the SDIO function at the same time.
PCIE_RST_N	55	DO	Reset output signal	P3	
PCIE_CLK_P	122	-	PCIe clock signal positive	-	Supports only master mode
PCIE_CLK_N	123	-	PCIe clock signal negative	-	
PCIE_TXP	124	-	PCIe data sending positive	-	
PCIE_TXN	125	-	PCIe data sending negative	-	
PCIE_RXP	126	-	PCIe data receiving positive	-	
PCIE_RXN	127	-	PCIe data receiving negative	-	
Antenna interfaces					
ANT_MAIN	76	-	Main antenna	-	50 Ω impedance characteristics

ANT_GNSS	92	-	GNSS antenna	-	50 Ω impedance characteristics
ANT_DIV	94	-	Diversity antenna	-	50 Ω impedance characteristics
RESERVED	50 – 53, 71 – 73, 80, 88 – 90, 104		Ensure that all RESERVED pins are left floating. These RESERVE pins might have different definitions or functions.		

5 Application Interfaces

N725 provides various interfaces including power, control, communications, audio, peripheral, and RF to meet the functional requirements of customers in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

5.1 Power Interface

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

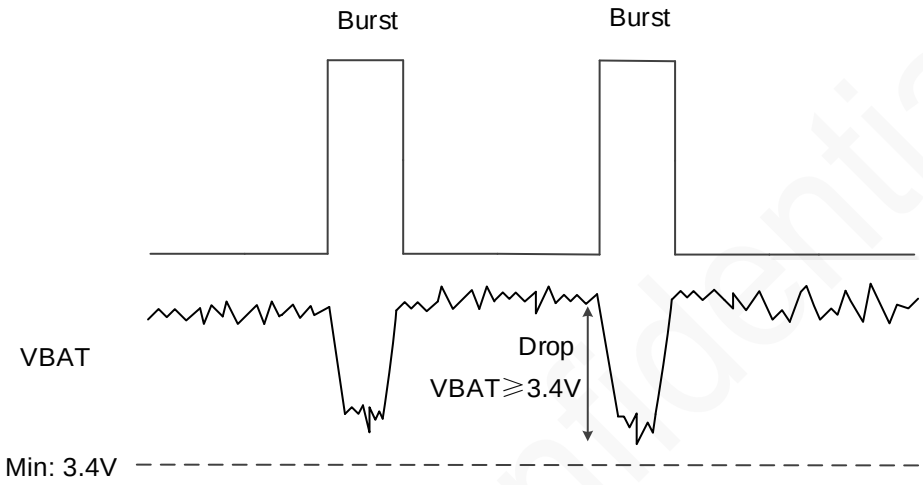
Signal	Pin	I/O	Function description	Remarks
VBAT	27, 28, 29	PI	Power input of the module	3.4 V - 4.2 V (typ.: 3.6 V)
VDD_1P8	45	PO	1.8 V power output	V_{norm} = 1.8 V I_{max} = 50 mA Only used for level shift and IO power supply. Add ESD protection when it is used.
VBACKUP	105	PI	GNSS backup power supply	Used for GNSS hot start; it can be connected to a button battery (3.0 V - 3.3 V) or a Farad capacitor. Connect this pin to ground through a capacitor (≥1uF) if not used.
GND	1, 14, 17, 20, 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97 - 103, 107, 111, 114 - 121, 128 - 192			Ensure that all GND pins are grounded.

5.1.1 VBAT

Schematic Design Guideline

In GSM/GPRS mode, RF data is transmitted in burst mode that generates voltage drops on the power supply. Furthermore, this results in a 217 Hz TDD noise through the power and the transient peak current is 2.4 A. Therefore, it is necessary to ensure that in the power supply design, the impedance of the power supply traces is low, and there are large-capacity capacitors to improve the freewheeling capability to ensure that the voltage will not drop below the minimum operating voltage of the module when the instantaneous current reaches its peak.

Figure 5-1 Voltage drop of the power supply.



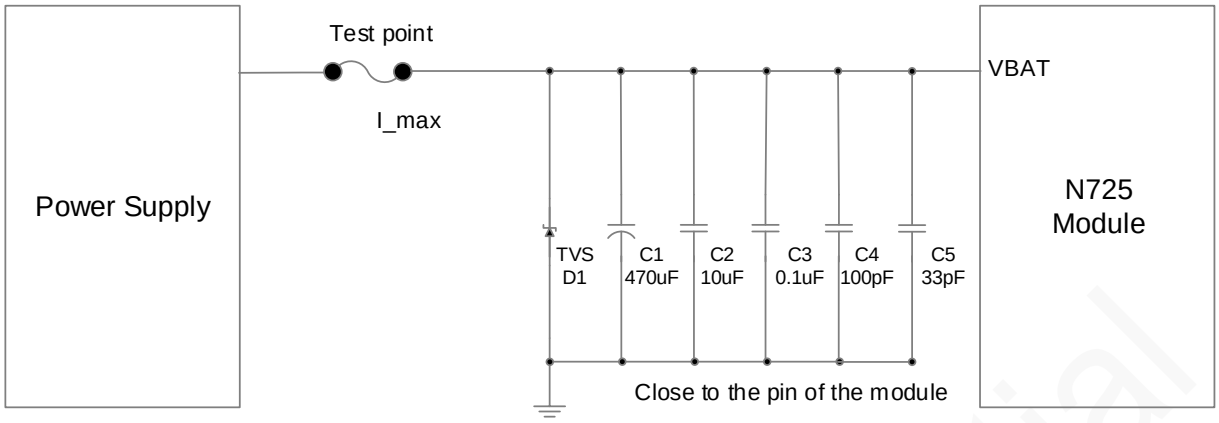
Never use a diode to make the drop voltage between a higher input and the module power supply. The forward voltage drop V_f of the diode has two characteristics: one is that it increases with the increase of forward current; the other is that it increases significantly at a low temperature. If there is an instantaneous high current, the instantaneous increase of forward voltage drop will lead to unstable operating voltage of the module, or even damage the module.

The power supply design of the N725 module is determined by the power input voltage. The designs are classified by power input voltage as follows:

- Supports the 3.4 V - 4.2 V power input (typical value: 3.6V, using the battery for power supply)
- Supports the 4.2 V - 5.5 V power input (typical value: 5.0 V, using the internal rectifier of the computer for power supply)
- Supports the 5.5 V - 24 V power input (typical value: 12 V, typically applicable to the automobile industry)

The recommended 3.4 V to 4.2 V input design is as follows:

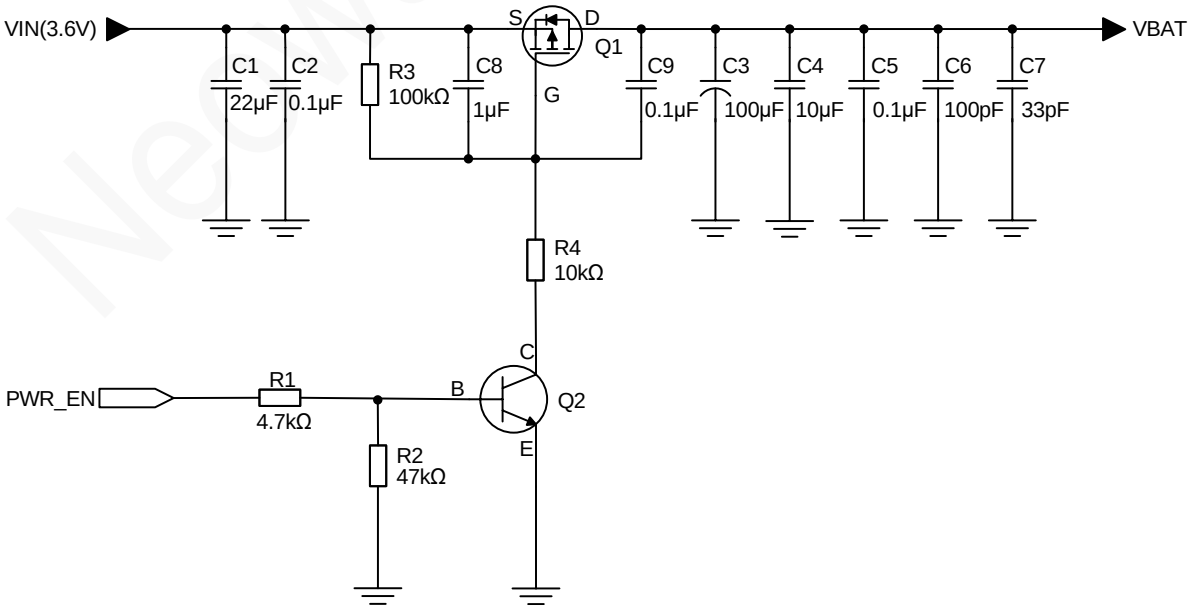
Figure 5-2 Recommended design 1



- The maximum input voltage for the module is 4.2 V and the typical value is 3.6 V. For VBAT, the recommended layout cable width is 2.5 mm or above.
- The reverse operating voltage (VRWM) of the TVS diode (D1) is 4.5 V, and the peak power Ppp is 2800 W (tp=8/20 uS). With surge protection function, place the TVS close to the input interface of the power input interface to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end component and the module are protected.
- A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be larger than 2 times the voltage across the power supply.
- Place a bypass capacitor (C2, C3, C4, C5) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

The following circuit design is recommended to control the power supply.

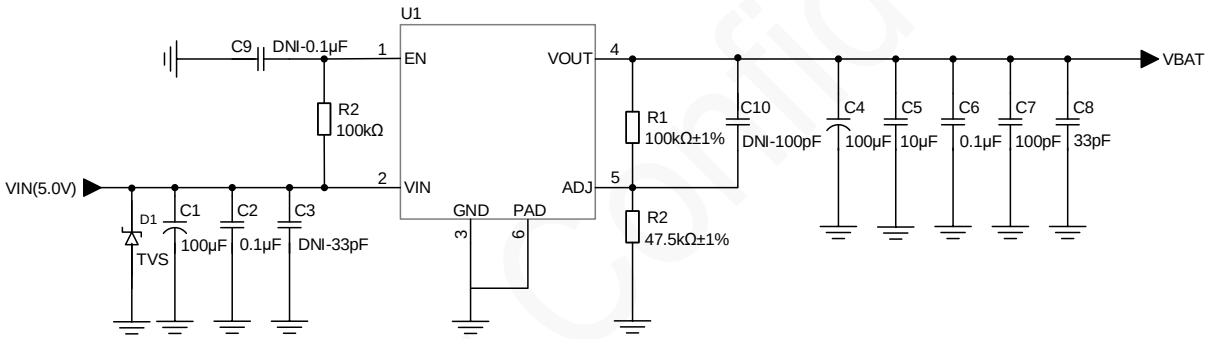
Figure 5-3 Recommended design 2



- Select an enhanced p-MOSFET at Q1, of which the safe operating voltage is at least 12 V (V_{dss}=-12 V) and drain current is at least 3.5 A ($I_{D(MAX)}$=-3.5 A) and Rds is low ($Rds_{(on)}$ =108 mΩ).
- Select a common NPN tripolar transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which operating voltage of the tripolar transistor might increase in low temperature; it is recommended that the value of R2 be at least 10 times that of R1.
- Place C3 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C3 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Place a bypass capacitor (C4, C5, C6, C7) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

Recommended 4.2 V to 5.5 V input design:

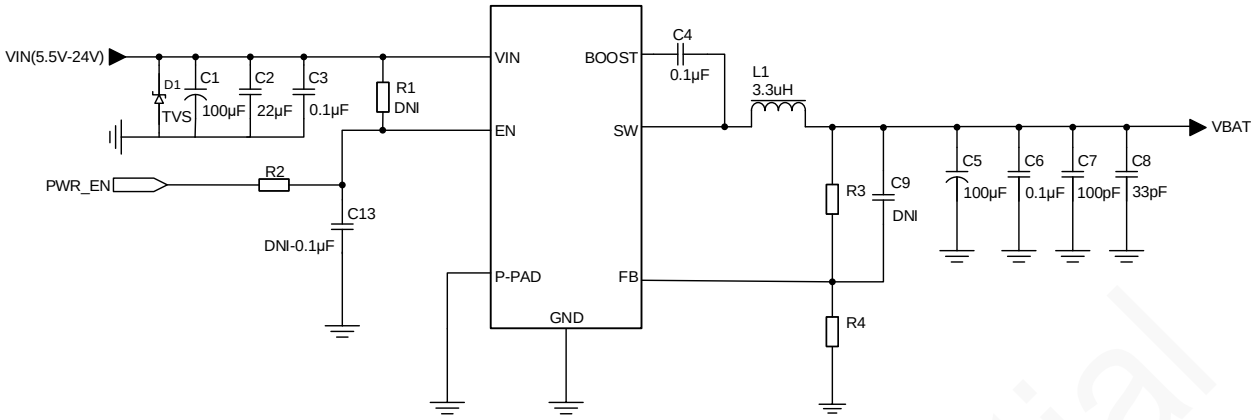
Figure 5-4 Recommended design 3



- Design with LDO is simpler and more efficient when the output of power supply is close to the permissible voltage across VBAT.
- Select an LDO that can output 2.5 A current at U1 to ensure the performance of the module.
- The reverse operating voltage (V_{RWM}) of the TVS diode (D1) is 4.5 V, and the peak power Ppp is 2800 W (tp=8/20 uS). With surge protection function, place the TVS close to the input interface of the power input interface to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end component and the module are protected.
- Place C4 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C4 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Place a bypass capacitor (C5, C6, C7, C8) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

Recommended 5.5 V to 24 V input design:

Figure 5-5 Recommended design 4



- As there is a big difference between the power input and VBAT, the DC-DC step-down chip should be selected, and the maximum output current should be at least 2.5 A.
- Place C5 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C7 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Place a bypass capacitor (C6, C7, C8) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

PCB Layout

An ESR capacitor must be placed at the output end of the power supply to suppress the peak current. A TVS must be placed at the power input end to suppress voltage spikes and protect back-end devices. The circuit design is important, and the device layout and routing are equally important. Several key points in power supply design are summarized below:

- The TVS can absorb instantaneous high-power pulses, and withstand instantaneous pulse current peaks up to tens or even hundreds of amperes. The clamp response time is extremely short. The TVS should be placed as close as possible to the power input to ensure that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB wires.
- The bypass capacitor must be placed close to the power supply pin of the module to filter out high-frequency noise signals in the power supply.
- For the module power circuit, the PCB routing width must ensure that the 2.5 A current can be passed safely, and there should be no obvious loop voltage drop. The PCB routing width should be at least 2.5 mm to ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make the power cable short and thick.
- Noise-sensitive circuits, such as audio circuits and RF circuits, should be kept away from power circuits, especially when the DC-DC power supply is used.

- The voltage frequency of the SW pin of the DC-DC power supply is high, and the loop should be minimized. Keep sensitive components far away from the SW pin of the DC-DC component to prevent noise coupling. Place feedback components as close as possible to the FB pin and COMP pin.
- The GND pin and bottom pad of the chip must be grounded to ensure good heat dissipation and noise isolation.

5.1.2 VDD_1P8

VDD_1P8 power is on normally and cannot be turned off even when the module is in sleep mode. Connecting the module to an external circuit will increase its power consumption in sleep module. It is recommended that VDD_1P8 is used for level shifting only and an ESD protector should be added.

N725 provides one VDD_1P8 output. It can provide the 1.8 V voltage and the maximum output current is 50 mA. It is recommended that DVDD_1P8 is used for level shifting and digital IO pull-up power supply only and an ESD protector should be added.

5.1.3 VBACKUP

VBACKUP is used for the hot start function of GNSS to supply power to the RTC and backup RAM of the GNSS unit of the module. When the main power supply VBAT is powered off, the module can still retain some key ephemeris data and almanac to realize the hot start function. The VBACKUP input voltage ranges from 1.65 V to 3.3 V; 3.0 V/3.3 V is recommended. Connect this pin to ground through a capacitor (≥1 uF) if not used.

5.2 Control Interfaces

PWRKEY_N and RESET_N cannot be used simultaneously.

Signal	Pin	I/O	Function description	Remarks
RESET_N	32	DI	Reset control	Triggered by the low pulse
PWRKEY_N	33	DI	Power-on/off control	Power-on/off of the module is low-power pulse-triggered, and is controlled based on the low pulse width. The internal interface voltage is default to VBAT.
PWRKEY	34	DI	Startup control	Active high Leave this pin floating if not used.

5.2.1 Module Startup

Ensure that the VBAT voltage is stable before controlling PWRKEY_N to start the module. It is recommended to control PWRKEY_N after the VBAT voltage keeps stable for 50 ms. Do Not keep the PWRKEY_N pin low all the time.

Table 5-1 Module startup

Trigger method	Shutdown method	Risk
Pulse	Input a low pulse to PWRKEY_N for more than 2s and release it to shut down the module.	Do Not cut off the power supply of the module when it is working normally to prevent its flash from being damaged.
Auto-start	Execute the shutdown AT command and then power down the module.	You should cut off the power supply of the module after executing the shutdown AT command; otherwise, the module will start again after shut-down.

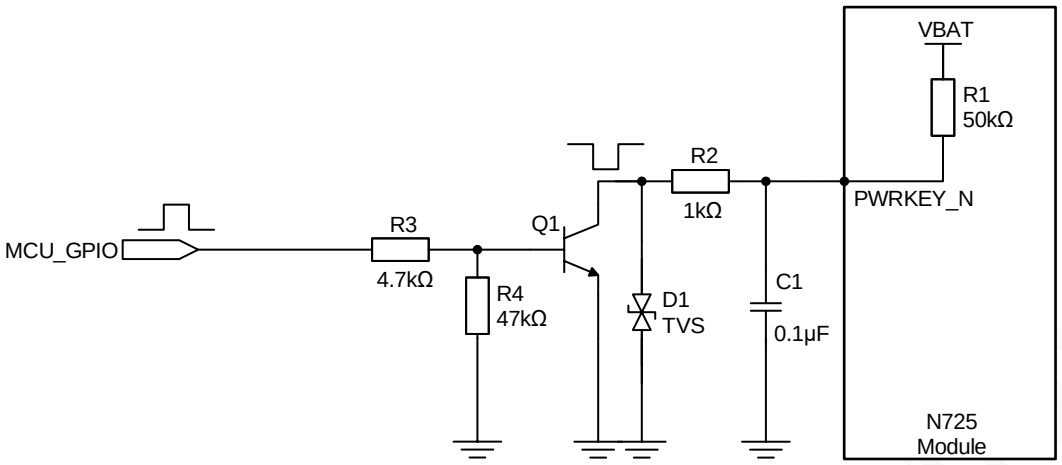
N725 allows startup by the following methods:

- Figure 5-6 shows the reference design of starting the module through pulse control.
- Figure 5-7 shows the reference design of automatic start once powered up.

Starting the module through pulse control

When the module is in shut-down state, inputting negative pulses for more than 0.5s and less than 2s to PWRKEY_N can start the module. The following figure shows the reference design of startup controlled by the PWRKEY_N pin:

Figure 5-6 Starting the module through pulse control

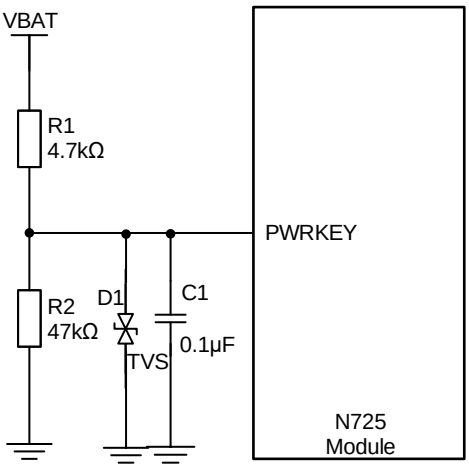


Automatic start once powered up

- If the design of automatic startup upon power-up is adopted, then module shutdown can be performed only through turning off the power supply of the module, that is, neither PWRKEY_N nor software shutdown can shut down the module.
- If the shutdown function is not required, you can directly pull up PWRKEY to VBAT to perform the automatic startup function.

PWRKEY is an active high startup pin. Pull the PWRKEY pin up to VBAT, and the module can start automatically once it is powered up. The following figure shows the reference design of startup controlled by the PWRKEY pin:

Figure 5-7 Reference design of automatic start once powered up



Startup process

After the module is powered up through VBAT, inputting a low level pulse to the PWRKEY_N pin for over 0.5s and less than 2s can trigger startup of the module. If your application does not need to control the ON/OFF state of the module, pull the PWRKEY pin up to VBAT, and the module can start automatically once it is powered up. The module startup time is greater than 10s but it may vary with different firmware of the module. The following figure shows the PWRKEY_N startup process:

Figure 5-8 Startup process (by controlling PWRKEY_N)

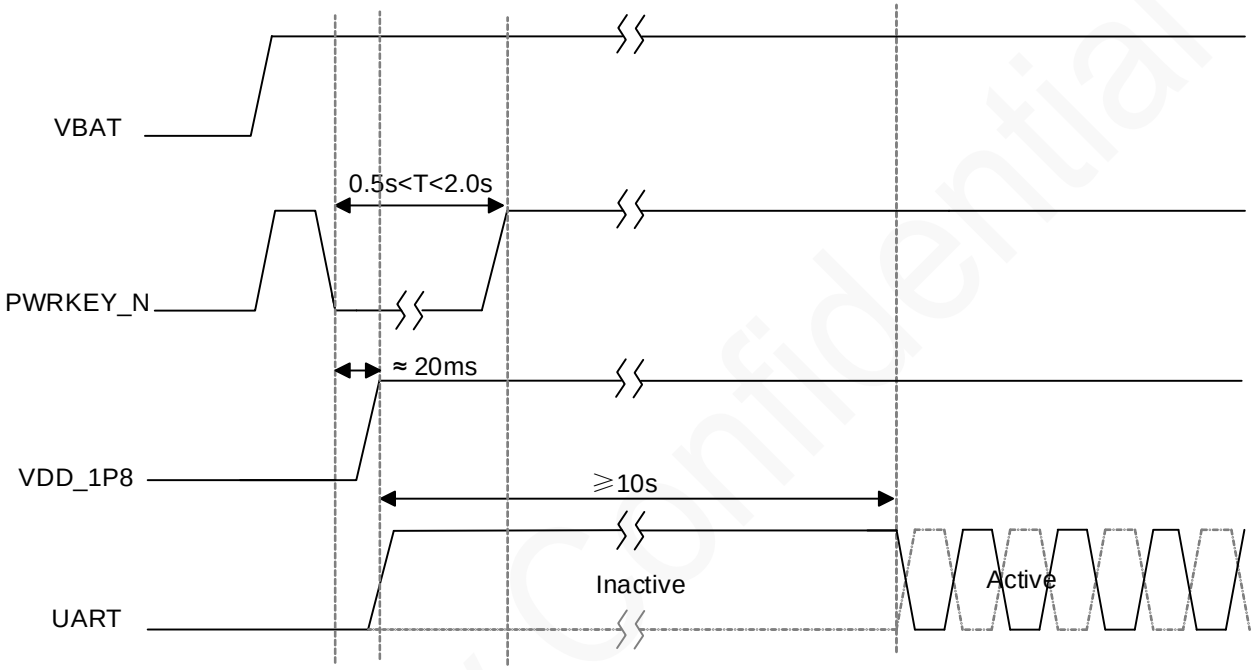
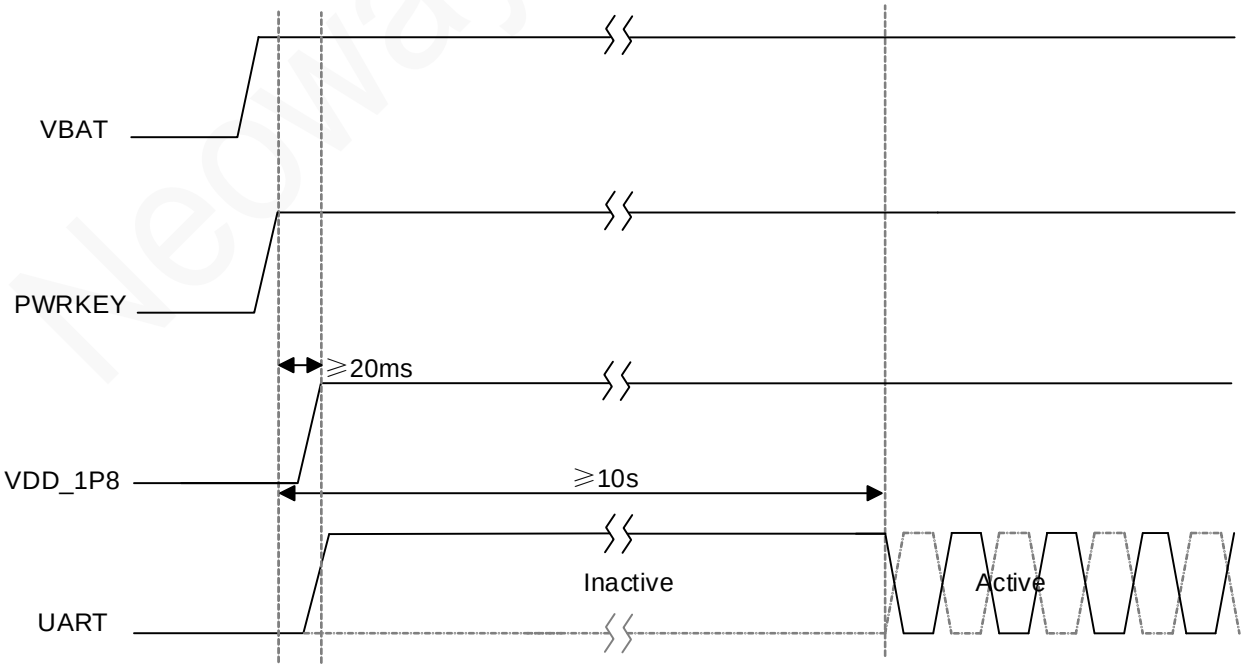


Figure 5-9 PWRKEY startup sequence diagram



After the module is triggered to start, before the startup process is completed, the module needs to be initialized. When VDD_1P8 of the module has voltage output, the UART port cannot communicate normally since its startup process has not been completed yet. The startup time may slightly vary with the module firmware.

5.2.2 Module Shutdown

When the module is working normally, do not directly disconnect the power supply of the module; otherwise, the flash memory (Flash) inside the module may be damaged. It is recommended to shut down the module through PWRKEY_N or AT-command shutdown first, and then disconnect the power supply.

Before implementing the AT-command shutdown, ensure that PWRKEY_N keeps high all the time and PWRKEY keeps low; otherwise, the module will start automatically after the module's shutdown process completes since the power supply is not disconnected.

If the design of automatic startup upon power-up is adopted, then module shutdown can be performed only through turning off the power supply of the module. Then, PWRKEY_N cannot implement shut-down.

When the module is in normal operating state, inputting negative pulses for more than 2s and less than 4s to PWRKEY_N can shut down the module.

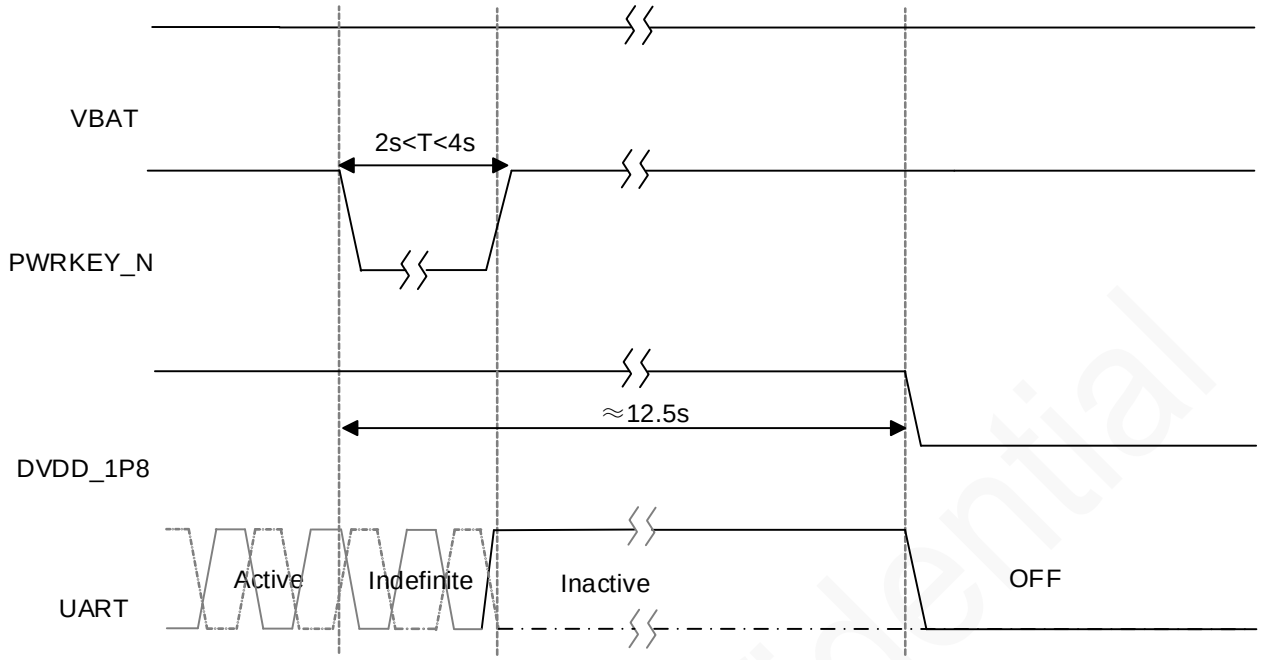
Shutdown process

Two methods are available to shut down the module: hard shutdown and soft shutdown.

For how to shut down the module through software, see *Neoway_N725_AT_Commands_Manual*.

Shutting down the module through hardware can be performed by controlling the PWRKEY_N pin. When the module is in normal operating state, inputting negative pulses for more than 2s and less than 4s to PWRKEY_N can shut down the module. The following figure shows the hardware shutdown process:

Figure 5-10 Hardware shutdown process



When the module executes the shutdown process, VDD_1P8 stops the voltage output after the shutdown process is completed. The low pulse width (shutdown time) needed for PWRKEY_N hard shutdown may slightly vary with the module firmware.

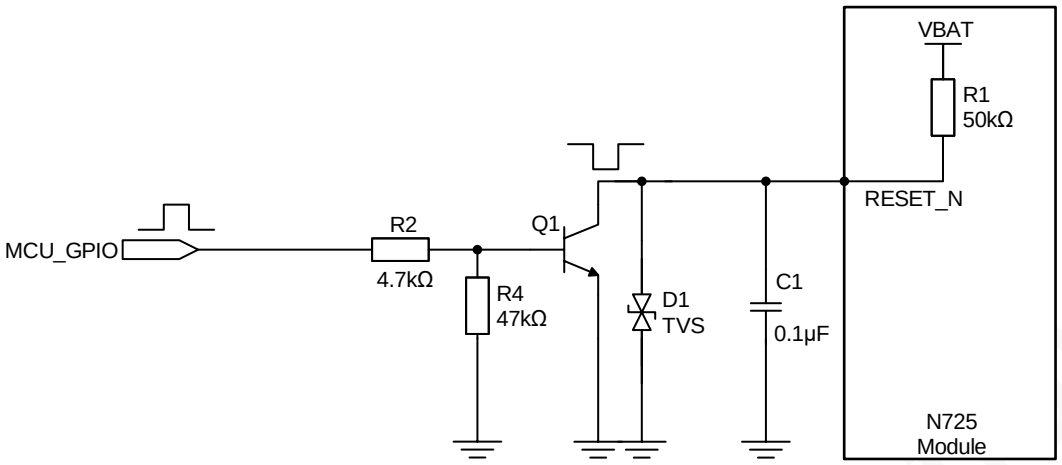
5.2.3 Module Reset

When the module is in normal operating state, inputting a negative pulses for more than 100 ms and less than 500 ms to RESET_N can reset the module. For the reset process, see Figure 5-12.

Notably, when the module crashes, pulling RESET_N down for more than 2s can forcibly reset the module. For the reset process, see Figure 5-13

For the reference design of module reset, see Figure 5-11.

Figure 5-11 Resetting module by inputting pulse



Schematic Design Guideline

Component selection suggestion for Q1: VCE(sat) <=0.2V@IC=50mA

Figure 5-12 Module reset process 1

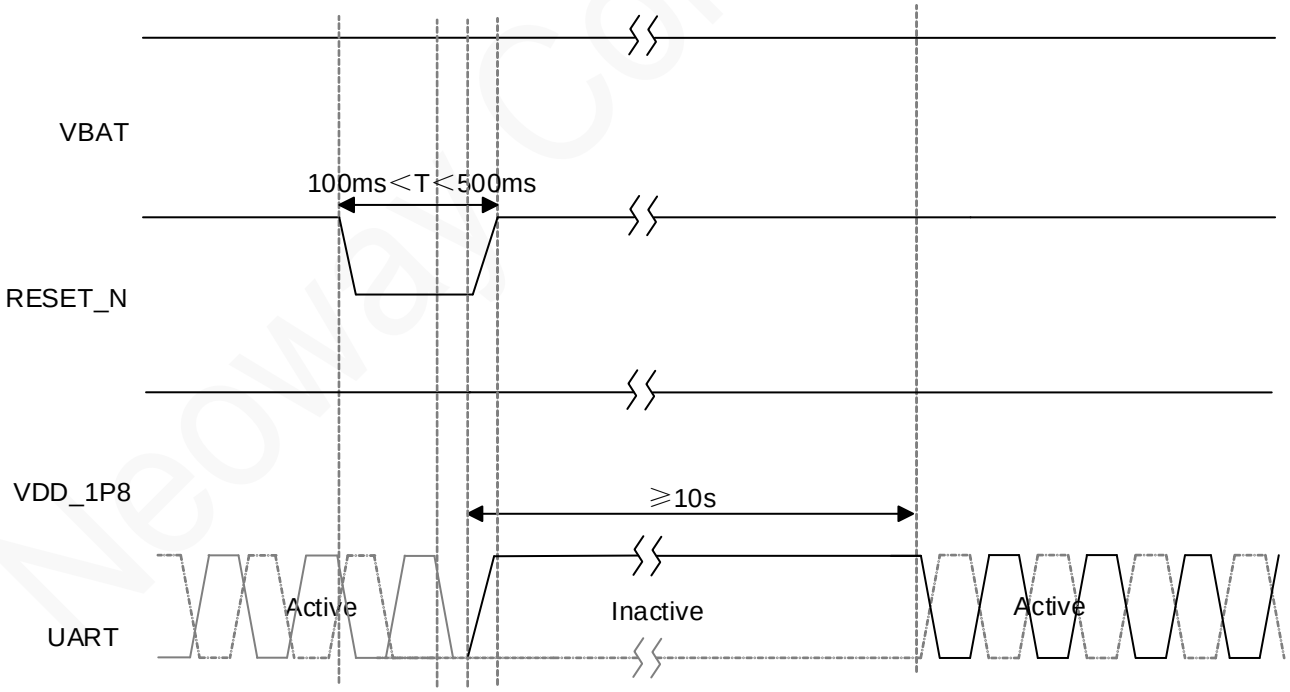
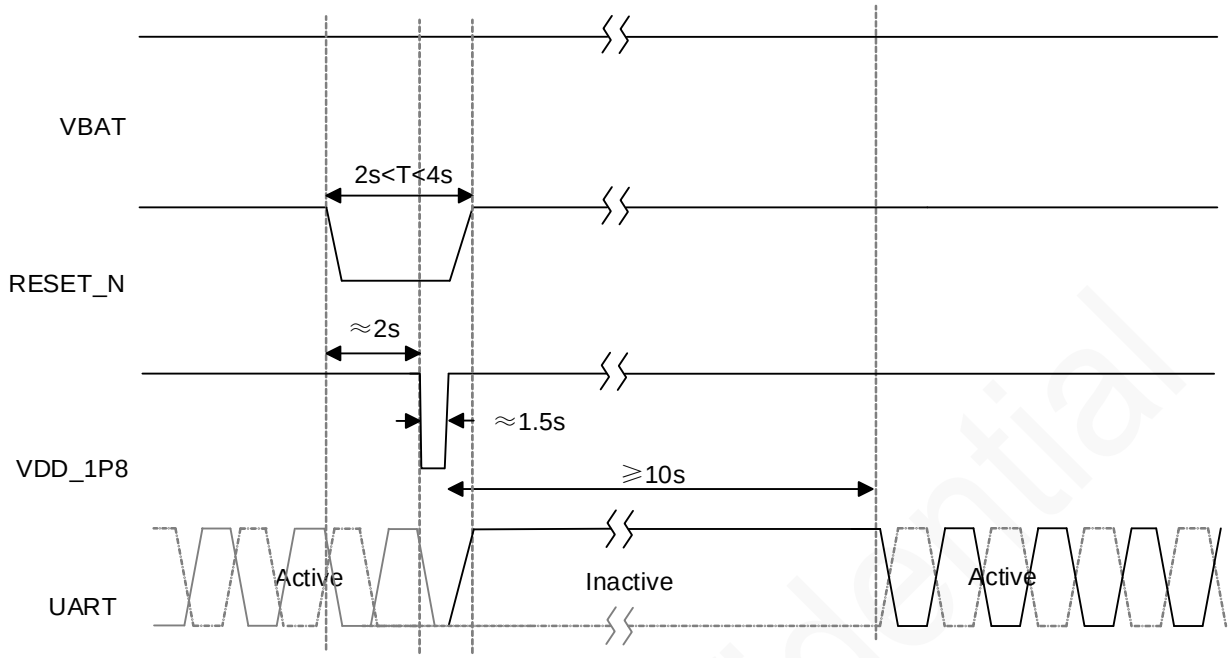


Figure 5-13 Module reset process 2



5.3 Control Interfaces

Signal	Pin	I/O	Function description	Remarks
USB_BOOT	48	DI	Forcible download/upgrade control pin	Pulling down this pin to GND can trigger the module to enter USB download mode. Leave this pin floating if it is not used.
RING	78	DO	Incoming call indicator control	Leave this pin floating if it is not used.
SLEEP	79	DI	Sleep mode control	It controls the sleep mode of the module. Leave this pin floating if it is not used.
NET_LIGHT	83	DO	Network indicator control	Leave this pin floating if it is not used.

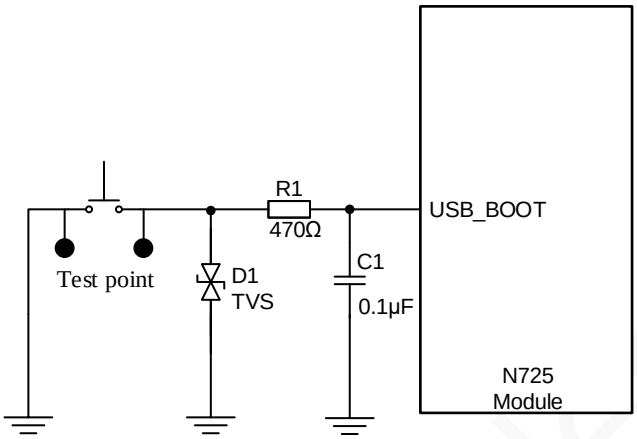
5.3.1 USB_BOOT

It is recommended to reserve test points for the USB_BOOT pin, which is used to enable the module to enter forcible download mode to perform software upgrades.

USB_BOOT is the pin used to forcibly enter the download mode. To enter forcible download mode you can connect USB_BOOT of the module to ground. This is the last method to handle issues that result

in startup or running failures. It is recommended to reserve this pin to facilitate software upgrades and debugging. You can reserve this pin as a button or a test point. The following figure shows the reference design of this pin. Adding an ESD component to protect USB_BOOT in a circuit is required.

Figure 5-14 Reference design of USB force download

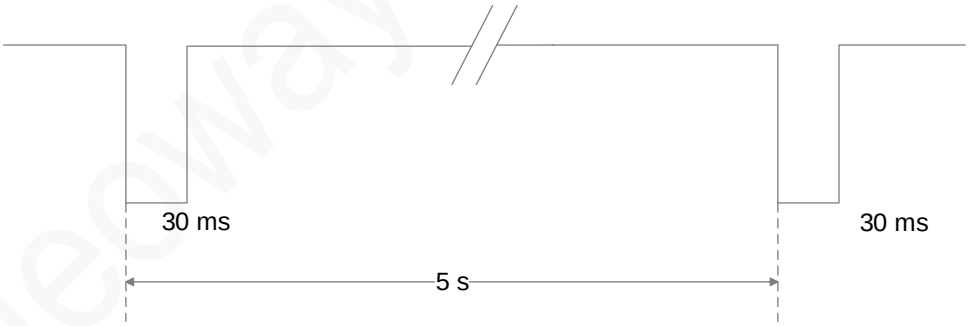


5.3.2 RING

- RING indicator for an incoming call

  Once a voice call is incoming, during the ringing process, the RING pin outputs a negative pulse with a width of 30 ms and a period of 5 seconds. After the call is answered, the pin restores to high-level output, as shown in the following figure.

Figure 5-15 Pulse wave for an incoming call



- RING indicator for SMS

  Upon receipt of an SMS message, the RING pin outputs a negative pulse of 35 ms. As shown in the following figure.

Figure 5-16 RING indicator for SMS

5.3.3 SLEEP

The SLEEP pin is used to control sleep mode of the module, it needs to be used together with the AT commands. For details, see the *Neoway_N725_AT Commands Manual*. In sleep mode, the module can also respond to incoming call, SMS, and data service in time.

The following show the processes:

Figure 5-17 Process of entering sleep mode

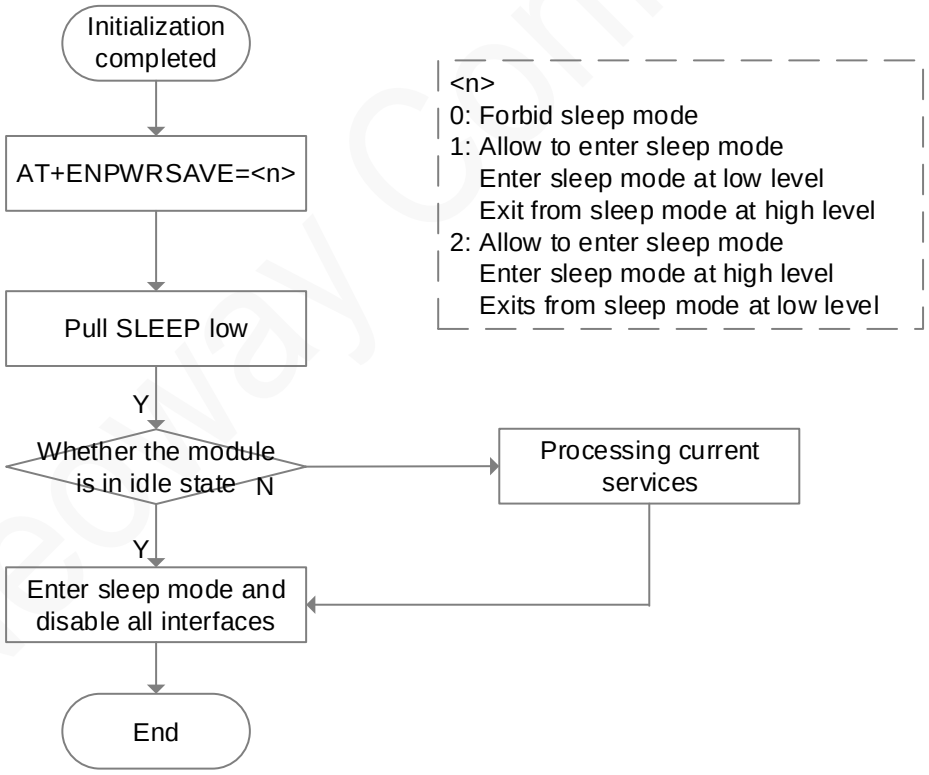


Figure 5-18 Incoming call service process

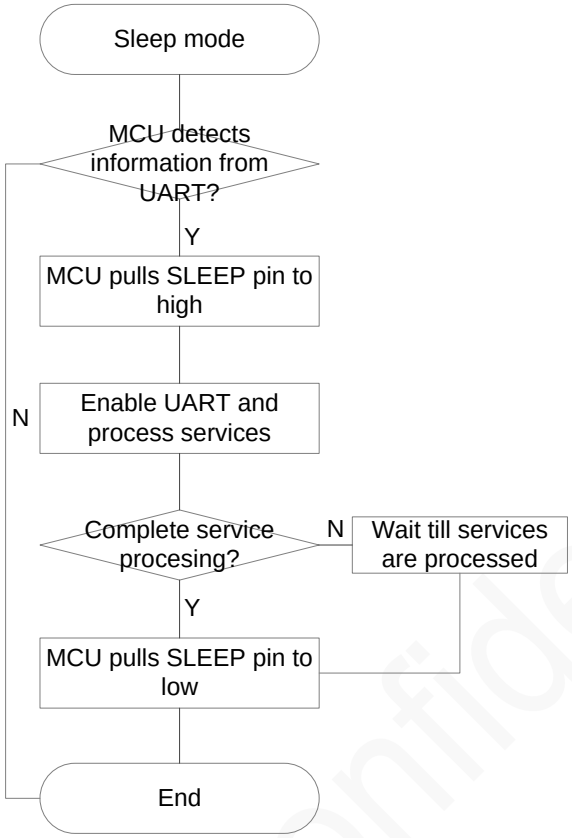


Figure 5-19 Outgoing call service process

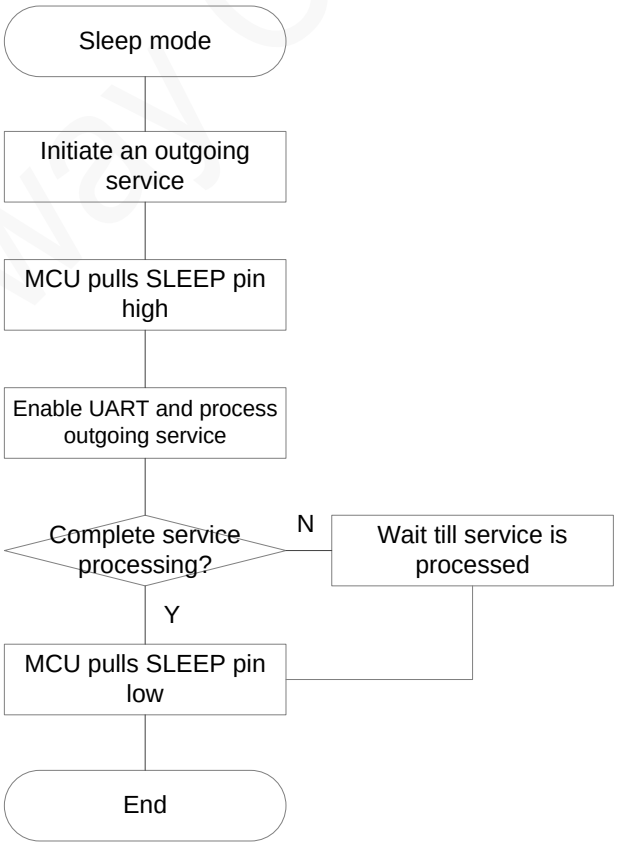
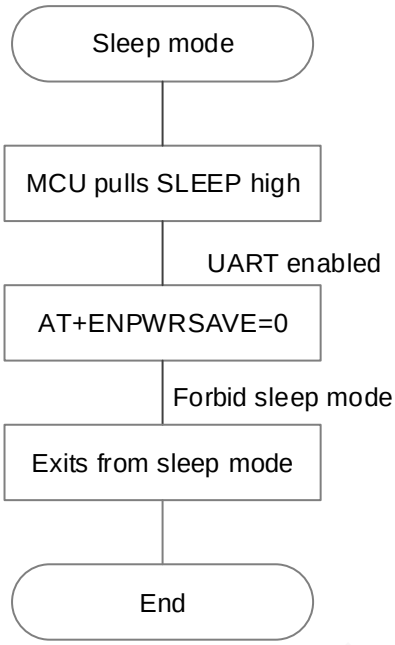


Figure 5-20 Process of existing from the sleep mode

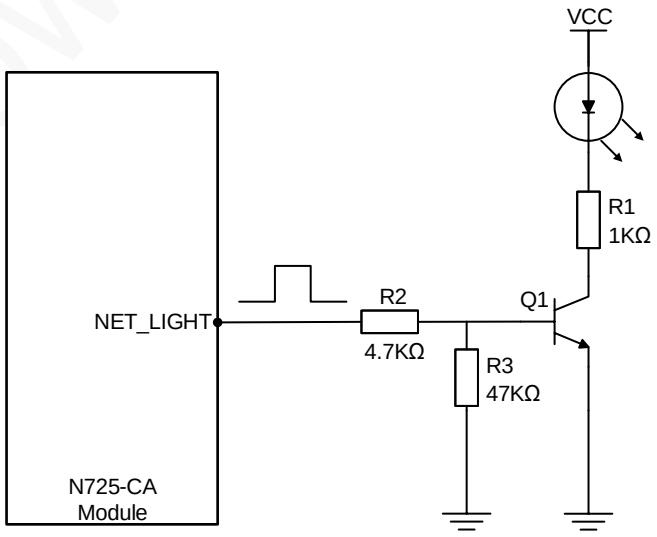


5.3.4 NET_LIGHT

NET_LIGHT is the network status indicator pin of the module. It outputs PMW waves of duty cycle varying with the status of the module and drives an LED indicator to blink at different frequencies. You can use the AT command to enable the LED indicator to blink in different states. For details, see *Neoway_N725_AT_Commands_Manual*.

Do not use NET_LIGHT to drive the LED indicator directly since it outputs a high level of 1.8 V. It is recommended to drive the LED indicator by controlling a triode.

Figure 5-21 Driving LED indicator with a triode



5.4 Peripheral Interfaces

N725 provides various peripheral interfaces.

In all reference designs of this section, the receiving and sending directions included in the pin names of the peripheral interface of the module are based on the module, whereas peripheral pins are named based on the components. For example, UART_TXD indicates the pin used by the module to send data, and MCU_RXD indicates the pin used by the MCU to receive data. These two pins should be connected.

In the process of MCU selection and design, note whether the signal naming of pins is based on the module or the MCU.

5.4.1 USB

The USB_ID and WLAN_EN signals cannot be used simultaneously.

Signal	Pin	I/O	Function description	Remarks
USB_VBUS	40	PI	USB insertion detection pin	USB_VBUS=3.5 V - 5.2 V, typical value: 5.0 V.
USB_DM	41	IO	USB data negative signal	USB 2.0. This pin is used for software download and data transmission. DM and DP adopt differential routing, and the differential impedance must be 90 Ω.
USB_DP	42	IO	USB data positive signal	
USB_ID	43	DI	USB ID pin	Used for OTG function, active high. Putting down this pin can enable The USB device enters master mode after this pin is pulled down.

N725 can implement program download, data communication, and debugging through the USB interface. The module's USB is as a slave device by default and it can be master mode after USB_ID is pulled down.Figure 5-22 and Figure 5-23 show the recommended USB connection circuit.

Figure 5-22 Reference USB connection design

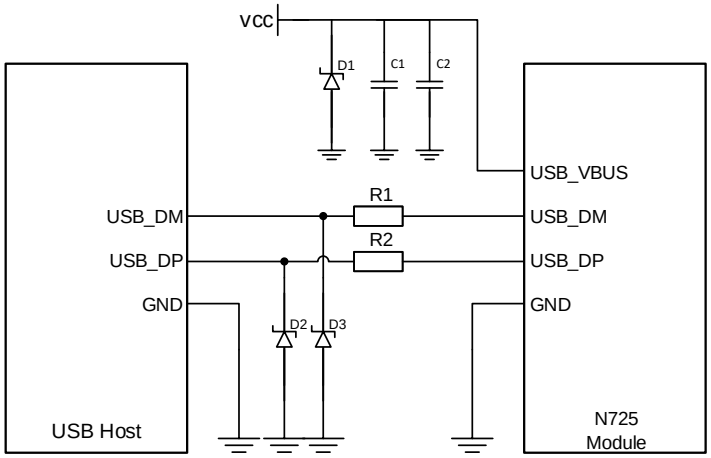
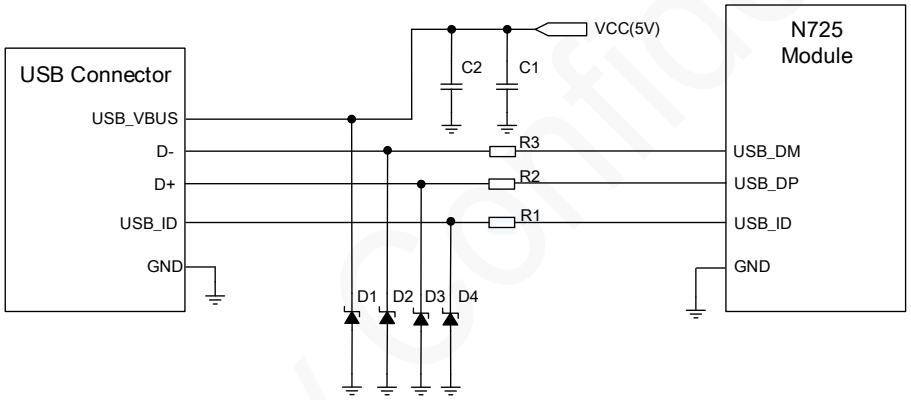


Figure 5-23 Reference USB connection design (with OTG)



Before using the OTG function, please contact Neoway FAEs to confirm whether the module's firmware supports this function.

Schematic Design Guidelines

- Connect a 1 μF (C1) and a 33 pF (C2) filter capacitors in parallel to the USB_VBUS pin. An ESD component must be added for the power cable. The reverse operating voltage (V_{RWM}) should be greater than 6 V.
- The junction capacitance of the ESD components D2 and D3 on the USB_DP and USB_DM data lines must be smaller than 0.5 pF.
- Connecting a resistor less than 10 Ω in series to each of the USB_DP and USB_DM cables can effectively improve the ESD performance of the USB.
- If the USD_ID is used for the OTG function, and it is pulled down, the module is operated in USB master module.

- If there is voltage input on the USB_VBUD pin all the time, the module cannot enter sleep mode; You can add a power switch for USB_VBUS to control it via an external MCU.

PCB Design Guidelines

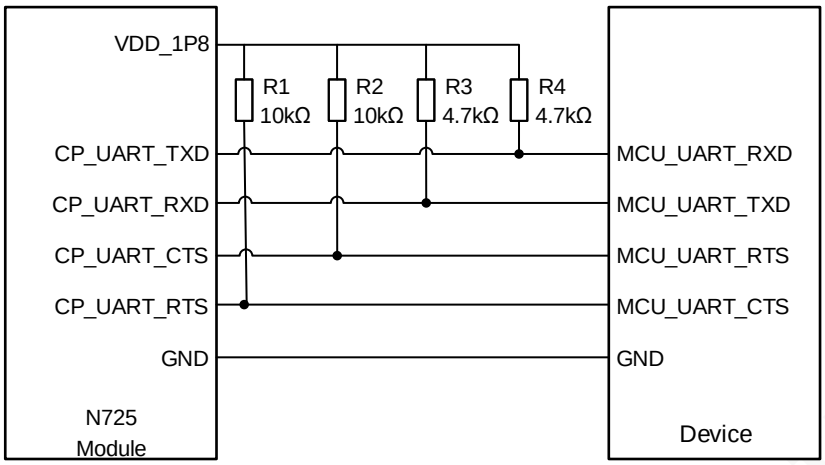
- Place the filter capacitor on the USB_VBUS as close as possible to the module pins, and place the ESD component as close as possible to the USB connector.
- Place the ESD component on the USB_DP and USB_DM as close to the USB connector as possible.
- USB data lines must adopt differential routing, and the differential impedance must be 90 Ω. The cable from the port to the module must be isolated from other signal cables and must be wrapped by ground cables.

5.4.2 UART

Signal	Pin	I/O	Function description	Remarks
DEBUG_UART1_TXD	46	DO	Data transmitting	Used for debug by default. When the device is started, there are outputted log messages. Leave this pin floating when it is not used.
DEBUG_UART1_RXD	47	DI	Data receiving	
CP_UART_TXD	69	DO	Data transmitting	It is used for data transmission and supports hardware flow control. Leave this pin floating if it is not used.
CP_UART_RXD	70	DI	Data receiving	
CP_UART_CTS	84	DI	The user allows the module to send data.	
CP_UART_RTS	87	DO	The module requests the user to send data.	
GNSS_UART2_TXD	85	DO	Data transmitting	N725 does not support GNSS_UART2 by default.
GNSS_UART2_RXD	86	DI	Data receiving	

N725 provides three UART interfaces, of which the CP_UART interface supports hardware flow control and a maximum rate of 3.6 Mbps. DEBUG_UART1 supports baud rates up to 921600 bps. GNSS_UART2 supports baud rates up to 921600 bps. Figure 5-24 shows the reference design of the UART interface. All the UART interfaces of the module are 1.8 V level.

Figure 5-24 Reference design of UART connection



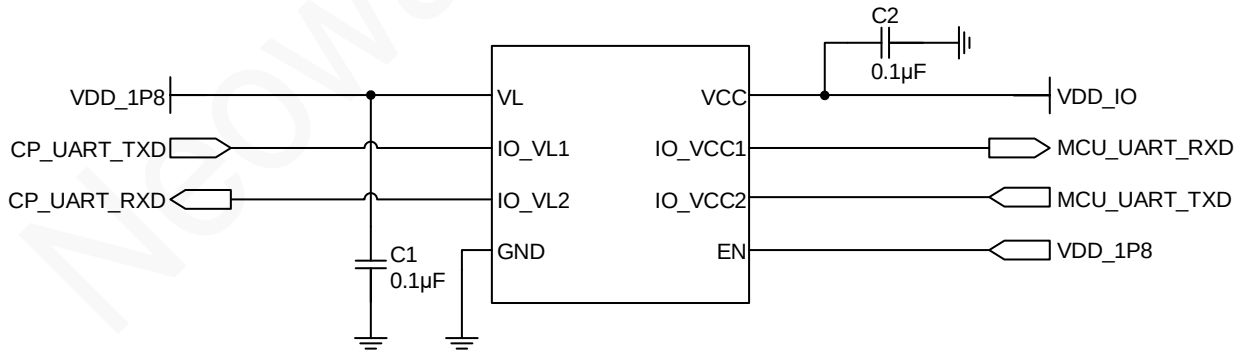
Schematic Design Guidelines

- Pay attention to the corresponding relations between the signal direction and the connection.
- It is prohibited to use diodes for level shifting.

If the UART does not match the logic voltage of the MCU, add a level shifting circuit outside of the module. Three level shifting circuits are recommended based on the differences in logic levels and rates.

- If the serial port baud rate is greater than 115200 bps, it is recommended to refer to the recommended level shifting circuit 1. See Figure 5-25.

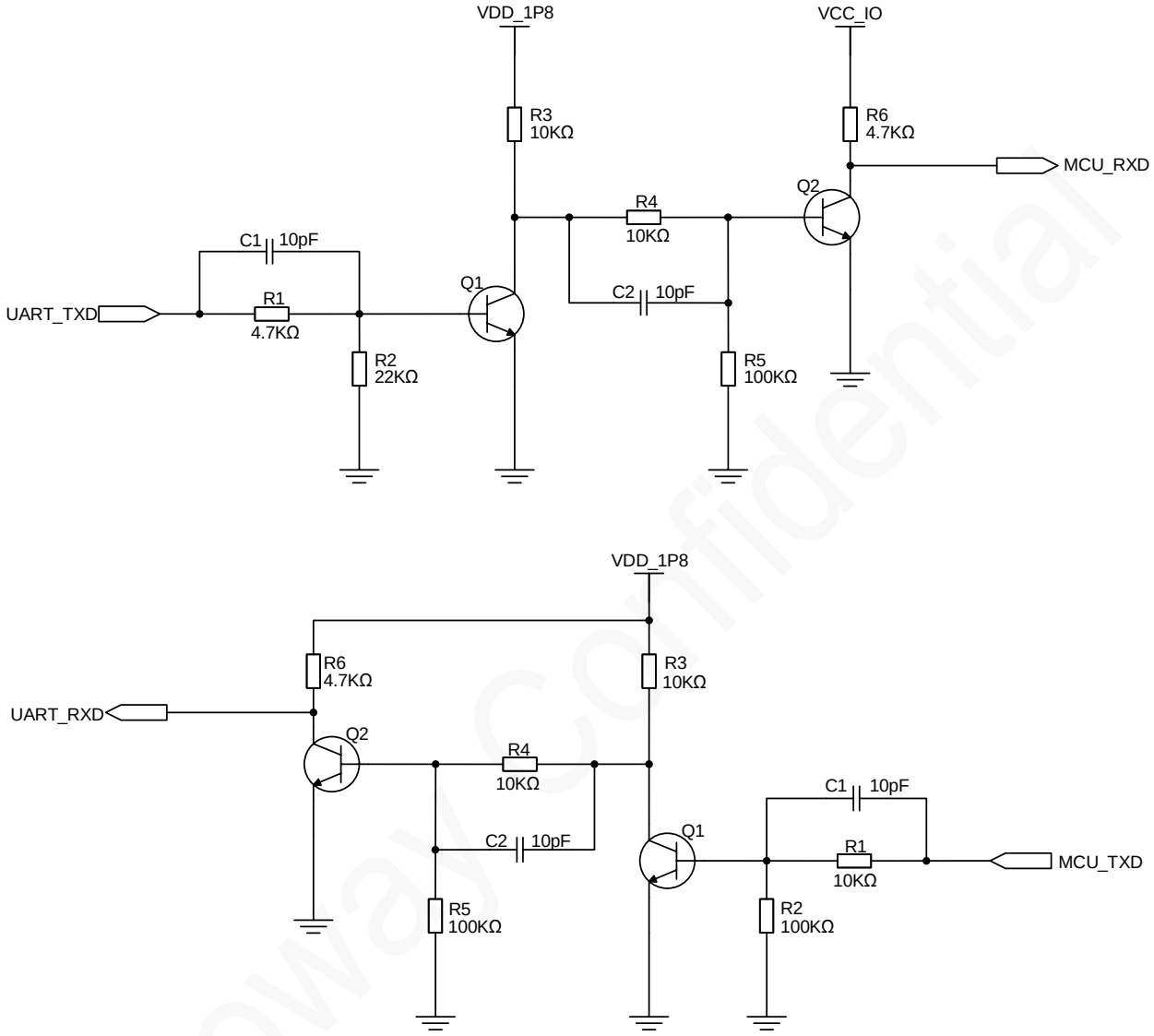
Figure 5-25 Recommended level shifting circuit 1



- VL is the reference voltage of IO_VL1 and IO_VL2.
- VCC is the reference voltage of IO_VCC1 and IO_VCC2.
- EN is the enable pin. In the above circuit, the EN pin is connected to VDD_1P8 and the level shifter is always working.

- If the serial port baud rate is less than or equal to 115200 bps, design the serial port TXD and RXD by referring to recommended level shifting circuit 2. As shown in Figure 5-26.

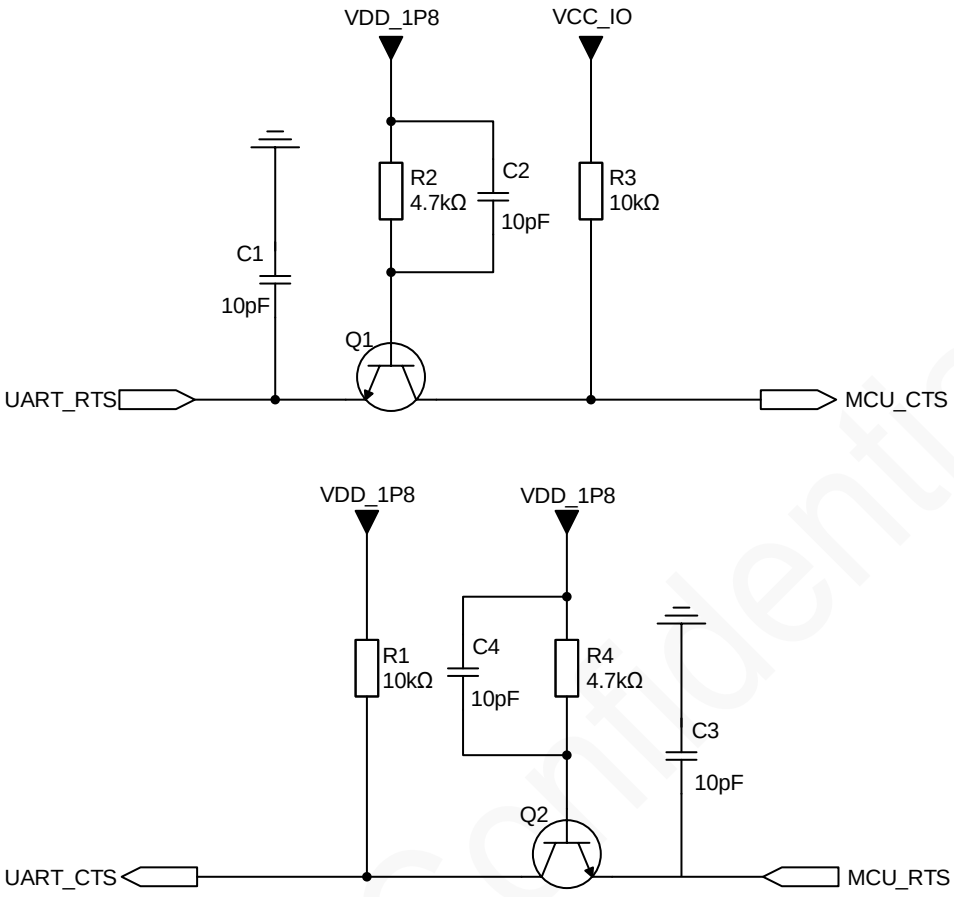
Figure 5-26 Recommended level shifting circuit 2



MCU_TXD and MCU_RXD are the sending and receiving ports of the MCU respectively, and TXD and RXD are the sending and receiving ports of the module respectively. VCC_IO is the IO voltage of the MCU. VDD1V85 is the IO voltage of the module.

- If the serial port baud rate is less than or equal to 115200 bps, design the CTS and RTS circuit by referring to recommended level shifting circuit 3. As shown in Figure 5-27.

Figure 5-27 Recommended level shifting circuit 3



Related components:

- R2/R4: 2 kΩ - 10 kΩ, the higher the working rate of the serial port, the smaller the value of R2/R4.
- R1/R3: 4.7 kΩ - 10 kΩ, the higher the working rate of the serial port, the smaller the value of R1/R3.
- C1 - C4: for the capacitor, it is recommended to select or adjust the capacitance value according to the signal waveform quality of the actual test to improve the signal waveform.

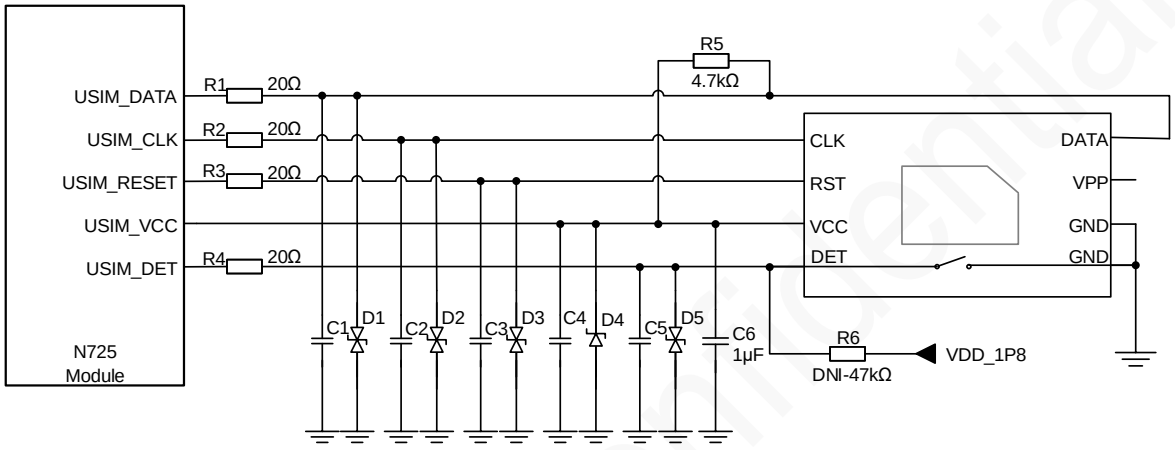
5.4.3 USIM

Signal	Pin	I/O	Function description	Remarks
USIM_VCC	35	PO	USIM power output	1.8 V/3.0 V (self-adaptive)
USIM_DATA	36	B	USIM data input and output	Connecting a 4.7 kΩ pull-up resistor to USIM_VCC is required.
USIM_CLK	37	DO	USIM clock output	Leave this pin floating if it is not used.
USIM_RESET	38	DO	USIM reset	Leave this pin floating if it is not used.

USIM_DET	39	DI	USIM detection	It is recommended to connect this pin to VDD_1P8 through a 47 kΩ pull-up resistor if it is not used.

N725 provides one USIM card interface. Figure 5-28 shows the reference design of the USIM card interface.

Figure 5-28 Reference design of the USIM card interface



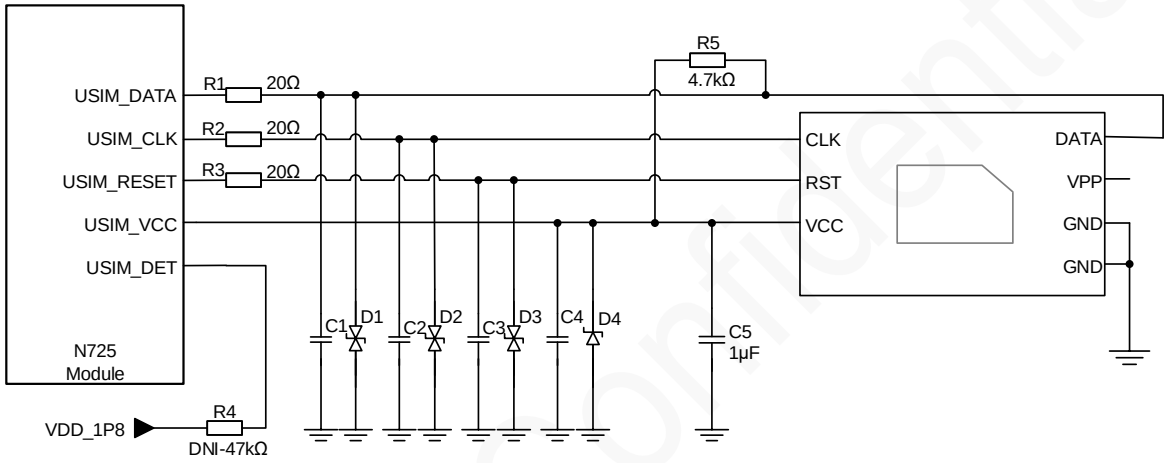
Schematic Design Guidelines

- USIM_VCC is the pin to supply power for USIM card and its maximum load is 50 mA. It is only used as power supply for USIM card (forbidden to supply power to other loads).
- Add a pull-up resistor externally to pull up the USIM_DATA pin to USIM_VCC since there is no internal pull-up on USIM_DATA.
- USIM_CLK is the clock signal pin of the USIM card.
- In applications with complex electromagnetic environments that have high requirements for ESD protection, it is recommended to add ESD protection diodes (junction capacitance ≤ 7 pF) on each signal cable.
- Connect a resistor (not greater than 20 Ω) respectively to USIM_DATA, USIM_RST, USIM_CLK, and USIM_DET (close to the card connector) in series to enhance the ESD performance.
- C1 - C5 are designed to place the high-frequency filter capacitors whose value is not greater than 10 pF.
- Connect a 20 Ω resistor respectively to USIM_DATA, USIM_RST, USIM_CLK, and USIM_DET (close to the module) in series to enhance the ESD performance.

- N725 supports USIM card detection. USIM_DET is a 1.8 V interrupt pin. The USIM detection circuit works by checking the levels across the USIM_DET pin before and after a USIM card is inserted.

Here is the example of a reference design circuit: before a USIM card is inserted, the card connector detection pin is floating, and the USIM_DET pin level is pulled up externally; after a USIM card is inserted, the card connector detection pin is grounded, and the low level at this time indicates that the USIM card is detected, whereas the high level indicates that no USIM card is detected. (In this example, the low level is used to detect the USIM card connector.) If the insertion detection function is not required, refer to Figure 5-29.

Figure 5-29 Reference design of the USIM card (without hot-swap) interface



The SIM card hot-swap function needs to be supported by the corresponding firmware version, and different card connector types have different configurations in firmware. If you require the SIM card hot-swap function, it is recommended to confirm the current configuration of the module firmware with Neoway FAEs.

5.4.4 I2S/PCM

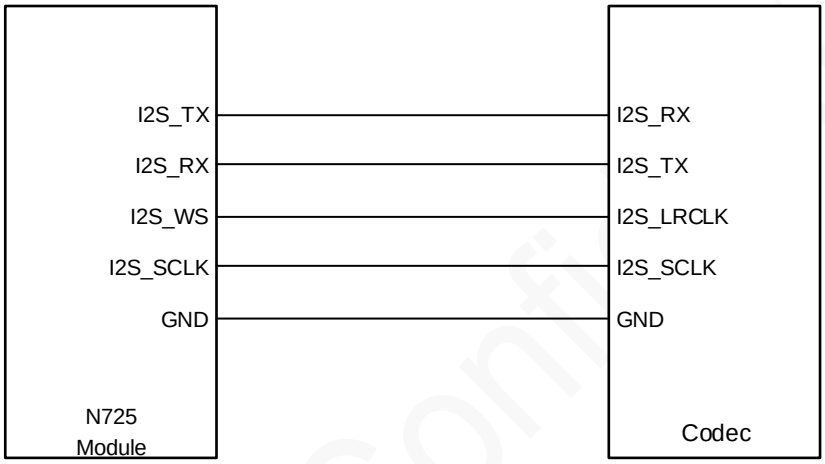
The I2S_MCLK pin has internal pull-up or pull down; do not add a pull-up or pull-down resistor to the pin when it is in use.

Signal	Pin	I/O	Function description	Remarks
I2S_MCLK	64	DO	I2S master clock	The default frequency is 26 MHz.
I2S_WS	65	B	I2S/PCM synchronization signal	Leave this pin floating if it is not used.

I2S_SCLK	66	DO	I2S/PCM data clock	Leave this pin floating if it is not used.
I2S_TX	67	DO	I2S/PCM data sending	Leave this pin floating if it is not used.
I2S_RX	68	DI	I2S/PCM data receiving	Leave this pin floating if it is not used.

N725 provides one PCM/I2S interface, supporting 1.8 V level. The following figure shows the reference design of the PCM interface.

Figure 5-30 PCM reference design



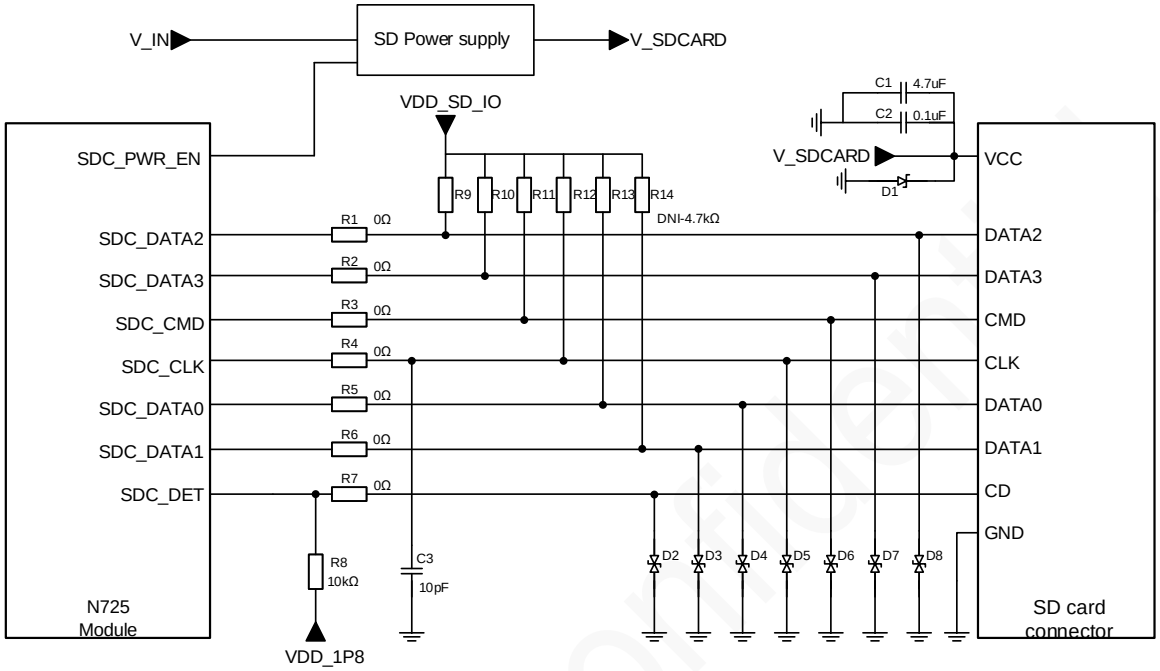
5.4.5 SD/eMMC Interface

Signal	Pin	I/O	Function description	Remarks
SDC_PWR_EN	2	DO	Control of the external power supply for SD/eMMC	Leave this pin floating if it is not used.
SDC_DATA_2	3	B	SD/MMC data 2	Leave this pin floating if it is not used.
SDC_DATA_3	4	B	SD/MMC data 3	Leave this pin floating if it is not used.
SDC_CMD	5	DO	SD/MMC command control	Leave this pin floating if it is not used.
SDC_CLK	6	DO	SD/MMC clock	Leave this pin floating if it is not used.
SDC_DATA_0	7	B	SD/MMC data 0	Leave this pin floating if it is not used.
SDC_DATA_1	8	B	SD/MMC data 1	Leave this pin floating if it is not used.
SDC_DET	96	DI	SD/MMC detect input	Leave this pin floating if it is not used.

N725 provides a SD/eMMC interface, supporting 1.8 V/3.0 V dual voltage. The interface features are as follows:

- Supports SD 3.0 and follows the MMC 4.5.1 standard specifications, with a storage capacity up to 32 GB.
- Supported modes: DS, HS, HS200, SDR12, SDR25, SDR50, SDR104, DDR50.

Figure 5-31 Reference design of the SD card interface



Schematic Design Guidelines

- The SDC_PWR_EN and SDC_DET pins only support 1.8 V level.
- It is recommended to reserve the positions (R9 to R14) for pull-up resistors on the SD/MMC lines.
- When using a SD card not supporting 1.8 V level, change the pull-up power supply of the SD/MMC signal to the corresponding power supply domain.
- Control equal length for the SDC/MMC signal traces.

5.4.6 *PCIe Interface

Signal	Pin	I/O	Function description	Remarks
PCIE_WAKE_IN	54	DI	Input signal for wakeup	Leave this pin floating if it is not used.
PCIE_RST_N	55	DO	Reset output signal	Leave this pin floating if it is not used.
PCIE_CLK_P	122	-	PCIe clock signal positive	Leave this pin floating if it is not used.
PCIE_CLK_N	123	-	PCIe clock signal negative	Leave this pin floating if it is not used.

PCIE_TXP	124	-	PCIe data sending positive	Leave this pin floating if it is not used.
PCIE_TXN	125	-	PCIe data sending negative	Leave this pin floating if it is not used.
PCIE_RXP	126	-	PCIe data receiving positive	Leave this pin floating if it is not used.
PCIE_RXN	127	-	PCIe data receiving negative	Leave this pin floating if it is not used.

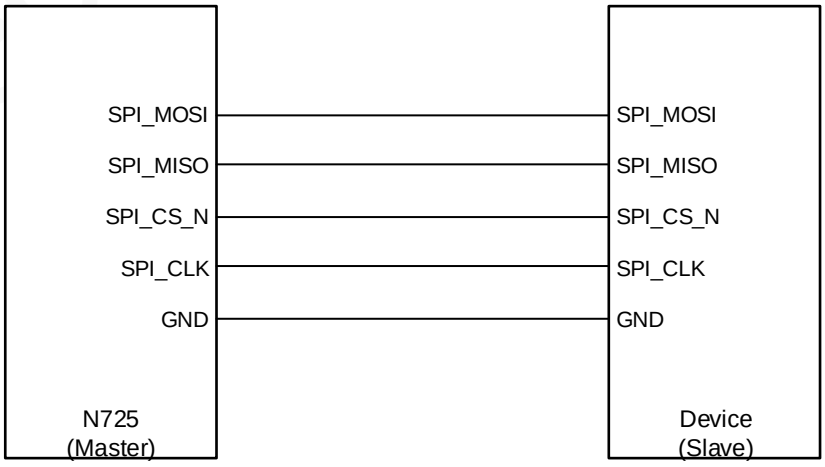
N725 provides one PCIe Gen1 interface and one data channel. It supports RC mode and master mode. Supports speed rates up to 2.5 Gbps theoretically. For the actual maximum rate, refer to the actual test data.

5.4.7 SPI

Signal	Pin	I/O	Function description	Remarks
SPI_CLK	9	DO	Clock signal	Leave this pin floating if it is not used.
SPI_CS_N	10	DI	Chip select signal of the slave device	Leave this pin floating if it is not used.
SPI_MISO	11	DI	Input of the master device and output of the slave device	Leave this pin floating if it is not used.
SPI_MOSI	12	DO	Output of the master device and input of the slave device	Leave this pin floating if it is not used.

N725 provides one SPI interface, which supports only master mode and 1.8 V level. The following figure shows the reference design of the SPI interface.

Figure 5-32 SPI reference design



5.4.8 I2C

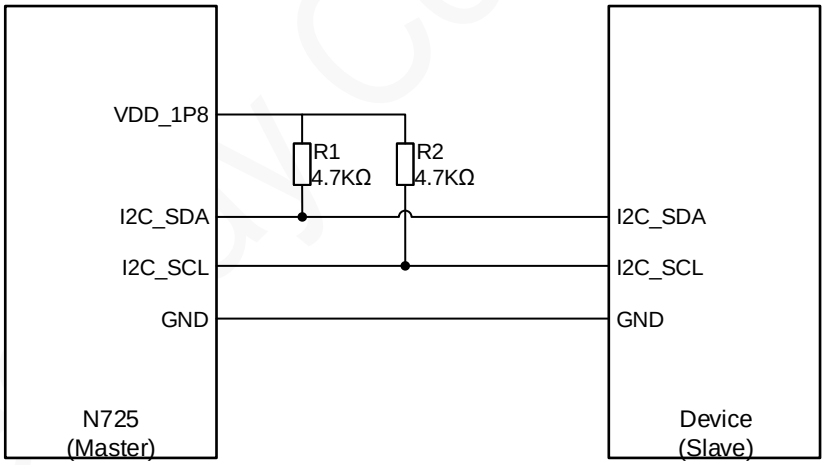
Signal	Pin	I/O	Function description	Remarks
I2C_SDA	81	B	I2C data	Connecting an external 4.7 kΩ pull-up resistor is required.
I2C_SCL	82	DO	I2C clock	Connecting an external 4.7 kΩ pull-up resistor is required.

Table 5-2 I2C interface parameters

IO level	Supported mode	Supported speed
1.8 V	Standard mode	100 kbps
	Fast mode	400 kbps

N725 provides one I2C interface, which supports only master mode and 1.8 V level. There are no internal pull-up resistors. Connecting an external pull-up resistor is required to prevent the lack of I2C drive capability. The following figure shows the reference design of the I2C interface.

Figure 5-33 Reference design of the I2C



Schematic Design Guidelines

If the level of the slave device does not match that of N725, level conversion is required; see Figure 5-25 "Recommended level shifting circuit 1".

PCB Design Guidelines

- Avoid cross routing between the I2C cable and other signal cables as much as possible. If cross-routing cannot be avoided, keep the signal cables perpendicular to other cables to reduce coupling.
- Keep the signal cables away from areas where static electricity may be introduced as much as possible.
- It is recommended that signal cables be wrapped with left and right ground wires.

5.5 Network and Connection

N725 supports Ethernet and Wi-Fi network connection methods.

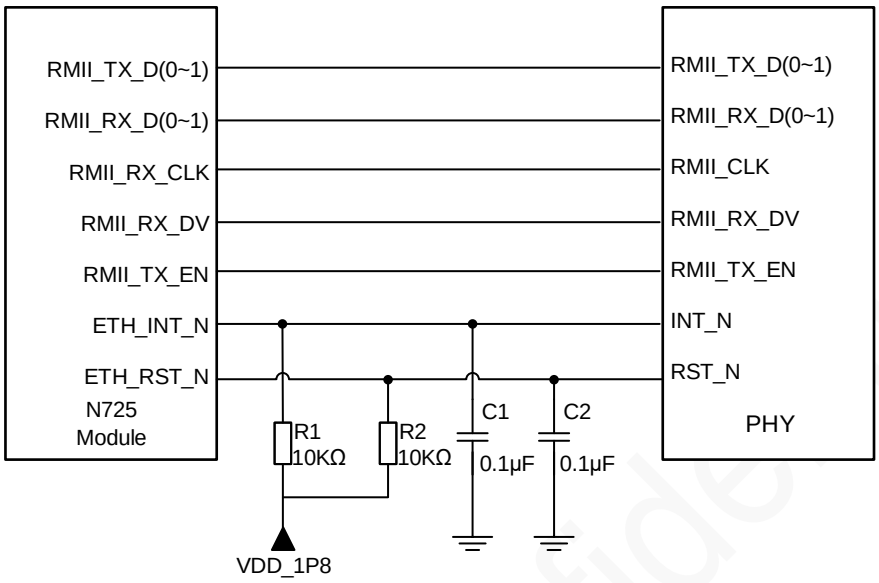
5.5.1 Ethernet

RMII/RGMII

Signal	Pin	I/O	Function description	Remarks
RGMII_RX_D0	19	DI	Data receiving bit 0	Leave this pin floating if it is not used.
RGMII_RX_D1	18	DI	Data receiving bit 1	Leave this pin floating if it is not used.
RGMII_RX_D2	112	DI	Data receiving bit 2	Leave this pin floating if it is not used.
RGMII_RX_D3	113	DI	Data receiving bit 3	Leave this pin floating if it is not used.
RGMII_RX_DV	24	DI	Valid when receiving data	Leave this pin floating if it is not used.
RGMII_RX_CLK	21	DI	Receiving clock	Leave this pin floating if it is not used.
RGMII_TX_D0	16	DO	Data sending bit 0	Leave this pin floating if it is not used.
RGMII_TX_D1	15	DO	Data sending bit 1	Leave this pin floating if it is not used.
RGMII_TX_D2	108	DO	Data sending bit 2	Leave this pin floating if it is not used.
RGMII_TX_D3	109	DO	Data sending bit 3	Leave this pin floating if it is not used.
RGMII_TX_CLK	110	DO	Sending clock	Leave this pin floating if it is not used.
RGMII_TX_EN	13	DO	Enable data sending	Leave this pin floating if it is not used.
ETH_INT_N	25	DI	Interrupt signal input	Leave this pin floating if it is not used.
ETH_RST_N	60	DO	Reset signal output	Leave this pin floating if it is not used.
ETH_PWR_EN	63	DO	Control of enabling the power supply for external PHY chips	Leave this pin floating if it is not used.

The RMII/RGMII multiplexing interface is used for Ethernet connection. RGMII and RMII only support 1.8 V. The following figure shows the reference design of the RMII interface.

Figure 5-34 Reference design of the RMII interface



Schematic Design Guidelines

- Pay attention to the corresponding relationship of the RGMII/RMII connection. Please read the PHY chip manual for details.
- Notably, the RGMII/RMII pin interface is 1.8V. If supporting 3.3 V is required, add the level shifting design.

PCB Design Guidelines

- Control the equal length for the TX and RX traces. For the trace length, refer to the PHY chip manual.
- Control the impedance for the TX and RX traces to 50 Ω. The clock must be wrapped by ground.
- Ensure that the TX and RX trace spacing is larger than 3 times the trace width. Ensure that the RGMII and other trace spacing is larger than 3 times the trace width.

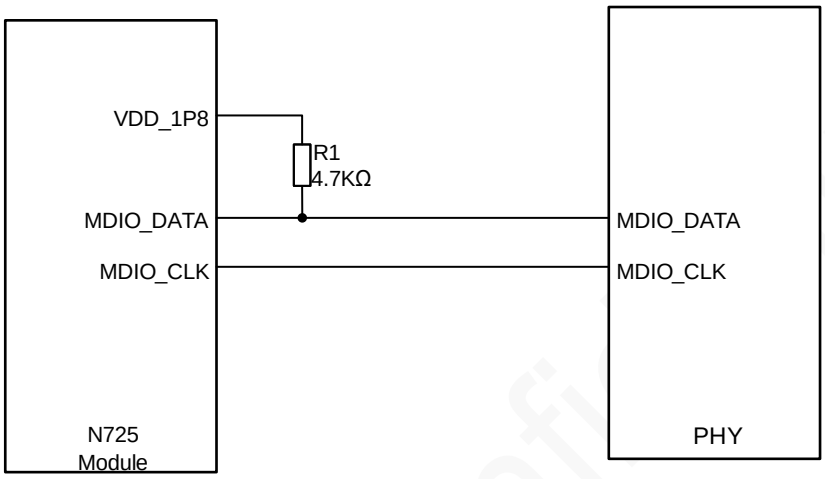
MDIO and PHY

Signal	Pin	I/O	Function description	Remarks
MDIO_CLK	22	DO	MDIO clock	-

MDIO_DATA	23	B	MDIO data	Reserving a position for a 4.7 kΩ pull-up resistor is required.

The following figure shows a reference design of the SDIO interface with a PHY chip:

Figure 5-35 Reference design of the SDIO interface with a PHY chip:



MDIO can control one MAC device or up to 32 PHY devices. With frequencies up to 2.5 MHz it only supports 1.8 V level.

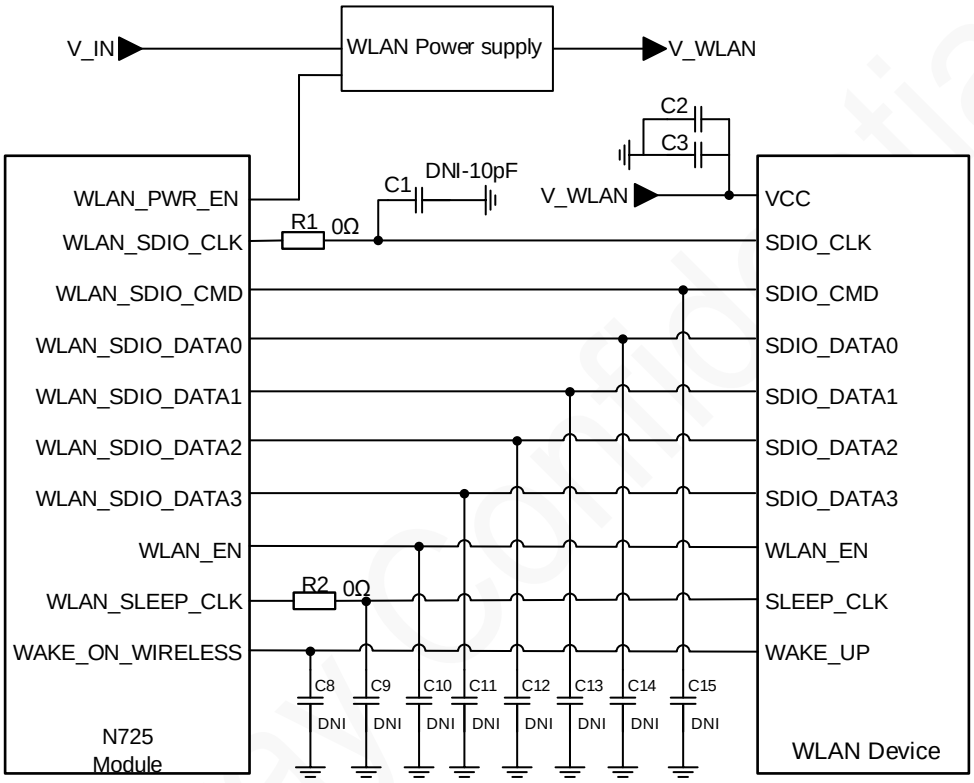
5.5.2 SDIO/WLAN

Signal	Pin	I/O	Function description	Remarks
WLAN_SDIO_CMD	54	B	SDIO command	Leave this pin floating if it is not used.
WLAN_SDIO_CLK	55	DO	SDIO clock	Leave this pin floating if it is not used.
WLAN_SDIO_DATA0	56	B	SDIO data bit 0	Leave this pin floating if it is not used.
WLAN_SDIO_DATA1	57	B	SDIO data bit 1	Leave this pin floating if it is not used.
WLAN_SDIO_DATA2	58	B	SDIO data bit 2	Leave this pin floating if it is not used.
WLAN_SDIO_DATA3	59	B	SDIO data bit 3	Leave this pin floating if it is not used.
WAKE_ON_WIRELESS	60	DO	WLAN wakeup control	Leave this pin floating if it is not used.
WLAN_SLEEP_CLK	61	DO	Wi-Fi sleep clock	Clock frequency: 32 KHz. Leave this pin floating if it is not used.
WLAN_EN	62	DO	WLAN enable control	Leave this pin floating if it is not used.
WLAN_PWR_EN	63	DO	Control of the external power supply for	Leave this pin floating if it is not used.

WLAN

The SDIO interface only supports 1.8 V voltage, supporting SDIO2.0 and SDIO3.0 for Wi-Fi connections. Supports clock frequencies up to SDR 200 MHz or DDR 50 MHz The following figure shows a reference design of the SDIO interface:

Figure 5-36 SDIO reference design



Schematic Design Guidelines

- SDIO of the WLAN chip is a 1.8 V level. If the DATA cable needs to be pulled up, DVDD_1P8 provided by the N725 module can be used for the pull-up power supply.
- The frequency of WLAN_SLEEP_CLK is 32 kHz. If the trace is too long, it is recommended to reserve an RC circuit close to the module.
- It is recommended to reserve an RC circuit on WLAN_SDIO_CLK close to the module. The resistance and capacitance of the RC should be adjusted according to the actual signal quality.
- PCB Design Guidelines
- Control the equal length for the SDIO interface. For the specific equal length requirements, see the requirements of the corresponding WLAN chip or module.

PCB Design Guidelines

- Control the equal length for the SDIO interface. For the specific equal length requirements, see the requirements of the corresponding WLAN chip or module.
- Spacing between DATA traces should be larger than 2 times trace width.
- Control the impedance for each SDIO trace to 50 Ω.

5.6 RF Interface

Signal	Pin	I/O	Function description	Remarks
ANT_MAIN	76	-	2G/3G/4G main antenna pin	50 Ω impedance characteristics
ANT_GNSS	92	-	GNSS antenna	
ANT_DIV	94	-	Diversity antenna pin	

5.6.1 ANT_MAIN/ANT_DIV Antenna Interfaces

The MAIN/DIV antenna interface of the N725 module requires the 50 Ω impedance characteristic. The impedance of the cable from the module interface to the antenna needs to be kept within the impedance range to ensure RF performance. Therefore, you should control the impedance of the traces between the pins and antenna to ensure the RF performance. An impedance matching circuit, such as the L network, split capacitor network, and pi network is mandatory in between. Pi network is recommended.

Figure 5-37 L-type network

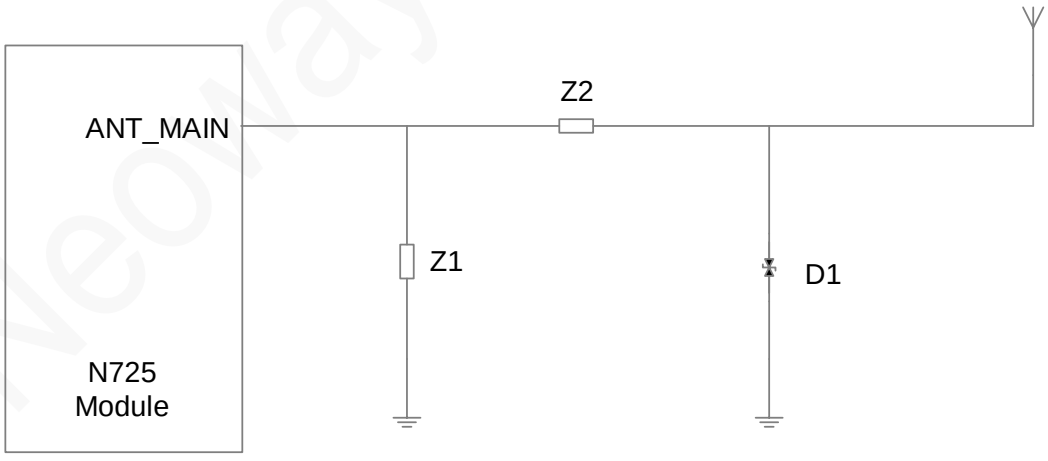


Figure 5-38 T-type network

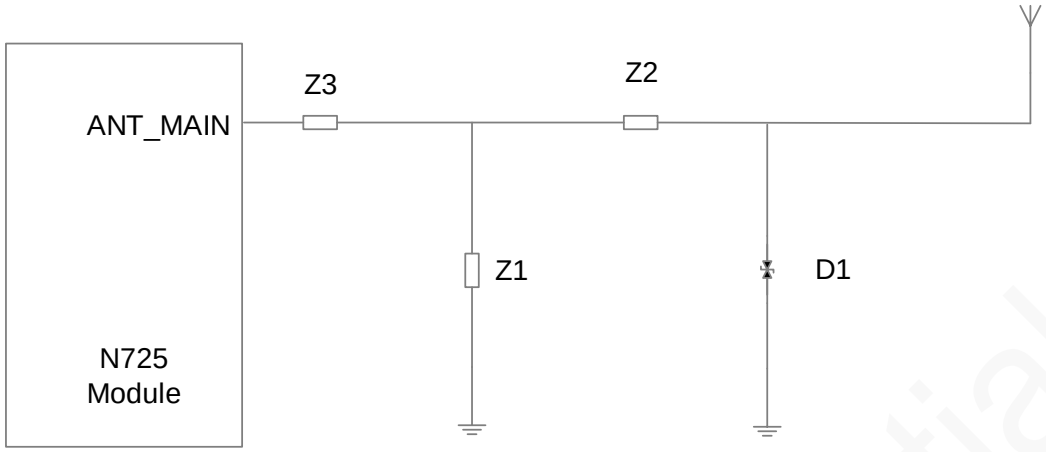
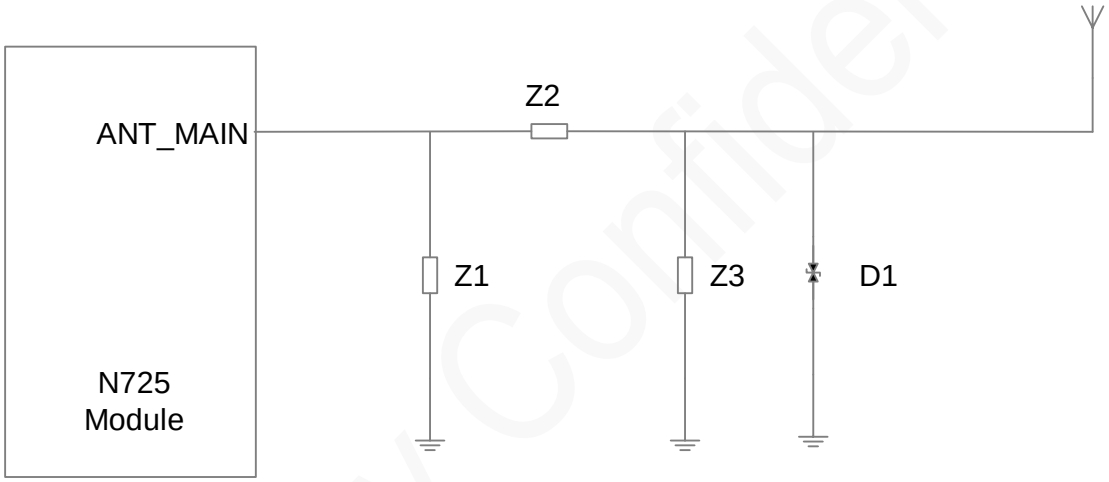


Figure 5-39 π-type network



Schematic Design Guidelines

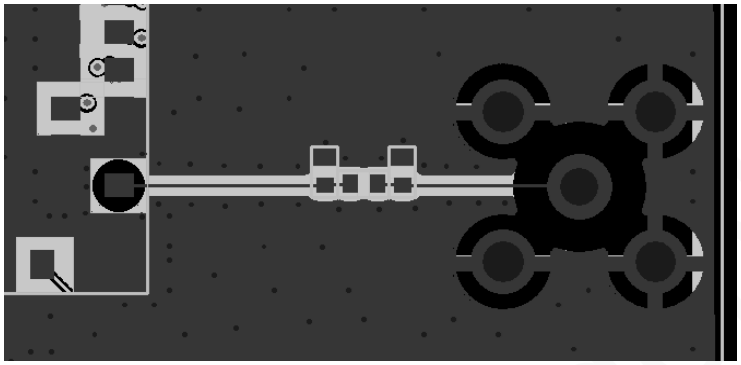
- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- If static electricity is introduced at the antenna, it is recommended that electrostatic protection be added. You can use a TVS tube with ultra-low junction capacitance. It is recommended that you use a TVS tube with a junction capacitance less than 0.5pF. In addition, you must ensure that the reverse breakdown voltage of the TVS tube is greater than 10V. TVS tubes with a reverse breakdown voltage of 15V or more are recommended.

PCB Design Guidelines

- Lay copper foil around the RF connector. Dig as many ground holes as possible on the copper to ensure 50 Ω impedance in the trace.

- The trace between the module pin and the RF lines should be as short as possible. Control the trace impedance to 50 Ω.
- If you adopt an SMA connector, a big RF solder pad might result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and fourth layers or all layers of a multiple-layer PCB under the RF solder pad.

Figure 5-40 Recommended RF PCB design



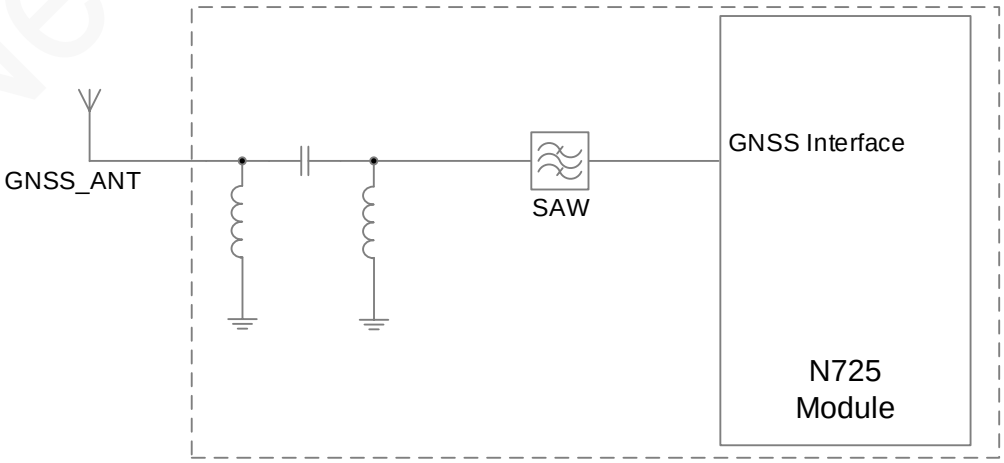
- A reasonable distance should be kept between ANT_MAIN and ANT_DIV to avoid mutual interference that may affect reception performance.
- On the PCB, keep the RF signals and components far away from high-speed circuits, power supplies, transformers, great inductors, the clock, etc.

5.6.2 ANT_GNSS Antenna Interface

GPS Impedance Control

pin 92nd of the N725 module is the GNSS RF interface, which requires a characteristic impedance of 50 Ω. The following figure shows the GNSS structure inside the module.

Figure 5-41 GNSS RF structure



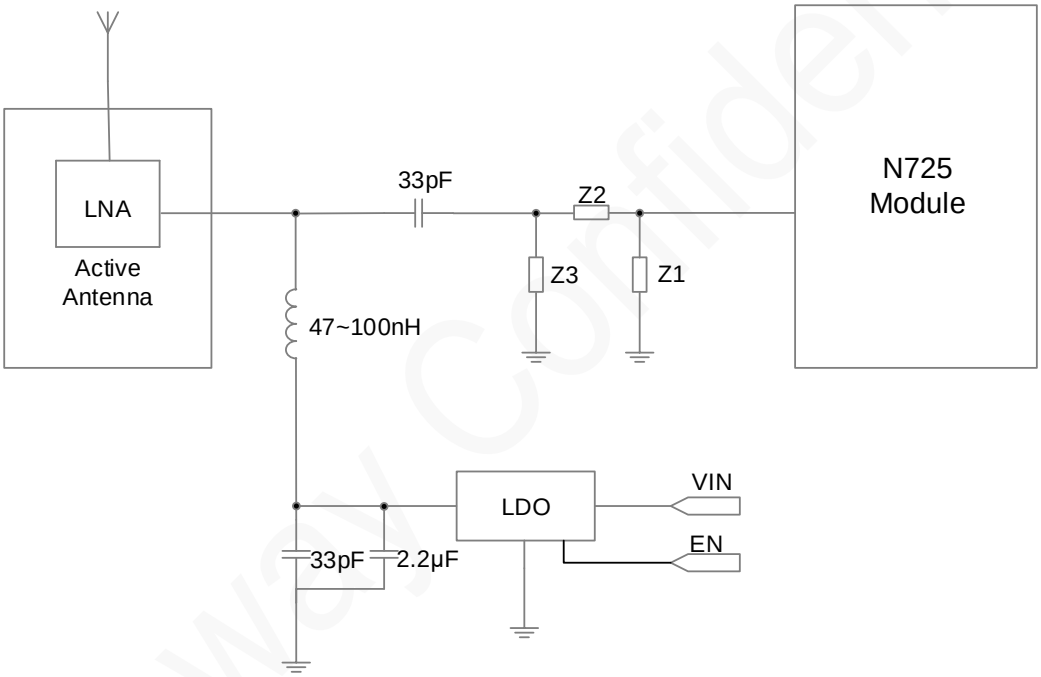
Schematic Design Guidelines

- For the impedance matching circuit between the N725 module and the GNSS antenna, refer to 5.6.1 “ANT_MAIN/ANT_DIV Antenna Interfaces”.
- There is an LNA inside the module; if a passive GNSS antenna is adopted, do not add an LNA.

Reference design of active GNSS antenna

After the antenna receives GNSS satellite signals, the LNA amplifies the signals first and then transmits them to the ANT_GNSS of N725 through feeder and PCB traces. The following figure shows a reference design of the active GNSS antenna.

Figure 5-42 Reference design of the active GNSS antenna



PCB Design Guidelines

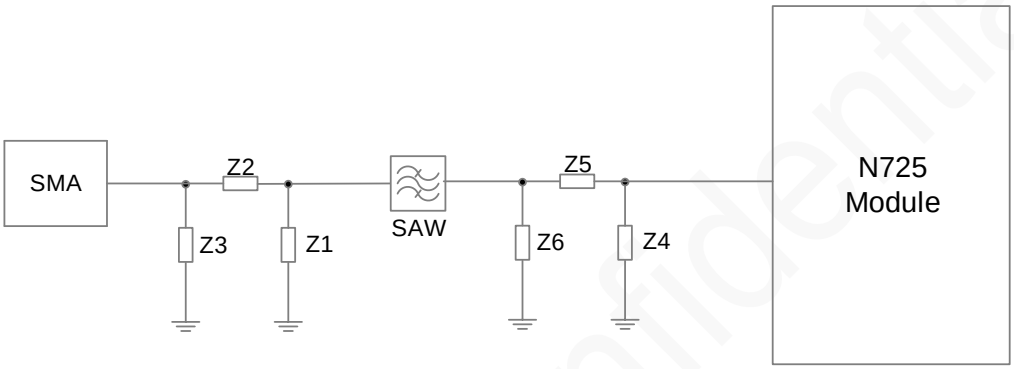
- For cautions of PCB design between GNSS interface and antenna, refer to the PCB design guidelines in 5.6.1 “ANT_MAIN/ANT_DIV Antenna Interfaces”.
- 50 Ω impedance is required for the feeder and PCB traces; Ensure the trace not be too long. The power supply of the active antenna is fed by the 47 nH to 100 nH inductance through the signal traces.
- The common active antenna requires 3.3V to 5V power supply. Though the active antenna is a low power component, it requires a low-noise LDO to supply power for the antenna through a 47 nH to 100 nH inductance.

- Keep the GNSS antenna circuit far away from the main and BT antenna circuits on PCB. Otherwise, these two parts will jam each other, lowing the RF performance.

Reference design of passive GNSS antenna

After the GNSS antenna receives the GNSS satellite signal, it is transmitted to the ANT_GNSS pin of the N725module through the PCB trace. The following figure shows a reference design of the passive GNSS antenna.

Figure 5-43 Reference design of passive GNSS antenna



PCB Design Guidelines

- For cautions of PCB design between GNSS interface and antenna, refer to the PCB design guidelines in 5.6.1 "ANT_MAIN/ANT_DIV Antenna Interfaces".
- Keep the GNSS antenna circuit far away from the main and BT antenna circuits on PCB. Otherwise, these two parts will jam each other, lowing the RF performance.

5.6.3 Antenna Assembling

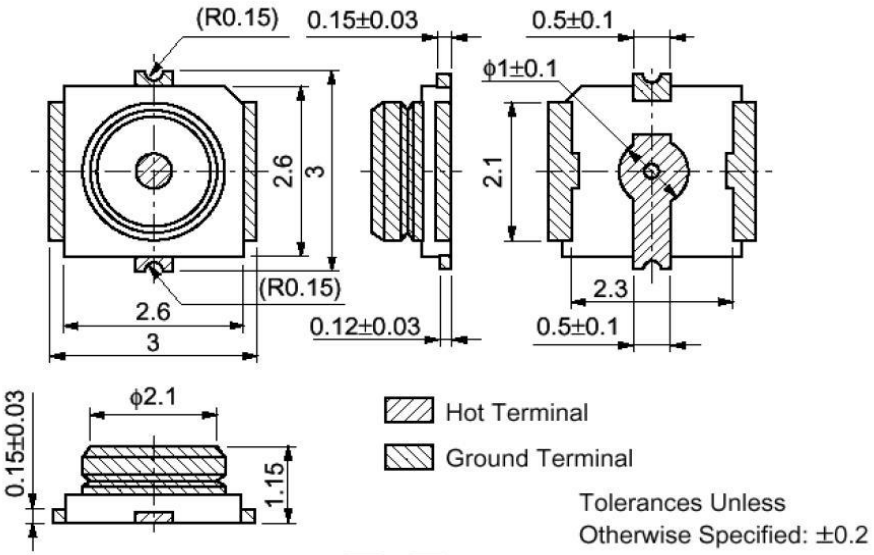
The antenna used by the module must comply with the mobile device standard. The standing wave ratio should be between 1.1 and 1.5, and the input impedance should be 50 Ω. Requirements for antenna gain vary according to the application environment. In general, the greater the in-band gain and the smaller the out-of-band gain, the better the performance of the antenna.

Antenna interfaces can be connected to a rubber ducky antenna, magnet antenna, or embedded Planar Inverted F Antenna (PIFA). Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.

The following methods are commonly used to assemble antenna:

- GSC RF connector
  MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

Figure 5-44 Murata RF connector encapsulation specifications



- The RF cable is connected to the module by means of soldering. However, this method has the stability, consistency, and RF performance degradation issues, and therefore is not recommended.

The following figure shows the effect of the connection methods.

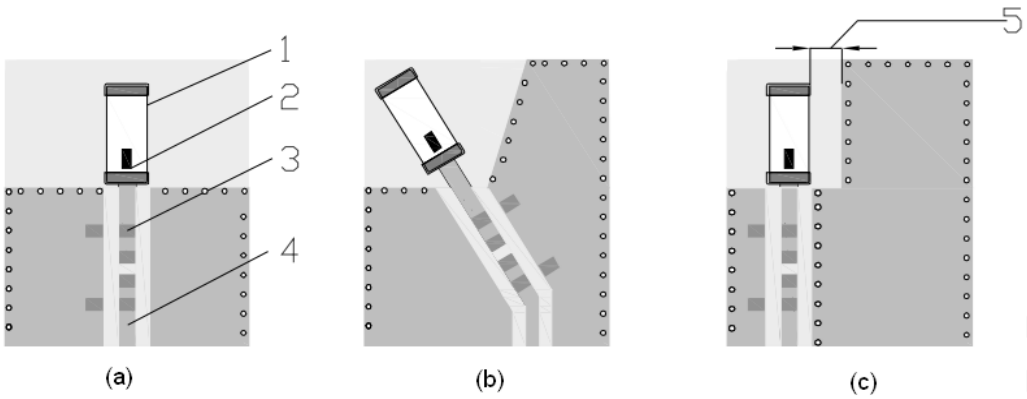
Figure 5-45 RF cable connections

- PCB Printing or SMT

  The module works in a wide frequency range, but it is difficult for PCB antennas or ceramic antennas to cover a wide frequency. Therefore, this connection method is recommended only for 2.4 GHz Wi-Fi or BT/BLE antennas.

The following figure shows the layout of the 2.4 GHz ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

Figure 5-46 Antenna layout

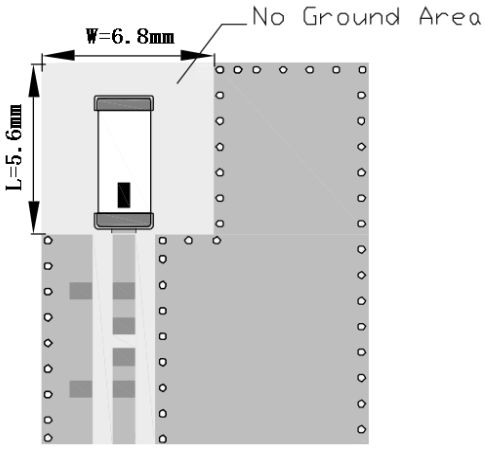


If your PCB is large enough, you can adopt the layout shown in Figure 5-46 (a).

- 1 Chip antenna
- 2 Feeding mark
- 3 Layout pad of the matching circuit
- 4 50 Ω transmission line

Figure 5-47 shows the layout for the area between the antenna and ground that is marked as "5" in Figure 5-46.

Figure 5-47 Layout around the antenna



For more details, refer to the antenna manuals and other documents.

5.7 Multi-Function Interfaces

Table 5-3 Pin definition description

Pin	Function (default)	Multiplexed function 1	Remarks
2	SDC_PWR_EN	GPIO_36	-
19	RGMII_RX_D0	RMII_RX_D0	-
18	RGMII_RX_D1	RMII_RX_D1	-
21	RGMII_RX_CLK	RMII_CLK	RMII_CLK only supports input.
24	RGMII_RX_DV	RMII_RX_DV	-
16	RGMII_TX_D0	RMII_TX_D0	-
15	RGMII_TX_D1	RMII_TX_D1	-
13	RGMII_TX_EN	RMII_TX_EN	-
25	RGMII_INT_N	RMII_INT_N	-
60	WAKE_ON_WIRELESS	ETH_RST_N	-
63	WLAN_PWR_EN	ETH_PWR_EN	-
65	I2S_SYNC	PCM_SYNC	-
66	I2S_BCLK	PCM _CLK	-
67	I2S_DOUT	PCM _DOUT	-
68	I2S_DIN	PCM _DIN	-
84	CP_UART_CTS	GPIO_31	-
87	CP_UART_RTS	GPIO_32	-
54	WLAN_SDIO_CMD	PCIE_WAKE_IN	-
55	WLAN_SDIO_CLK	PCIE_RST_N	-

6 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the N725 module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

6.1 Electrical Characteristics

- If the voltage is lower than threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it outputs at least 2.5A current. The 2.5A current occurs when the module is working at the maximum power level of the GSM mode. The peak current during burst transmission has a short duration. Placing a large capacitor on the VBAT pin of the module can effectively enhance the flyback capability of the power supply and avoid excessive voltage drops that may cause exceptions, such as module shutdown.

Table 6-1 N725 electrical characteristics

Parameter		Minimum Value	Typical Value	Maximum Value
VBAT	V_{in}	3.4 V	3.6 V	4.2 V
	I_{in}	N/A	N/A	2.5 A

Table 6-2 N725 current consumption (Typical)

Status / Network Standard and Band	Sleep (mA)	Idle (DRX) (mA)	Active (mA) @max power
LTE-FDD: B1, B3, B5, B7, B8, B20, B28	≤ 3.0	≤ 20	≤ 650
LTE-TDD: B34, B38, B39, B40, B41	≤ 3.0	≤ 20	≤ 400
B1, B5, B8	≤ 3.0	≤ 20	≤ 560
GSM900	≤ 3.0	≤ 20	≤ 560
GSM1800	≤ 3.0	≤ 20	≤ 400

6.2 Temperature Characteristics

Table 6-3 N725 temperature characteristics

Parameter	Minimum Value	Typical Value	Maximum Value
Operating	-30℃	25℃	75℃
Extended	-40℃	25℃	85℃
Storage	-40℃	25℃	90℃
eCall	-40℃	25℃	90℃

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse but it can still work properly.

6.3 ESD Protection

Electronic products generally need to undergo strict ESD testing. The following details the ESD protection capability of the main pins of the module. When designing related products, you need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25℃

Table 6-4 N725 ESD protection characteristics

Testing point	Contact discharge	Air discharge
GND	±8 kV	±15 kV
ANT	±8 kV	±15 kV
Cover	±8 kV	±15 kV

7 RF Characteristics

N725 supports GSM, WCDMA, FDD-LTE, and TDD-LTE (Cat.4) network modes. This chapter describes the RF characteristics of N725.

7.1 Operating band

Table 7-1 N725 operating bands

Operating band	Uplink	Downlink
EGSM900	880~915MHz	925~960MHz
DCS1800	1710~1785MHz	1805~1880MHz
WCDMA B1	1920~1980MHz	2110~2170MHz
WCDMA B5	824~849MHz	869~894MHz
WCDMA B8	880~915MHz	925~960MHz
FDD-LTE B1	1920~1980MHz	2110~2170MHz
FDD-LTE B3	1710~1785MHz	1805~1880MHz
FDD-LTE B5	824~849MHz	869~894MHz
FDD-LTE B7	2500~2570MHz	2620~2690MHz
FDD-LTE B8	880~915MHz	925~960MHz
FDD-LTE B20	832~862MHz	791~821MHz
FDD-LTE B28	703~748MHz	758~803MHz
TDD-LTE B34	2010~2025MHz	2010~2025MHz
TDD-LTE B38	2570~2620MHz	2570~2620MHz
TDD-LTE B39	1880~1920MHz	1880~1920MHz
TDD-LTE B40	2300~2400MHz	2300~2400MHz
TDD-LTE B41	2535~2655MHz	2535~2655MHz

7.2 TX Power and RX Sensitivity

Table 7-2 N725 RF transmit power

Band	Max power	Min. power
EGSM900	33 dBm±2.7 dB	5 dBm±5 dB
DCS1800	30 dBm±2.7 dB	5 dBm±5 dB
WCDMA B1	24 dBm+1/-3 dB	< -50 dBm
WCDMA B5	24 dBm +1/-3 dB	< -50 dBm
WCDMA B8	24 dBm +1/-3 dB	< -50 dBm
FDD LTE B1	23 dBm±2.7 dB	< -39 dBm
FDD LTE B3	23 dBm±2.7 dB	< -39 dBm
FDD LTE B5	23 dBm±2.7 dB	< -39 dBm
FDD LTE B7	23 dBm±2.7 dB	< -39 dBm
FDD LTE B8	23 dBm±2.7 dB	< -39 dBm
FDD LTE B20	23 dBm±2.7 dB	< -39 dBm
FDD LTE B28	23 dBm±2.7 dB	< -39 dBm
TDD LTE B34	23 dBm±2.7 dB	< -39 dBm
TDD LTE B38	23 dBm±2.7 dB	< -39 dBm
TDD LTE B39	23 dBm±2.7 dB	< -39 dBm
TDD LTE B40	23 dBm±2.7 dB	< -39 dBm
TDD-LTE B41	23 dBm±2.7 dB	< -39 dBm

Table 7-3 GSM RX sensitivity of N725

Band	Receiving sensitivity
EGSM900	≤ -102 dBm
DCS1800	≤ -102 dBm

Table 7-4 WCDMA receiving sensitivity

Band	Receiving sensitivity
WCDMA B1	≤ -106.7 dBm
WCDMA B5	≤ -104.7 dBm

WCDMA B8	≤ -103.7 dBm

Table 7-5 LTE RX sensitivity of N725

Band	Receiving sensitivity	Duplex mode
LTE B1	≤ -96.3 dBm	FDD
LTE B3	≤ -93.3 dBm	FDD
LTE B5	≤ -94.3 dBm	FDD
LTE B7	≤ -94.3 dBm	FDD
LTE B8	≤ -94.3 dBm	FDD
LTE B20	≤ -93.3 dBm	FDD
LTE B28	≤ -94.8 dBm	FDD
LTE B34	≤ -96.3 dBm	TDD
LTE B38	≤ -96.3 dBm	TDD
LTE B39	≤ -96.3 dBm	TDD
LTE B40	≤ -96.3 dBm	TDD
LTE B41	≤ -94.3 dBm	TDD

The preceding indicators are tested in a shielded environment in the laboratory. The LTE band indicators are the test results when the bandwidth is 10 MHz, the modulation mode is QPST and RB is set according to the protocol. On no-shielded environments, deviations may exist in the receiver sensitivity of some individual bands due to the interference.

7.3 GNSS Technical Parameters

Table 7-6 GNSS technical parameters

Parameter	Notice
GPS L1 operating frequency	1575.42±1.023 MHz
GLONASS operating frequency	1597.5 - 1605.9 MHz
BDS operation frequency	1559.1 - 1563.1 MHz
Tracking sensitivity	-160 dBm
Acquisition sensitivity	-156 dBm
Positioning precision (in air)	< 3 m (CEP50)

Hot start (in air)	
Cold start (in air)	<33 s
Update frequency	
Max. positioning altitude	18000 m
Max. positioning speed	515 m/s
Max. positioning acceleration	1G
CNRin/CNRout	3 dB
GNSS data type	NMEA-0183
GNSS data type	Passive/active antenna

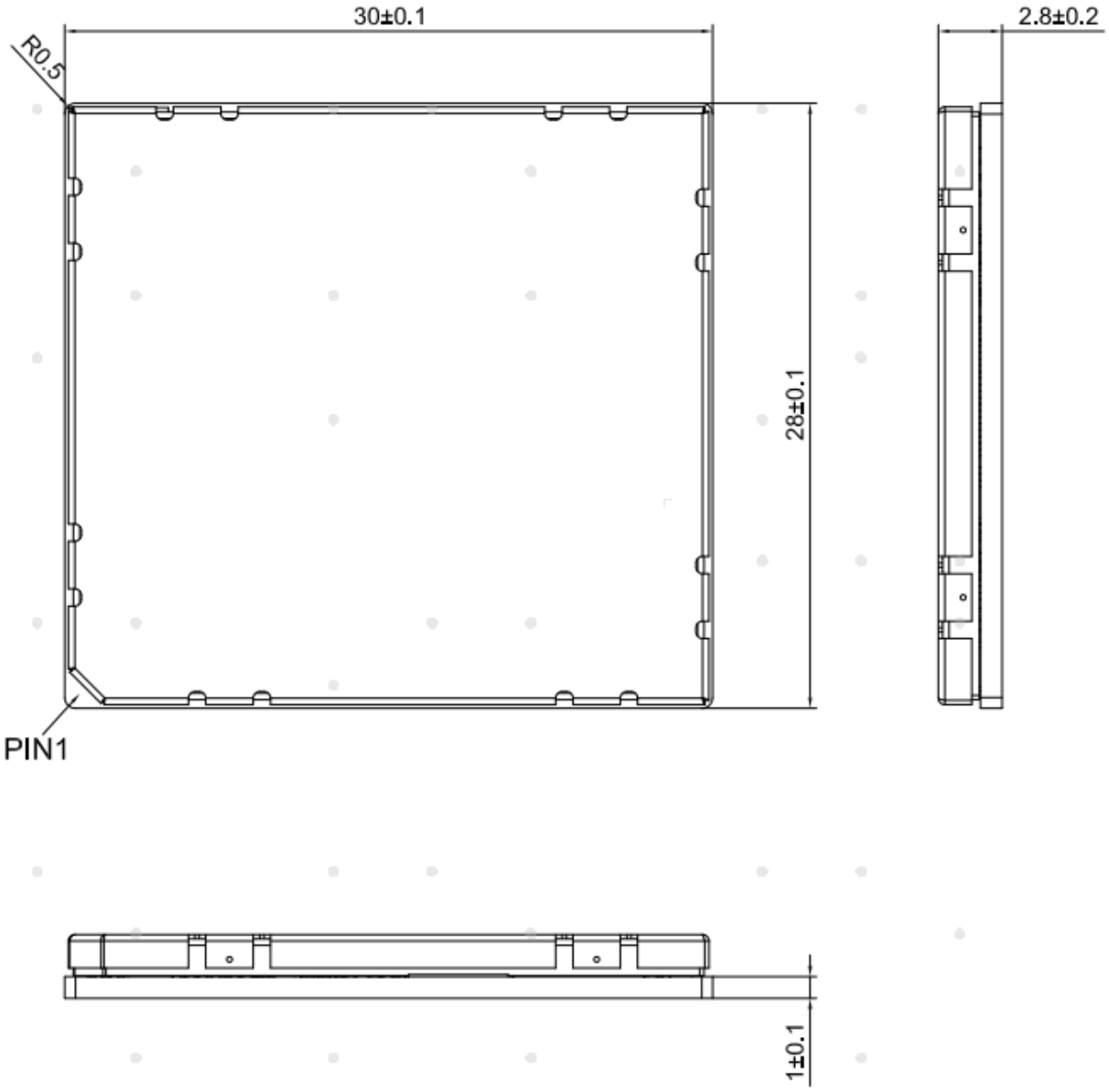
The tracking sensitivity and recapture sensitivity are obtained from the signaling test on SPIRENTGSS7000. The values are the maximum values obtained from multiple measurements performed on samples. No external LNA, active antenna, or other signal amplification measures are used during the test.

8 Mechanical Characteristics

This chapter describes mechanical characteristics of the N725 module.

8.1 Dimensions

Figure 8-1 N725 dimensions (unit: mm)



8.2 Label

The label information is laser carved on the cover. The following figure shows the label of N725.

Figure 8-2 N725 label

The picture above is only for reference.

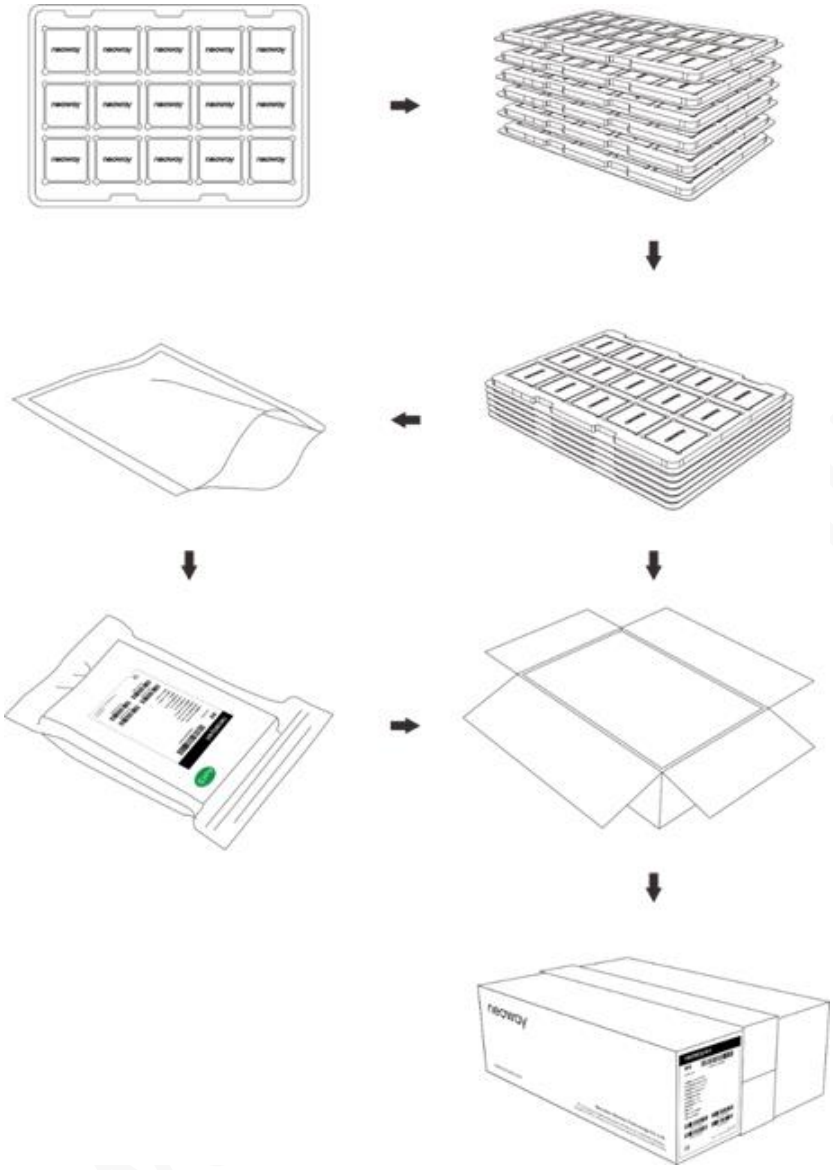
8.3 Packing

The N725 module adopts the SMT method for oven soldering. To prevent the products from being damped before they are delivered to customers, use the tray for moisture-proof packaging and use the aluminum foil bag, desiccant, humidity indicator card, tray, vacuum and other processing methods to ensure the dryness of the product and extend its service life.

8.3.1 Tray

The mass-produced module is packed and shipped using the following tray method:

Figure 8-3 Packing process



The picture above is only for reference.

8.3.2 Moisture

N725 is a level 3 moisture-sensitive electronic element, in compliance with IPC/JEDEC J-STD-020 standard.

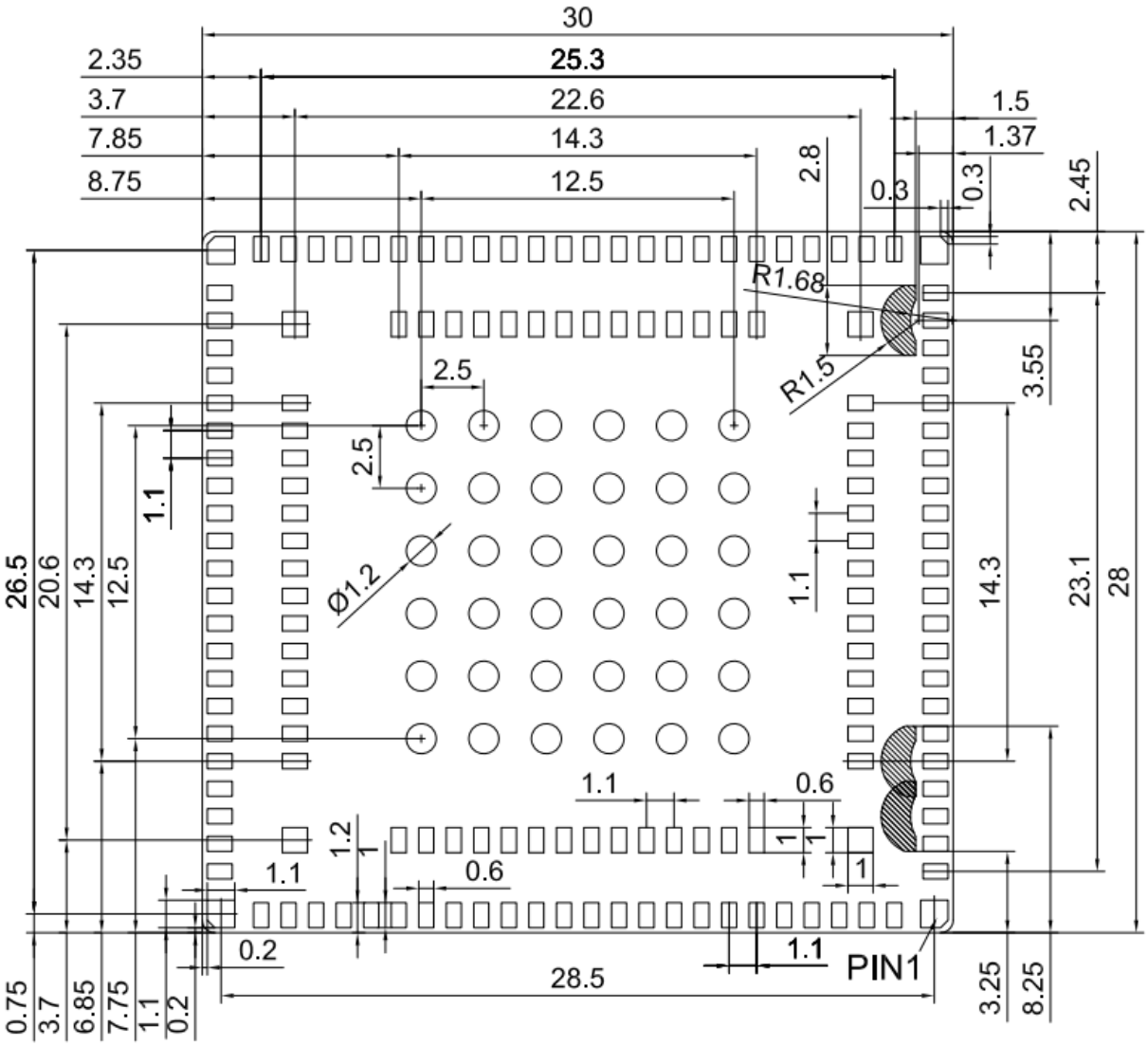
After the module is unpacked, if it is exposed to the air for a long time, the module will get damped, and may be damaged during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at a temperature higher than 90 degrees for more than 12 hours. In addition, since the package tray is made of non-high temperature resistant material, do not bake modules with the tray directly.

9 Mounting

This chapter describes the module PCB package and application PCB package of N725, as well as the key points of SMT related technology.

9.1 PCB Package

Figure 9-1 Bottom view of N725 PCB package (unit: mm)

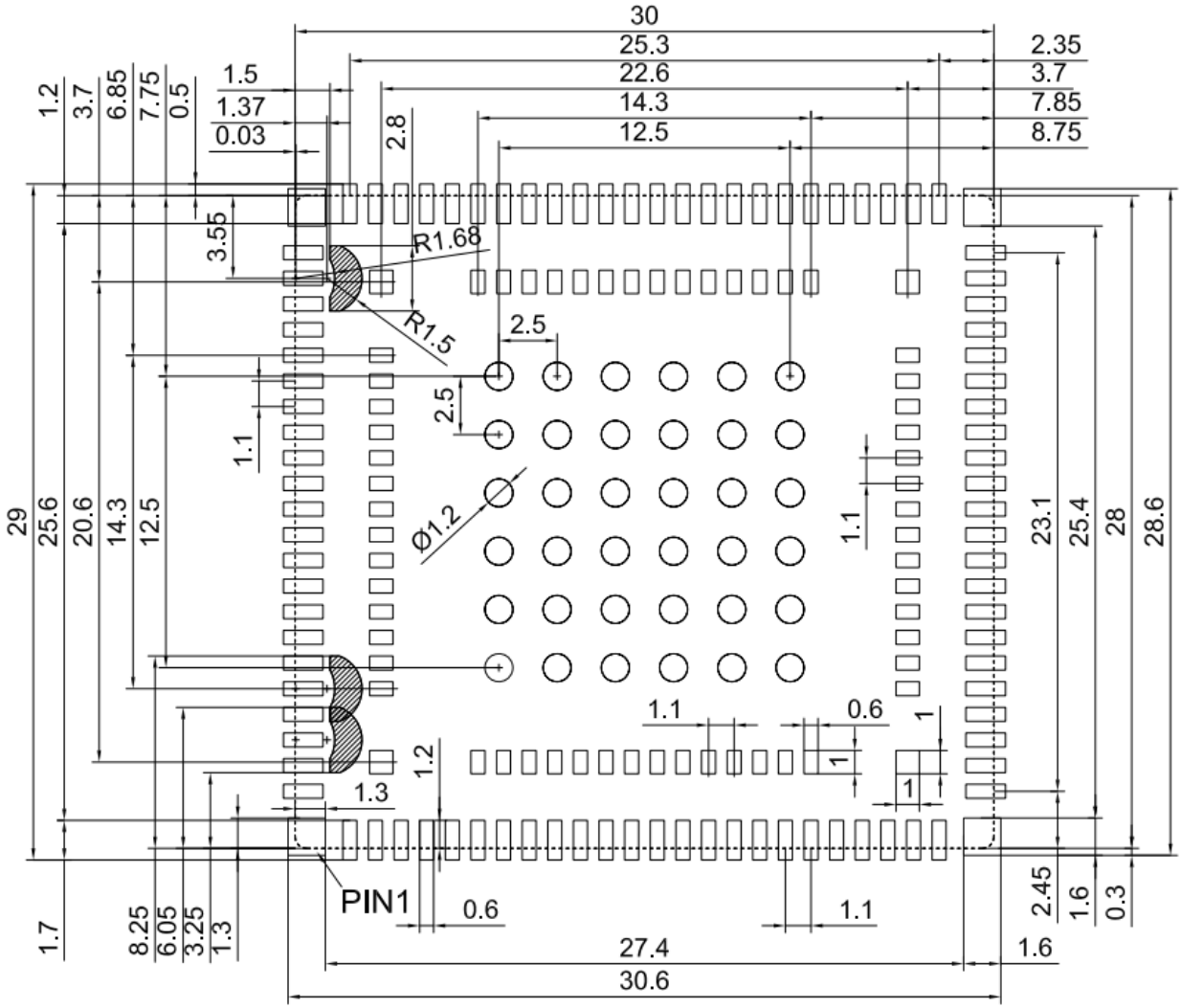


9.2 Application Foot Print

The N725 module has a total of 192 pins in LGA package. and the recommended application PCB package is as follows:

Only GND via-holes and pour coppers are allowed in the shaded area "▨" of the PCB package to ensure the proper operation of the module.

Figure 9-2 N725 recommended footprint of the the application PCB (unit: mm)



9.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

9.4 Solder Paste

The thickness of the solder paste and the flatness of the PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

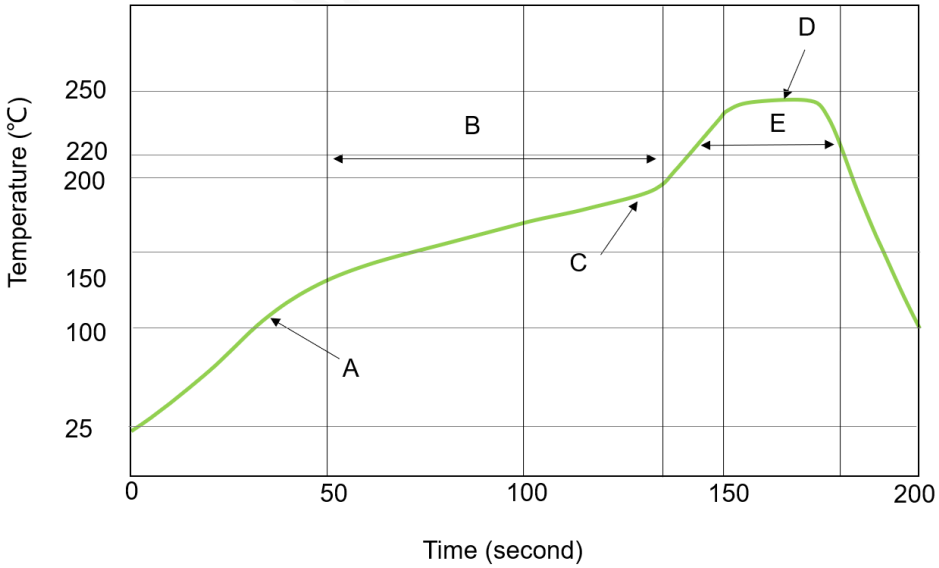
- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process parameters is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220 °C for more than 45 seconds and the peak temperature reaches 240 °C.

9.5 SMT Oven Temperature Profile

Neoway will not provide warranties for heat-responsive element abnormalities caused by improper temperature control.

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 9-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4 °C/sec
- Ramp down rate: -3 to -1 °C/sec
- Soaking zone: 150 - 180°C, Time: 60 - 100s
- Reflow zone: >220°C, Time: 40 - 90s
- Peak temperature: 235 - 245°C

For information about cautions in storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 245 °C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module at high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

A Abbreviations

Abbreviation	Full name
AI	Analog Input
AO	Analog Output
ARM	Advanced RISC Machine
Bps	Bits per Second
CCC	China Compulsory Certification
CS	Chip Select
CTS	Clear to Send
DC	Direct Current
DCS	Digital Cellular System
DI	Digital Input
DL	Downlink
DO	Digital Output
DRX	Discontinuous Reception
eCall	Emergency Call
EGSM	Enhanced GSM
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance
EVK	Evaluation Kit
FDD	Frequency Division Duplexing
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
3GPP	3rd Generation Partnership Project
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
IO	Input/Output
LCC	Leadless Chip Carriers

LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCLK	Main Clock
MCU	Microcontroller Unit
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage
WiFi	Wireless Fidelity
WCDMA	Wide-band Code Division Multiple Access
WLAN	Wireless Local Area Network

