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N723-EA

Hardware User Guide

Issue 1.0 Date 2022-06-02

Notice

This document provides guide for users to use N723-EA.

This document is intended for system engineers (SEs), development engineers, and test engineers.

THIS GUIDE PROVIDES INSTRUCTIONS FOR CUSTOMERS TO DESIGN THEIR APPLICATIONS. PLEASE FOLLOW THE RULES AND PARAMETERS IN THIS GUIDE TO DESIGN AND COMMISSION. NEOWAY WILL NOT TAKE ANY RESPONSIBILITY OF BODILY HURT OR ASSET LOSS CAUSED BY IMPROPER OPERATIONS.

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About This Document

Scope

This document is applicable to N723-EA series.

It defines the features, indicators, and test standards of the N723-EA module and provides reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2022-04	Initial draft	Zou Shiqiang

Conventions

Symbol	Indication
	Indicates danger or warning. This information must be followed. Otherwise, a catastrophic module or user device failure or bodily injury may occur.
	Indicates caution. This symbol alerts the user to important points about using the module. If these points are not followed, the module or user device may fail.
	Indicates instructions or tips. This symbol provides advices or suggestions that may be useful when using the module.

Related Documents

Neoway_N723-EA_Datasheet

Neoway_N723-EA_Product_Specifications

Neoway_N723-EA_AT_Commands_Mannual

Neoway_N723-EA_EVK_User_Guide

1 Safety Recommendations

Ensure that this product is used in compliance with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or workplace:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, and so on.

  If the product is used in a place with flammable gas or dust such as propane gas, gasoline, or flammable spray, the product will cause an explosion or fire.

- Do not use this product in environments such as hospital or airplane where it might interfere with other electronic equipment.

  If the product is used in medical institutions or on airplanes, electromagnetic waves emitted by this product may interfere with surrounding equipment.

Please follow the requirements below in application design:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Please design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Please connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not insert/remove a USIM card or move a memory card from the module while it is still switched on.

2 About N723-EA

This chapter introduces product overview, block diagram, and basic features of N723-EA.

2.1 Product Overview

N723-EA is an industry-grade cellular module that supports LTE-FDD, LTE-TDD, WCDMA, and GSM. It has dimensions of (30.00±0.10) mm × (28.00±0.10) mm × (2.95±0.20) mm and supports PHY chip with external RMII interface, SD card, WLAN chip with SDIO interface, and Codec chip with PCM/I2S interface. It is suitable for developing IoT communication devices such as wireless meter reading terminals, vehicle/handheld POS, industrial routers and so on.

N723-EA has the following characteristics:

- ARM Cortex-R5 processors, 832 MHz main frequency at most, 32 kB L1 command cache, 32 kB L1 data cache
- Supported network modes: LTE Cat. 4, WCDMA, GSM.
- Supports interfaces: I2S/PCM, RMII, USIM, USB2.0, UART, SDIO, SD/eMMC, I2C, and SPI.

Table 2-1 lists the variant and frequency bands that N723-EA supports.

Table 2-1 Variant and frequency bands

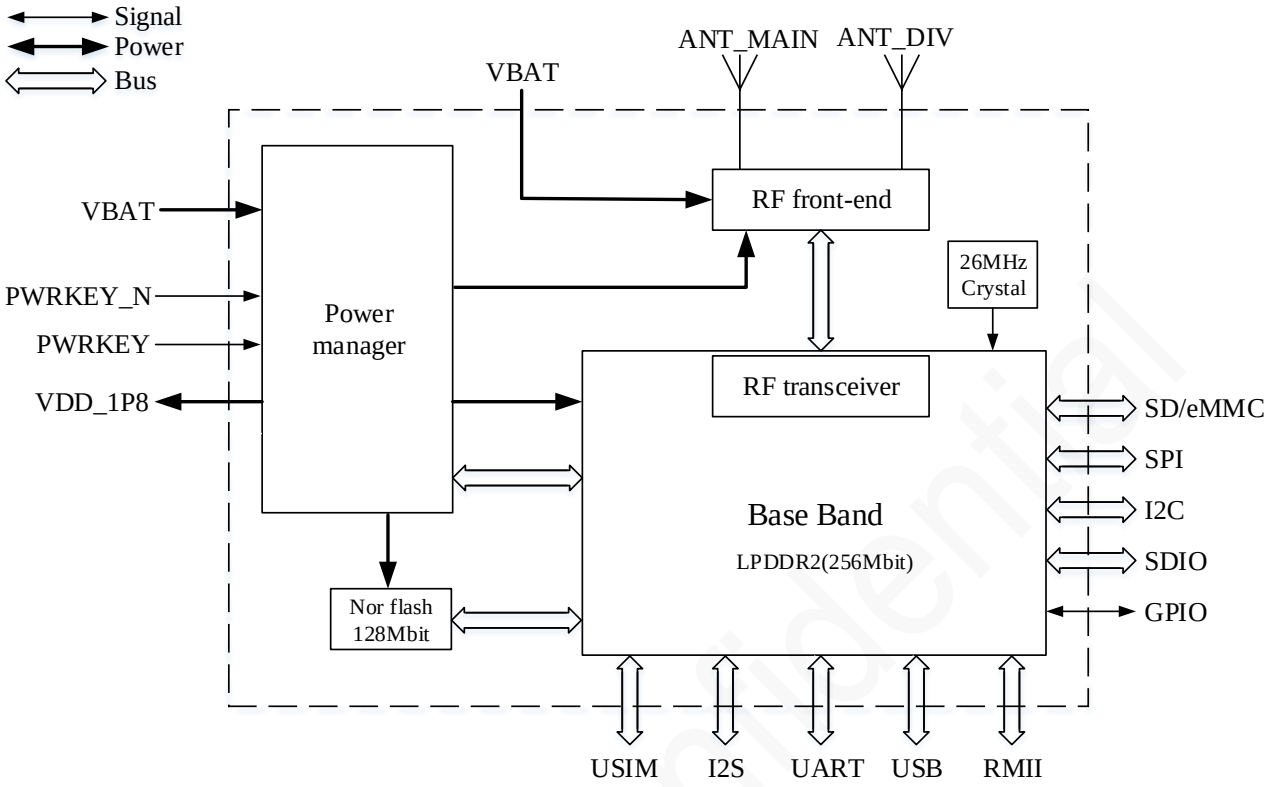
Variant	Region	Category	Band	GNSS	Codec
EA	Europe	Cat 4	FDD-LTE: B1, B3, B5, B7, B8, B20 ,B28 TDD-LTE: B38, B40, B41 WCDMA: B1, B5, B8 GSM/GPRS/EDGE: 900/1800 MHz	Not supported	Not supported

2.2 Block Diagram

N723-EA consists of the following functionality units:

- Baseband unit
- Power management unit
- Radio frequency unit
- Flash storage unit
- Digital interfaces (I2S/PCM, RMII, USIM, USB2.0, UART, SDIO, SD/eMMC, I2C, SPI, GPIO)

Figure 2-1 Block diagram



2.3 Basic Features

Parameter	Description
Physical features	• Dimensions: (30.00±0.10) mm × (28.00±0.10) mm × (2.95±0.20) mm • Package: LGA • Weight: about 5.10 g
Temperature ranges	Operating: -30°C to +75°C Extended[1]: -40°C ~ +85°C Storage: -40°C to +90°C
Operating voltage	VBAT: 3.4 V- 4.2 V, typical value: 3.8 V
Operating current	Sleep[2] : ≤ 4.0 mA
	Idle[3]: ≤ 35 mA
	Operating[4] (LTE mode):≤ 630mA
Application processor	ARM Cortex-R5 processor, 832 MHz main frequency at most, 32 kB L1 command cache, 32 kB L1 data cache
Memory	RAM: 256 Mb ROM: 128 Mb
Band	See Table 2-1.

Wireless rate	GPRS: Max 85.6 Kbps (DL)/Max 85.6 Kbps (UL) EDGE: Max 236.8 Kbps (DL)/Max 236.8 Kbps (UL) WCDMA: HSPA+, Max 21 Mbps (DL)/Max 5.76 Mbps (UL) LTE-FDD: Cat4, no-CA, Max 150 Mbps (DL)/Max 50M bps (UL) LTE-TDD: Cat4, no-CA, Max 130 Mbps (DL)/Max 30 Mbps (UL)
Transmit power	EGSM900: +33 dBm (Power Class 4) DCS1800: +30dBm (Power Class 1) EDGE 900 MHz: +27 dBm (Power Class E2) EDGE1800 MHz: +26 dBm (Power Class E2) WCDMA: +23 dBm (Power Class 3) LTE: +23 dBm (Power Class 3)
Application interfaces	2G/3G/4G antenna, 4G diversity RX antenna. All of each has a characteristic impedance of 50 Ω.
	Three UART interfaces, one of which is a Debug UART interface.
	One USIM interface, 1.8V/3.0V adaptive
	One USB 2.0 interface
	One SDIO interface, used for WLAN
	One SD/eMMC interface, used for SD card or eMMC
	One PCM/I2S interface
	One RMII interface
	One SPI interface, host mode only
	One I2C interface, master mode only
	Four GPIO interfaces
AT commands	3GPP Release 9 Neoway extended commands
SMS	PDU, TXT
Data	PPP, RNDIS
Protocol	TCP/TCPS, UDP, HTTP/HTTPS, FTP, MQTT
Certification approval	CE, RoHS

"Extended[1)]" the module can be registered on the network, but some indicators cannot meet 3GPP standards.

"Sleep mode[2)]": the module enters a low power consumption state. In this state, the peripheral interface of the module is disabled, but the radio frequency (RF) is functioning properly. The module will exit the sleep mode when there is an incoming call or SMS message, and will re-enter the sleep mode at the end of the incoming call or conversation.

"Standby mode[3)]": the module is in normal working state, but there is no on-going data service.

"Operating mode[4)]": refers to the working current of the module when there is data communication. Only the currents in LTE mode are listed here. For details about currents under other network standards, see the N723-EA current test report.

3 Reference Standards

N723-EA is designed by referring to the following standards:

- 3GPP TS 36.521-1 V9.10.0 User Equipment(UE) conformance specification; Radio transmission and reception; Part 3: Radio Resource Management (RRM) conformance testing
- 3GPP TS 21.111 V9.0.0 USIM and IC card requirements
- 3GPP TS 31.102 V9.19.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V9.12.2 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V9.9.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V9.0.1 Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

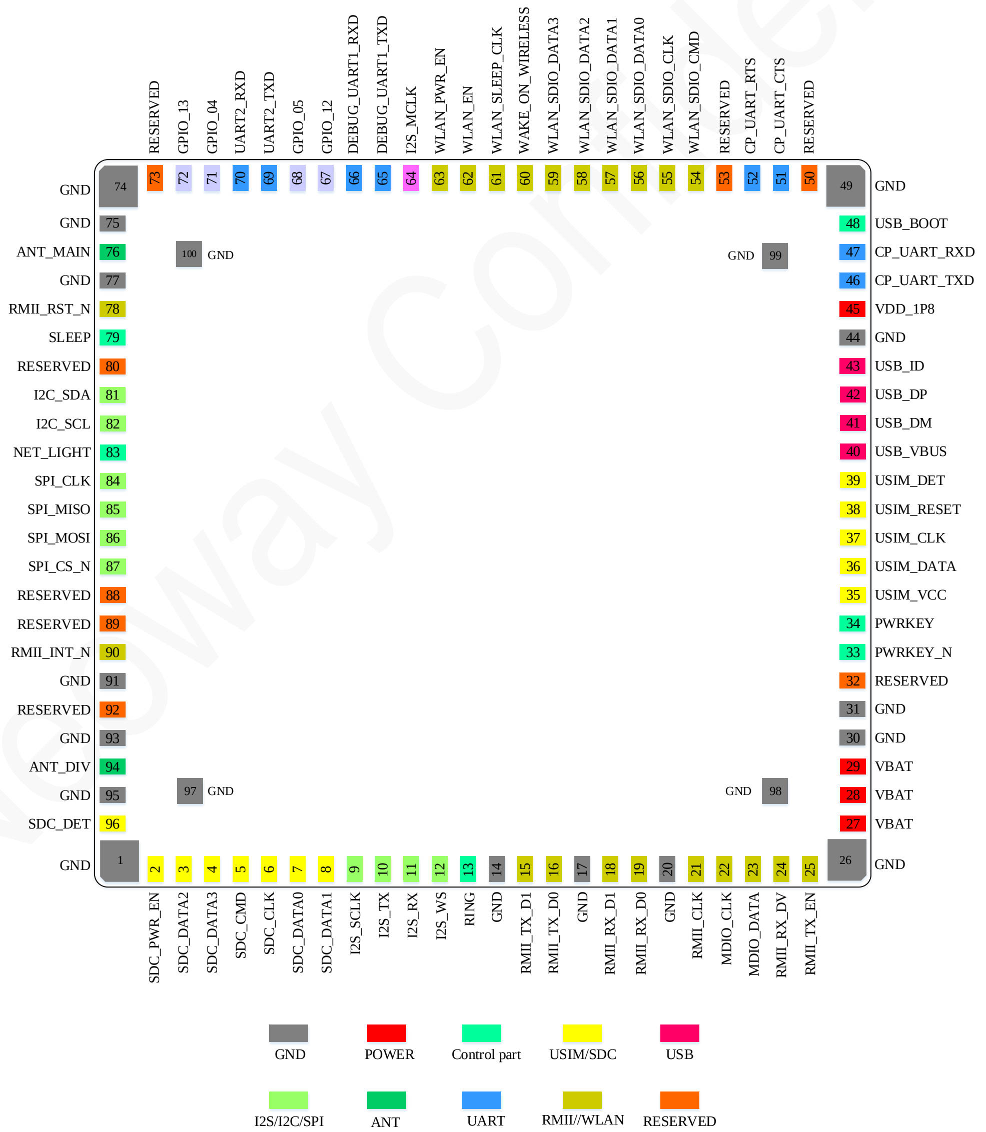
4 Module Pins

There are 100 pins on N723-EA and their pads are introduced in LGA package.

4.1 Pin Layout

Figure 4-1 shows the pad layout of N723-EA.

Figure 4-1 N723-EA pin definition (top view)



- If you need to use the I2S or RMII function, contact Neoway FAEs.
- Do Not pull-down USB_BOOT before the initialization process is completed.
- All the RESERVED and Ground pins must be left floating.

4.2 Pin Description

Table 4-1 lists the IO definitions and DC characteristics.

Table 4-1 Pin description

IO type	Pin description
AI	Analog input
AO	Analog output
AIO	Analog input/output
B	Digital Input/Output
DI	Digital Input
DO	Digital Output
PI	Power input
PO	Power output

Table 4-2 Level feature

Interface type	Power domain	Power domain description	Power domain features	Logic level
USIM	P1	USIM interface	1.8 V/3.0 V self-adaptive	1.8 V level feature: $V_{IH} = 0.7 * V_{DD\_P1} \sim V_{DD\_P1} + 0.2V$ $V_{IL} = -0.3V \sim 0.3 * V_{DD\_P1}$ $V_{OH(Min)} = V_{DD\_P1} - 0.2V$ $V_{OL(Max)} = 0.2V$ 3.0V level feature: $V_{IH} = 2.0V \sim V_{DD\_P1} + 0.3V$ $V_{IL} = -0.3V \sim 0.8V$ $V_{OH(Min)} = 2.4V$ $V_{OL(Max)} = 0.4V$
SD/eMMC	P2	SD/eMMC interface	1.8 V or 3.0 V	1.8 V level feature: $V_{IH} = 0.7 * V_{DD\_P2} \sim V_{DD\_P2} + 0.2V$

				$V_{IL} = -0.3V \sim 0.3 * V_{DD\_P2}$ $V_{OH(Min)} = V_{DD\_P2} - 0.2V$ $V_{OL(Max)} = 0.2V$ 3.0V level feature: $V_{IH} = 2.0V \sim V_{DD\_P2} + 0.3V$ $V_{IL} = -0.3V \sim 0.8V$ $V_{OH(Min)} = 2.4V$ $V_{OL(Max)} = 0.4V$
GPIO	P3	1.8 V digital IO	1.8 V power	Input: $V_{IH} = 0.7 * V_{DD\_P3} \sim V_{DD\_P3} + 0.2V$ $V_{IL} = -0.3V \sim 0.3 * V_{DD\_P3}$ Output: $V_{OH(Min)} = V_{DD\_P3} - 0.2V$ $V_{OL(Max)} = 0.2V$
RMII	P4	RMII interface	1.8 V or 3.3 V	1.8 V level feature: $V_{IH} = 0.7 * V_{DD\_P4} \sim V_{DD\_P4} + 0.2V$ $V_{IL} = -0.3V \sim 0.3 * V_{DD\_P4}$ $V_{OH(Min)} = V_{DD\_P4} - 0.2V$ $V_{OL(Max)} = 0.2V$ 3.3V level feature: $V_{IH} = 2.0V \sim V_{DD\_P4} + 0.3V$ $V_{IL} = -0.3V \sim 0.8V$ $V_{OH(Min)} = 2.4V$ $V_{OL(Max)} = 0.4V$

- If you need to use the PCM/I2S or RMII function, contact Neoway FAEs.
- The power domains of PWRKEY_N is VBAT, and direct connection of GPIOs in different power domains is prohibited, as that will result in voltage backflow.
- RMII only supports 1.8 V level by default. If supporting 3.3 V level is required, ensure that the hardware supports it.
- SD/eMMC supports 1.8 V level by default. If supporting 3.0 V level is required, the firmware should be configured; ensure whether it is configured before using the pin.
- The GPIO interface is equipped with the interrupt function. If you need to use the interrupt function, contact Neoway FAE; otherwise, the software interrupt priority may be abnormal and unpredictable risks may arise when the module is running.

Table 4-3 Pin Description

Signal	Pin	I/O	Function description	Level feature	Remarks
Power interface					
VBAT	27, 28, 29	PI	Main power supply of the module	V_{min} = 3.4 V V_{norm} = 3.8 V V_{max} = 4.2 V	The external power supplies at least 2.5 A current to VBAT.
VDD_1P8	45	PO	1.8 V power output	V_{norm} = 1.8V I_{max} = 50 mA	Used only for level shifting. Leave this pin floating if it is not used.
GND	1, 14, 17, 20, 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97, 98, 99, 100				Ensure that all GND pins are grounded.
Control Interfaces					
PWRKEY_N	33	DI	Used to power on/off or reset the module.	-	Power-on/off & reset of the module is triggered by the low pulse, and is controlled based on the low pulse width. The interface voltage is default to VBAT.
PWRKEY	34	DI	Startup control	-	Power-on of the module is triggered by the high level. Leave this pin floating if it is not used.
USB_BOOT	48	DI	Forcible download/upgrade control pin	P3	Used to enter the USB download mode by pulling up its voltage to GND. Leave this pin floating if it is not used.
SLEEP	79	DI	Sleep mode control	P3	Controls the module to enter into/exit from sleep mode. Leave this pin floating if it is not used.

SD/eMMC interface					
SDC_PWR_EN	2	DO	Control of the external power supply for SD/eMMC	P3	Leave this pin floating if it is not used.
SDC_DATA2	3	B	SD/eMMC data 2	P2	Leave this pin floating if it is not used.
SDC_DATA3	4	B	SD/eMMC data 3	P2	Leave this pin floating if it is not used.
SDC_CMD	5	DO	SD/eMMC command control	P2	Leave this pin floating if it is not used.
SDC_CLK	6	DO	SD/eMMC clock	P2	Leave this pin floating if it is not used.
SDC_DATA0	7	B	SD/eMMC data 0	P2	Leave this pin floating if it is not used.
SDC_DATA1	8	B	SD/eMMC data 1	P2	Leave this pin floating if it is not used.
SDC_DET	96	DI	SD/eMMC detect input	P3	Leave this pin floating if it is not used.
USIM2 Interfaces					
I2S_SCLK	9	DO	I2S data clock	P3	Leave this pin floating if it is not used.
I2S_TX	10	DO	I2S data sending	P3	Leave this pin floating if it is not used.
I2S_RX	11	DI	I2S data receiving	P3	Leave this pin floating if it is not used.
I2S_WS	12	B	I2S right and right channels selection	P3	Leave this pin floating if it is not used.
I2S_MCLK	64	DO	I2S master clock	P3	The default frequency is 26 MHz.
RMII Interfaces					
RMII_TX_D0	16	DO	Data sending bit 0	P4	Leave this pin floating if it is not used.
RMII_TX_D1	15	DO	Data sending bit 1	P4	Leave this pin floating if it is not used.
RMII_RX_D0	19	DI	Data receiving bit 0	P4	Leave this pin floating if it is not used.

RMII_RX_D1	18	DI	Data receiving bit 1	P4	Leave this pin floating if it is not used.
RMII_CLK	21	DI	Data clock	P4	Leave this pin floating if it is not used.
RMII_RX_DV	24	DI	Valid when receiving data	P4	Leave this pin floating if it is not used.
RMII_TX_EN	25	DO	Enable data sending	P4	Leave this pin floating if it is not used.
RMII_INT_N	90	DI	Interrupt input	P4	Leave this pin floating if it is not used.
RMII_RST_N	78	DO	Reset signal output	P3	Leave this pin floating if it is not used.
MDIO					
MDIO_CLK	22	DO	MDIO clock	P4	Leave this pin floating if it is not used.
MDIO_DATA	23	B	MDIO data	P4	Connecting a 4.7 kΩ external pull-up resistor is required. Leave this pin floating if it is not used.
USIM Interface					
USIM_VCC	35	PO	USIM power output	P1	Iomax=50 mA.
USIM_DATA	36	B	USIM data input and output	P1	Connecting a 4.7 kΩ pull-up resistor to USIM_VCC is required.
USIM_CLK	37	DO	USIM clock output	P1	Leave this pin floating if it is not used.
USIM_RESET	38	DO	USIM reset	P1	Leave this pin floating if it is not used.
USIM_DET	39	DI	USIM detection	P3	It is recommended to connect this pin to VDD_1P8 through a 47 kΩ pull-up resistor if it is not used.
USB Interface					
USB_VBUS	40	PI	Voltage detection	3.5 V to 5.2 V, typical value: 5.0 V	Used for software download and data transmission. DM and DP adopt differential routing, and the differential impedance must

USB_DM	41	IO	USB data negative signal	-	be 90 Ω. Leave this pin floating if it is not used.
USB_DP	42	IO	USB data positive signal	-	
USB_ID	43	DI	OTG detect	P3	This function is in development. Leave this pin floating if it is not used.
UART Interface					
CP_UART_TXD	46	DO	Data transmitting	P3	Used for AT commands communication and support hardware flow control. Leave this pin floating if it is not used.
CP_UART_RXD	47	DI	Data receiving	P3	
CP_UART_CTS	51	DI	The user allows the module to send data.	P3	
CP_UART_RTS	52	DO	The module requests the user to send data.	P3	
DEBUG_UART1_TXD	65	DO	Data transmitting	P3	Only used for debug. Leave this pin floating if it is not used.
DEBUG_UART1_RXD	66	DI	Data receiving	P3	
UART2_TXD	69	DO	Data transmitting	P3	Used for data transmission. Leave this pin floating if it is not used.
UART2_RXD	70	DI	Data receiving	P3	
SDIO Interface					
WLAN_SDIO_CMD	54	B	SDIO command	P3	Leave this pin floating if it is not used.
WLAN_SDIO_CLK	55	DO	SDIO clock	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA0	56	B	SDIO data bit 0	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA1	57	B	SDIO data bit 1	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA2	58	B	SDIO data bit 2	P3	Leave this pin floating if it is not used.
WLAN_SDIO_DATA3	59	B	SDIO data bit 3	P3	Leave this pin floating if it is not used.
WAKE_ON_WIRELESS	60	DO	WLAN wakeup control	P3	Leave this pin floating if it is not used.

WLAN_SLEEP_CLK	61	DO	Wi-Fi sleep clock	P3	Clock frequency: 32 KHz. Leave this pin floating if it is not used.
WLAN_EN	62	DO	WLAN enable control	P3	Leave this pin floating if it is not used.
WLAN_PWR_EN	63	DO	Control of the external power supply for WLAN	P3	Leave this pin floating if it is not used.
I2C Interface					
I2C_SDA	81	B	I2C data	P3	Supporting only host mode; connecting this pin to VDD_1P8 through a pull-up resistor externally is required; for details, see 5.3.7 .
I2C_SCL	82	DO	I2C clock	P3	
SPI interface					
SPI_CLK	84	DO	Clock signal	P3	Supporting only master mode. Leave this pin floating if it is not used.
SPI_MISO	85	DI	Output of the slave device and input of the master device	P3	
SPI_MOSI	86	DO	Input of the slave device and output of the master device	P3	
SPI_CS_N	87	DO	Chip select signal of the slave device	P3	
GPIO					
GPIO_12	67	B	GPIO with interrupt	P3	Pull-up by default. Leave this pin floating if it is not used.
GPIO_05	68	B	GPIO with interrupt	P3	Pull-up by default. Leave this pin floating if it is not used.
GPIO_04	71	B	GPIO with interrupt	P3	Pull-up by default.

					Leave this pin floating if it is not used.
GPIO_13	72	B	GPIO with interrupt	P3	Pull-down by default. Leave this pin floating if it is not used.
Antenna Interfaces					
ANT_MAIN	76		Main antenna		50 Ω impedance characteristics
ANT_DIV	94		Diversity antenna		50 Ω impedance characteristics
Other Interfaces					
RING	13	DO	Incoming call indicator control	P3	Leave this pin floating if it is not used.
NET_LIGHT	83	DO	Network indicator control	P3	Leave this pin floating if it is not used.
RESERVED					
RESERVED	32, 50, 53, 73, 80, 88, 89, 92				Used for function extension or the function not open to users. These RESERVE pins might have different definitions or functions. Ensure that all RESERVED pins are left floating.

5 Application Interfaces

N723-EA provides the power, control, communication, audio, RF interfaces, and so on to meet the functional requirements of customers in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

5.1 Power Interface

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin	I/O	Function description	Remarks
VBAT	27, 28, 29	PI	Power input of the module	V_{min} = 3.4 V V_{norm} = 3.8 V V_{max} = 4.2V
VDD_1P8	45	PO	1.8 V power output	V_{norm} = 1.8V I_{max} = 50 mA
GND	1, 14, 17, 20, 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97, 98, 99, 100			Ensure that all GND pins are grounded.

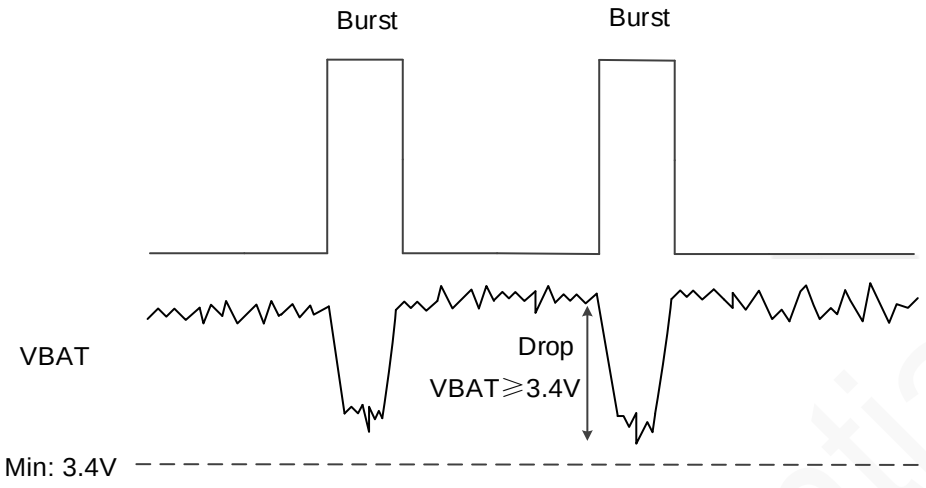
5.1.1 VBAT

The power supply design covers two parts: schematic design and PCB layout.

Power Supply Design

In GSM/GPRS mode, RF data is transmitted in burst mode that generates voltage drops on the power supply. Furthermore, this results in a 217 Hz TDD noise through the power and the transient peak current is 2 A. Therefore, it is necessary to ensure that in the power supply design, the impedance of the power supply traces is low, and there are large-capacity capacitors to improve the freewheeling capability to ensure that the voltage will not drop below the minimum operating voltage of the module when the instantaneous current reaches its peak.

Figure 5-1 Voltage drop of the power supply.



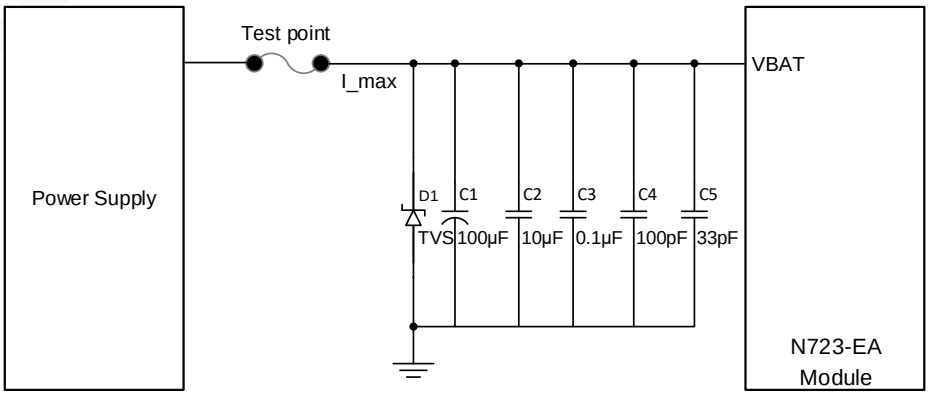
Never use a diode to make the drop voltage between a higher input and module power. The forward voltage drop V_f of the diode has two characteristics: one is that it increases with the increase of forward current; the other is that it increases significantly at a low temperature. If there is an instantaneous high current, the instantaneous increase of forward voltage drop will lead to unstable operating voltage of the module, or even damage the module.

The power supply design of the N723-EA module is determined by the power input voltage. The designs are classified by power input voltage as follows:

- Supports the 3.4V - 4.2 V power input (typical value: 3.8 V, using the battery for power supply)
- Supports the 4.2V - 5.5 V power input (typical value: 5.0 V, using the internal rectifier of the computer for power supply)
- Supports the 5.5 V - 24 V power input (typical value: 12 V, typically applicable to the automobile industry)

The recommended 3.4V to 4.2 V input design is as follows:

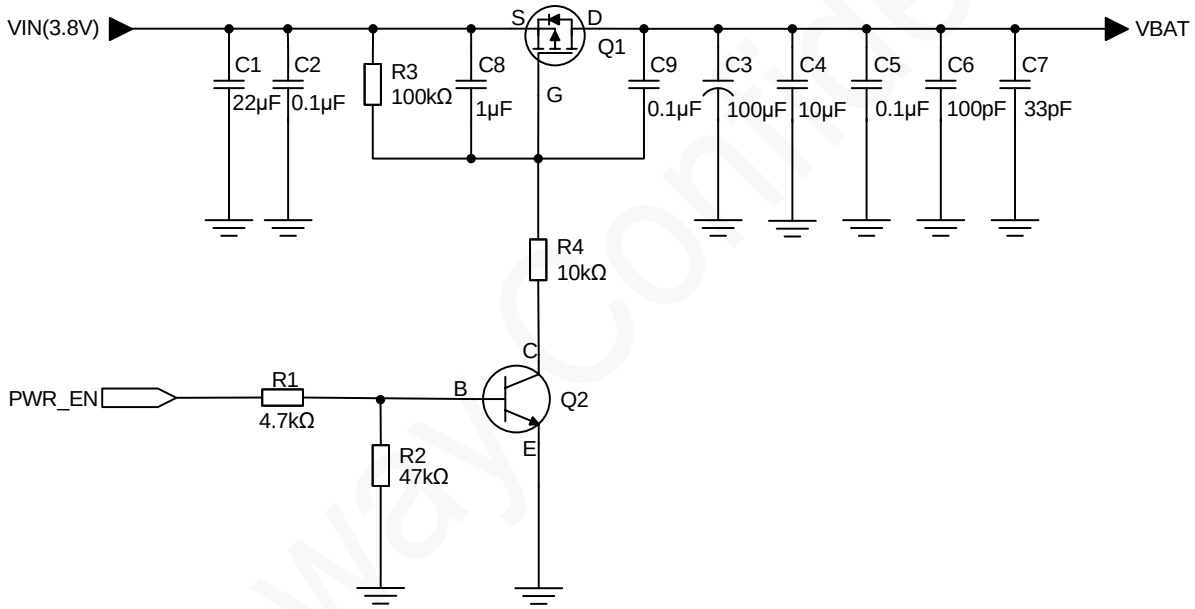
Figure 5-2 Recommended design 1



- The maximum input voltage for the module is 4.2 V and the typical value is 3.8 V. For VBAT, the recommended layout cable width is 2.5 mm or above.
- The TVS diode selected at D1 has a reverse operating voltage (V_{RWM}) of 4.5 V, and its peak power Ppp is 2800 W (tp=8/20 uS). It has the surge protection mechanism. Place the TVS close to the power input interface to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be larger than 2 times the voltage across the power supply.
- Place a bypass capacitor (C2, C3, C4, C5) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

The following circuit design is recommended to control the power supply.

Figure 5-3 Recommended design 2

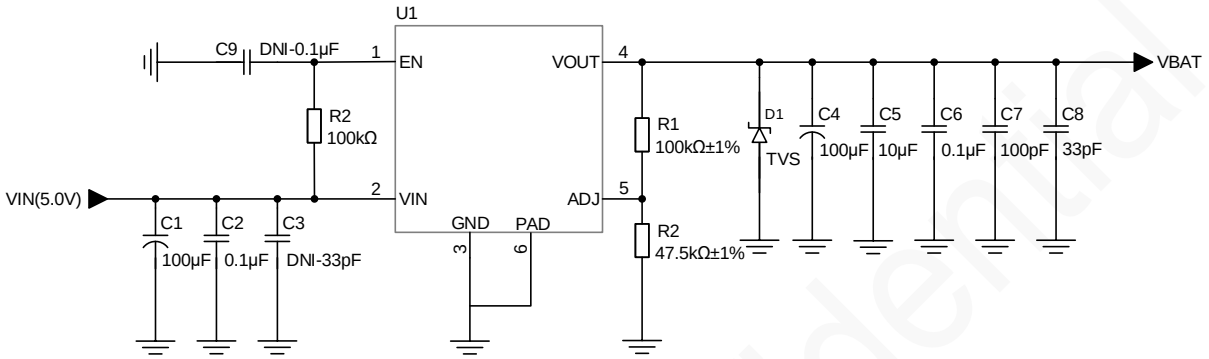


- Select an enhanced p-MOSFET at Q1, of which the safe operating voltage is at least 12 V (V_{dss}=-12 V) and drain current is at least 3.5 A ($I_{D(MAX)}$=-3.5) and Rds is low ($Rds_{(on)}$ =108 mΩ).
- Select a common NPN tripolar transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which operating voltage of the tripolar transistor might increase in low temperature; it is recommended that the value of R2 be at least 10 times that of R1.
- Place C3 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C3 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.

- Place a bypass capacitor (C4, C5, C6, C7) of low-ESR close to the module to filter out high-frequency jamming from the power supply.
- Select the capacitors at C8 and C9 based on the specifications and the actual test conditions of the p-MOSFET since their capacitance may affect the turn-on and off time of the p-MOSFET.

Recommended 4.2V to 5.5 V input design:

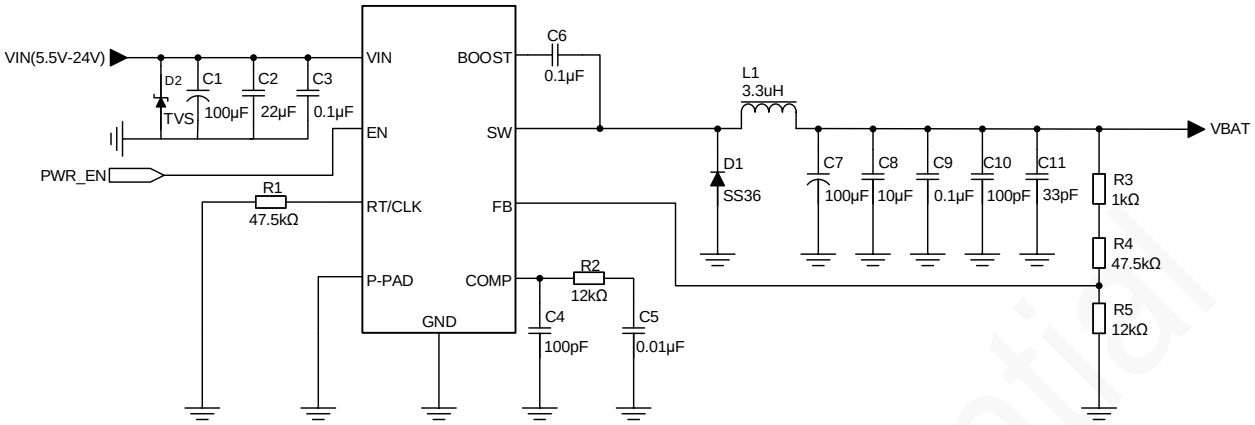
Figure 5-4 Recommended design 3



- Design with LDO is more simpler and efficient when the output of power supply is close to the permissible voltage across VBAT.
- It is recommended to select an LDO that its maximum output current be greater than 2.5 A at U1.
- The TVS diode selected at D1 has a reverse operating voltage (V_{RWM}) of 4.5 V, and its peak power Ppp is 2800 W (tp=8/20 uS). It has the surge protection mechanism. Place the TVS close to the power input interface to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Place C4 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C4 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Place a bypass capacitor (C5, C6, C7, C8) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

Recommended 5.5 V to 24 V input design:

Figure 5-5 Recommended design 4



- As there is a big difference between the power input and VBAT, the DC-DC step-down chip should be selected, and the maximum output current should be at least 2.5 A.
- Place the TVS (D2) close to the power input interface to clamp the surge voltage before it enters back-end circuits to ensure that the back-end components and the module are protected.
- It is recommended to select a DC-DC step-down chip with a 500 kHz switching frequency or above; the value of the power inductor is related to the setting of the switching frequency. For details, refer to the specifications of the chip.

  Note that the switching frequency of the DC-DC power supply is related to the device performance, and may cause EMI interference.
- For vehicle batteries (lead-acid batteries), power surge protection should be added to the input front end, and the device withstand voltage should be greater than 42 V.
- Place C7 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C7 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Place a bypass capacitor (C8, C9, C10, C11) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

PCB Layout

An ESR capacitor must be placed at the output end of the power supply to suppress the peak current. A TVS diode must be placed at the power input end to suppress voltage spikes and protect back-end devices. The circuit design is important, and the device layout and routing are equally important. Several key points in power supply design are summarized below:

- The TVS diode can absorb instantaneous high-power pulses, and withstand instantaneous pulse current peaks up to tens or even hundreds of amperes. The clamp response time is extremely short. The TVS diode should be placed as close as possible to the power input to ensure that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB wires.
- The bypass capacitor must be placed close to the power supply pin of the module to filter out high-frequency noise signals in the power supply.
- For the module power circuit, the PCB routing width must ensure that the 2.5 A current can be passed safely, and there should be no obvious loop voltage drop. The PCB routing width should be at least 2.5 mm to ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make the power cable short and thick.
- Noise-sensitive circuits, such as audio circuits and RF circuits, should be kept away from power circuits, especially when the DC-DC power supply is used.
- The voltage frequency of the SW pin of the DC-DC power supply is high, and the loop should be minimized. Sensitive component should be kept far away from the SW pin of the DC-DC component to prevent noise coupling. Feedback component should be placed as close as possible to the FB pin and COMP pin.
- The GND pin and bottom pad of the chip must be grounded to ensure good heat dissipation and noise isolation.

5.1.2 VDD_1P8

VDD_1P8 power is on normally and cannot be turned off even when the module is in sleep mode. Connecting the module to an external circuit will increase its power consumption in sleep module. It is recommended that VDD_1P8 is used for level shift only and an ESD protector should be added.

N723-EA provides one VDD_1P8 output. It can provide the 1.8 V voltage and the maximum output current is 50 mA. It is recommended that DVDD_1P8 is used for level shift and digital IO pull-up power supply only and an ESD protector should be added.

5.2 Control Interfaces

Signal	Pin	I/O	Function description	Remarks
PWRKEY_N	33	DI	Power-on/off & reset control	Power-on/off & reset of the module is triggered by the low pulse, and is controlled based on the low pulse width. The internal interface voltage is default to VBAT.
PWRKEY	34	DI	Startup control	Power-on of the module is triggered by the high level. Leave this pin floating if it is not used.

USB_BOOT	48	DI	Forcible download/upgrade control pin	Pulling down this pin to GND can trigger the module to enter USB download mode. Leave this pin floating if it is not used.
SLEEP	79	DI	Sleep mode control	It controls the sleep mode of the module. Leave this pin floating if it is not used.

There are three methods to start the module. You can choose the method according to the specific application scenario. Contact Neoway FAEs if necessary.

N723-EA allows startup by the following methods:

- Figure 5-6 shows the reference design of starting the module by using a button.
- Figure 5-7 shows the reference design of starting the module through an MCU.
- Figure 5-8 shows the reference design of automatic start once powered up.

5.2.1 PWRKEY_N

PWRKEY_N supports the following functions:

- When the module is in shut-down state, inputting negative pulses for more than 0.5s to PWRKEY_N can trigger the power-on state of the module.
- When the module is in normal startup state, inputting negative pulses for more than 4s to PWRKEY_N can reset the module
- When the module is in normal startup state, inputting negative pulses for more than 18s to PWRKEY_N can shut down the module.

Ensure that the VBAT voltage is stable before controlling PWRKEY_N. It is recommended to control PWRKEY_N after the VBAT voltage rises to 3.8 V for 50 ms.

The following figure shows the reference design of startup controlled by the PWRKEY_N pin:

Figure 5-6 Reference design of startup, shutdown, and reset controlled by a button

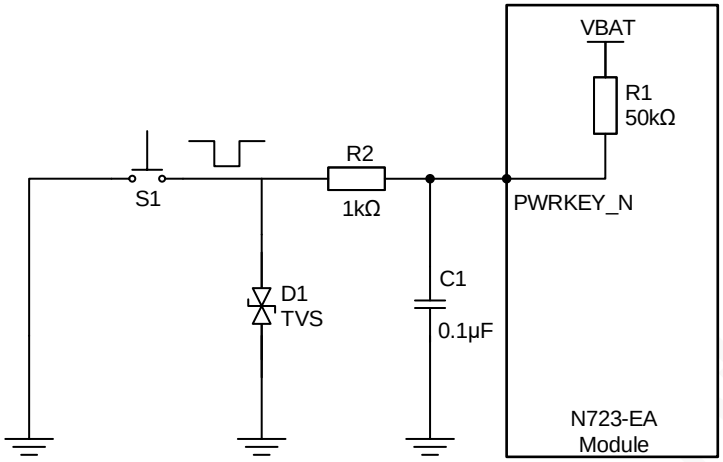
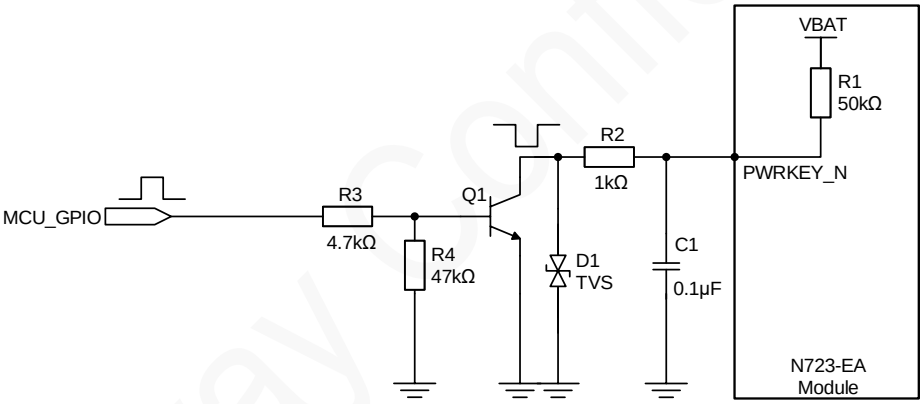


Figure 5-7 Reference design of startup, shutdown, and reset controlled by an MCU



Do NOT connect an external resistor (R2) with large resistance in series to the PWRKEY_N pin. Otherwise, the module cannot be started since the PWRKEY_N is at a high level all the time.

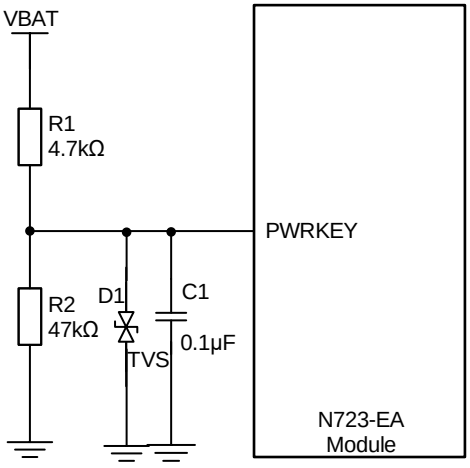
5.2.2 PWRKEY

PWRKEY is a high-level control startup pin; pull the PWRKEY pin up to VBAT, and the module can start automatically once it is powered on.

If the design of automatic startup upon power-on is adopted, then shutdown can be performed only through power-down (PWRKEY_N cannot be used to shut down the module at that time).

The following figure shows the reference design of startup controlled by the PWRKEY pin:

Figure 5-8 Reference design of automatic start once powered up



Startup process

When the module is in shut-down state, it is recommended that inputting a low-level pulse to PWRKEY_N less than 3s can start the module.

The following figure shows the startup process:

Figure 5-9 Startup process (by controlling PWRKEY_N)

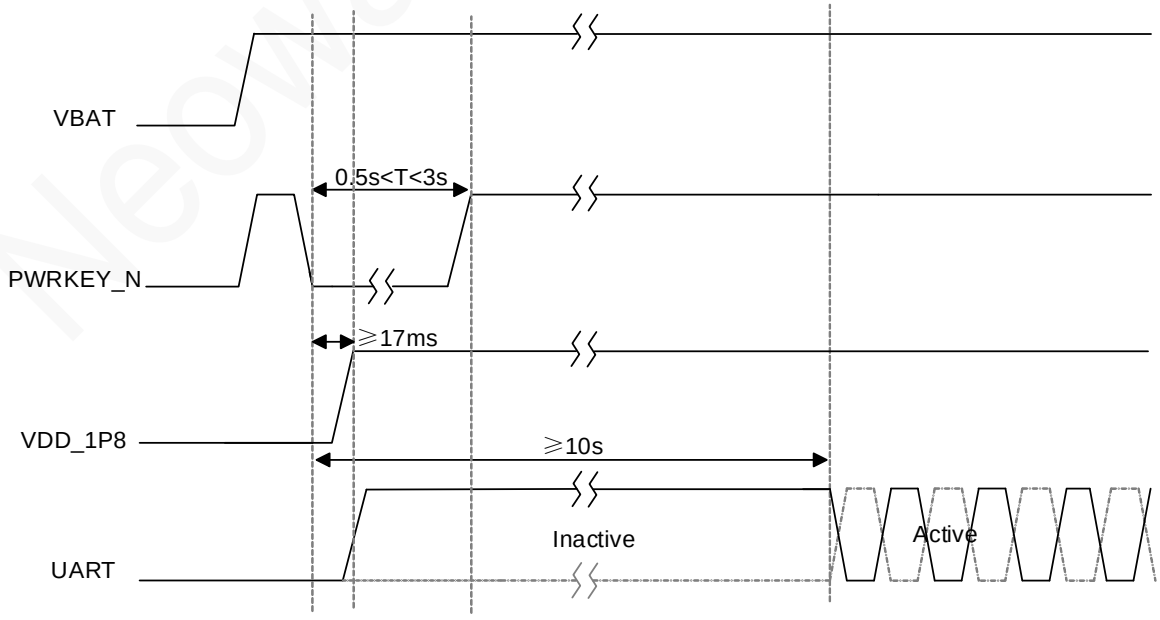
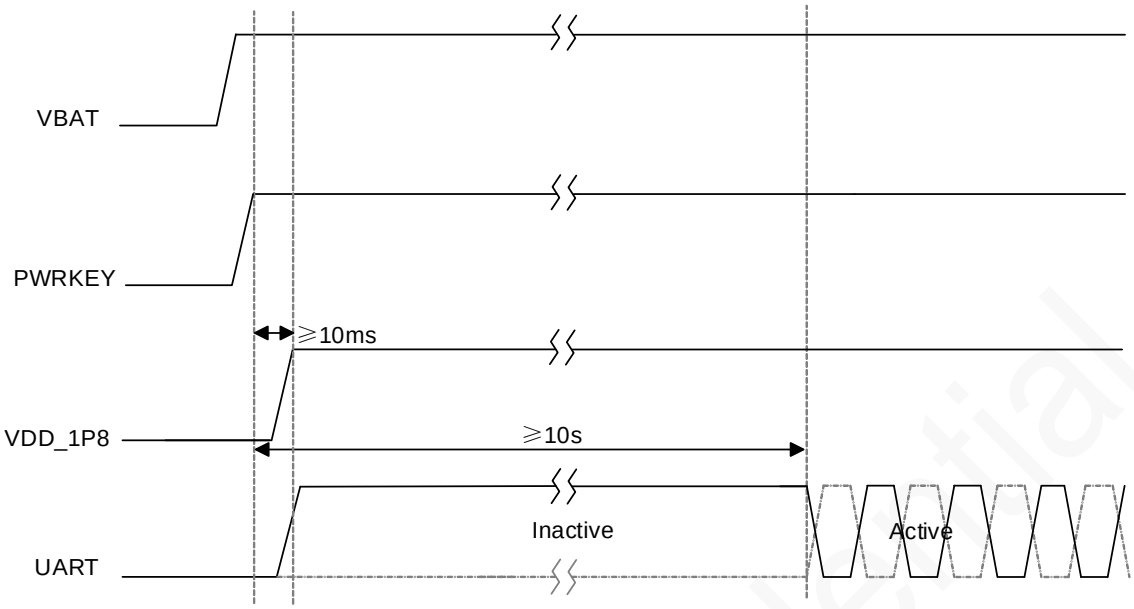


Figure 5-10 Startup process (by controlling PWRKEY)



Do not perform other operations on the module until it is initialized completely since if the module is started but the initialization process has not been completed, the states of each pin are uncertain.

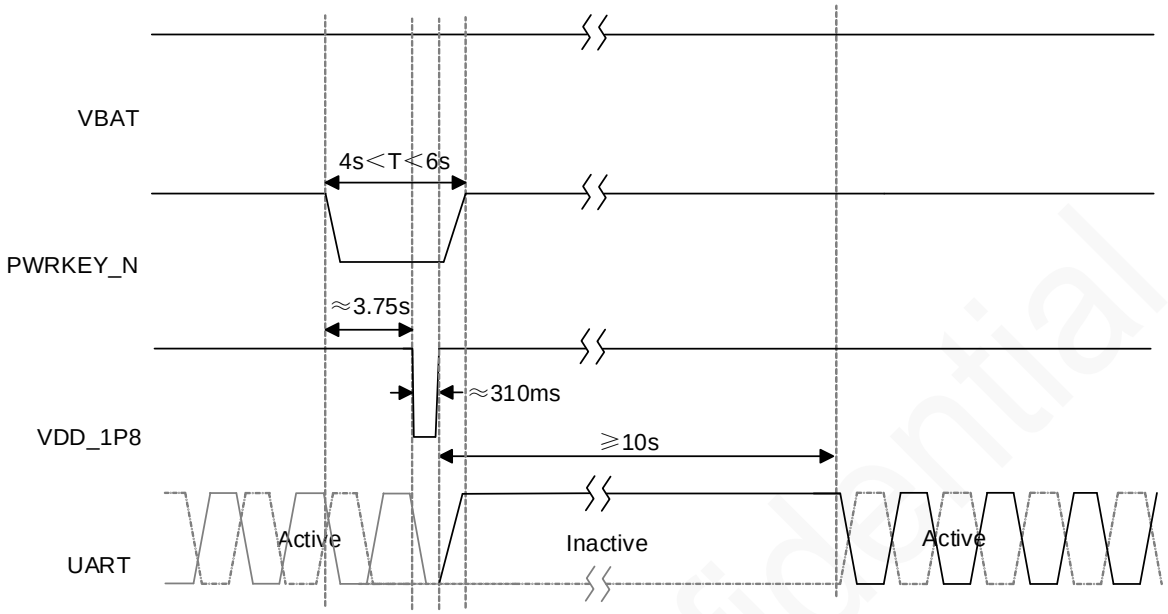
When VDD_1P8 of the module has voltage output, the UART port cannot communicate normally since its boot process has not been completed yet. The power-on time of VDD_1P8 and UART may slightly vary with the module software.

Reset process

When the module is in startup state, it is recommended that inputting a low-level pulse to PWRKEY_N less than 6s can reset the module.

The following figure shows the reset process of the module:

Figure 5-11 Reset process of the module



Shutdown process

When the module is in a normal startup state, during the process of shutting down the module by controlling PWRKEY_N, the module will first perform the reset process, and finally enter the shutdown state. It is recommended that before shutdown, the MCU completes the data communication operation with the UART, USB and other interfaces of the module, and then performs the shutdown operation.

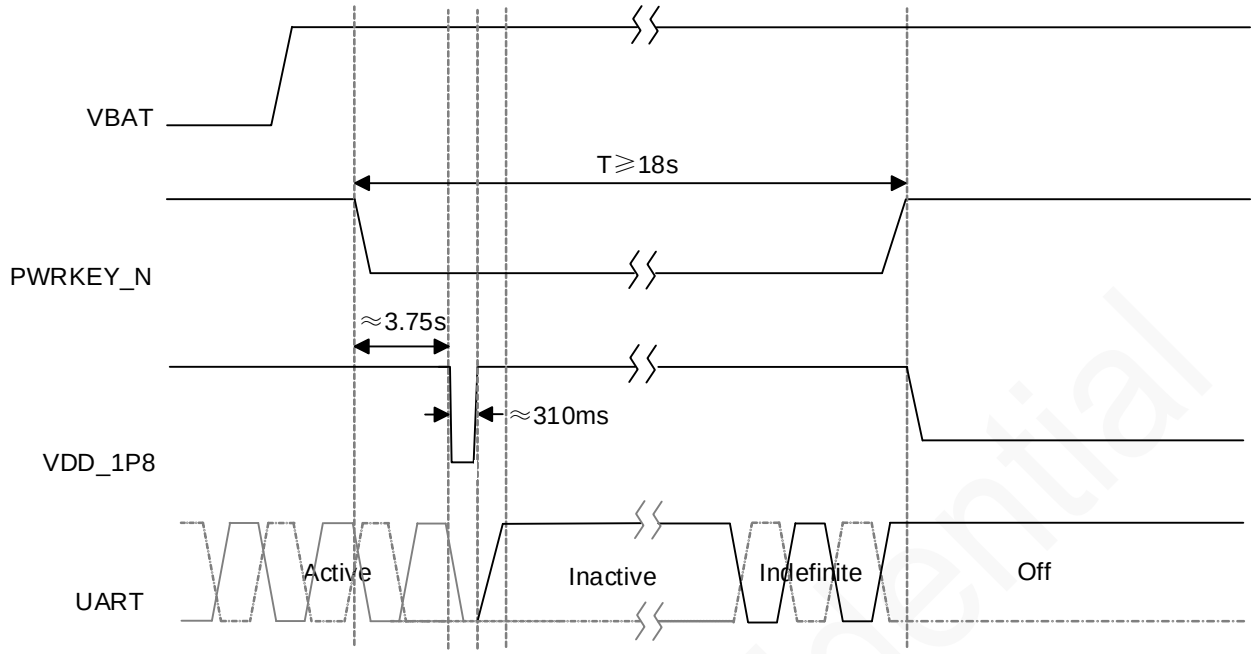
If the design of automatic startup upon power-on is adopted, shutdown can be performed only through power-down.

Two methods are available to shut down the module: hard shutdown and soft shutdown.

- For how to shut down the module through software, see *Neoway_N723-EA_AT_Commands_Manual*.
- Shut down the module through hardware can be performed by controlling the PWRKEY_N pin.

The following figure shows the hardware shutdown process:

Figure 5-12 Hardware shutdown process



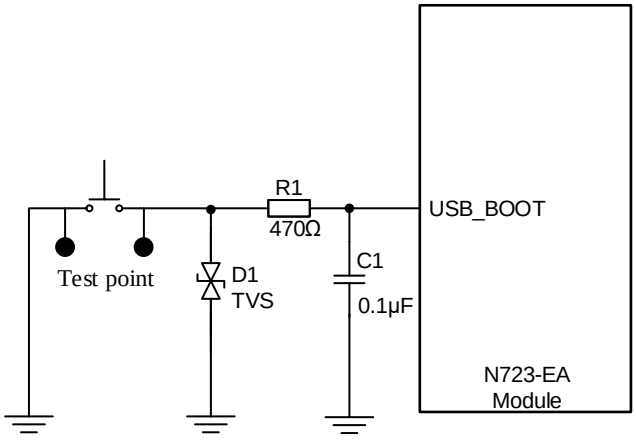
When the module executes the shutdown process, VDD_1P8 stops the voltage output after the UART port completes the shutdown process. The low pulse width needed for RESET_N hard shutdown may slightly vary with the module software.

5.2.3 USB_BOOT

USB_BOOT is the pin to forcibly enter the download mode. Connect USB_BOOT to GND through a pull-down resistor after the module is started, and the module will enter forcible download mode. This is the last method to handle issues that result in startup or running failures. It is recommended to reserve this pin (as a button or a test point) to facilitate software upgrades and debugging.

The following figure shows a reference design of USB force download:

Figure 5-13 Reference design of USB force download



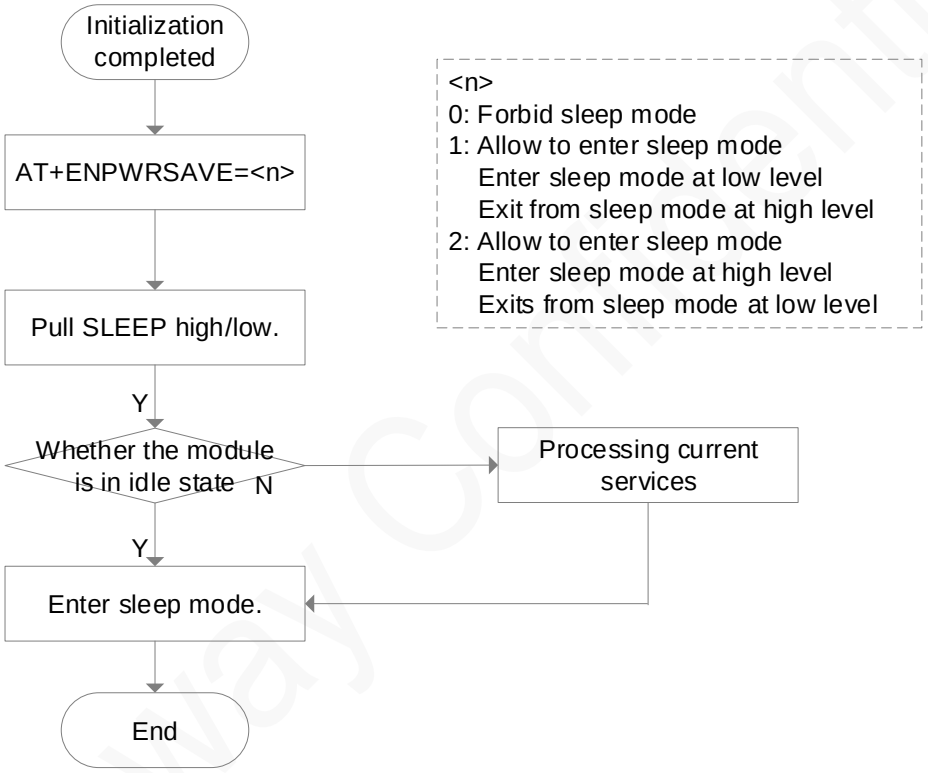
Note that an ESD component should be added to protect the USB_BOOT pin.

5.2.4 SLEEP

The SLEEP pin is used to control sleep mode of the module, it needs to be used together with the AT commands. For details, see the *Neoway*_N723-EA_*AT Command Manual*. In sleep mode, the module can also respond to incoming call, SMS, and data service in time.

The following figure shows the process of entering sleep mode:

Figure 5-14 Process of entering the sleep mode



The following figure shows the process of exiting from sleep mode:

Figure 5-15 Process of exiting from sleep mode

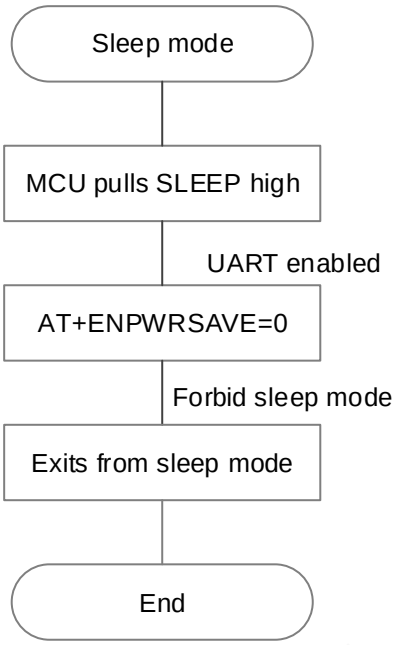


Figure 5-16 Incoming call service process

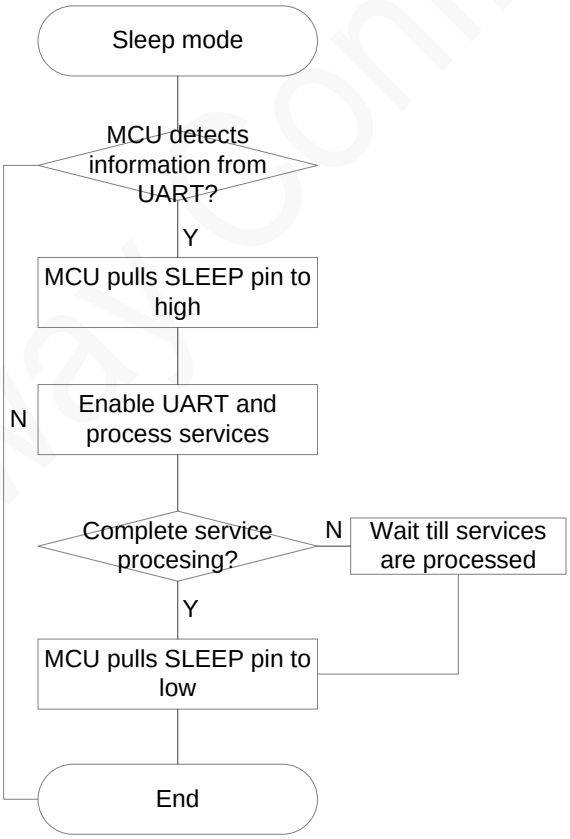
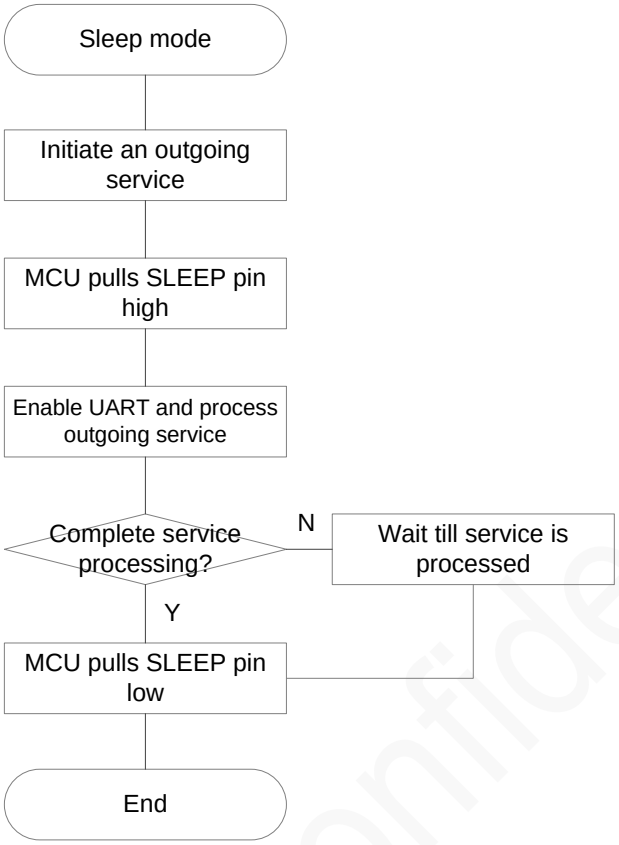


Figure 5-17 Outgoing call service process



5.3 Peripheral Interfaces

N723-EA provides various peripheral interfaces.

In all reference designs of this section, the receiving and sending directions included in the pin names of the peripheral interface of the module are based on the module, whereas peripheral pins are named based on the components. For example, **UART_TXD** indicates the pin used by the module to send data, and **MCU_RXD** indicates the pin used by the MCU to receive data. These two pins should be connected.

In the process of MCU selection and design, note whether the signal naming of pins is based on the module or the MCU.

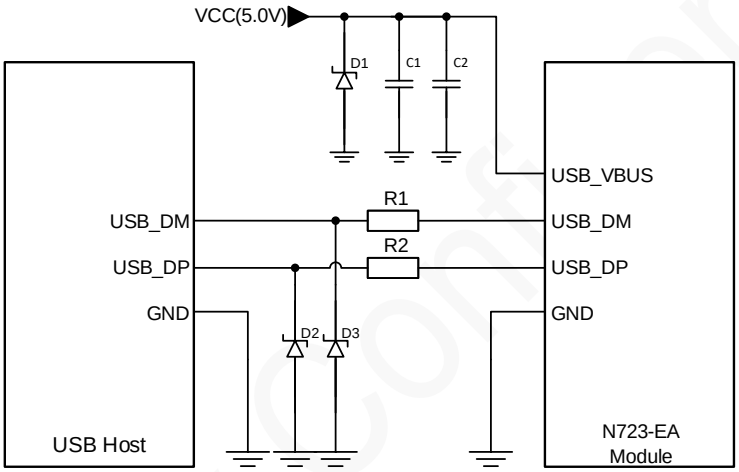
5.3.1 USB

Signal	Pin	I/O	Function description	Remarks
USB_VBUS	40	PI	USB insertion detection pin	USB_VBUS=3.5 V - 5.2 V, typical value: 5.0 V.
USB_DM	41	IO	USB data negative signal	USB 2.0. This pin is used for software

USB_DP	42	IO	USB data positive signal	download and data transmission. DM and DP adopt differential routing, and the differential impedance must be 90 Ω.
USB_ID	43	DI	USB ID pin	Used for OTG function. Leave this pin floating if it is not used.

N723-EA can implement program download, data communication, and debugging through the USB interface. The module's USB is as a slave device by default. Figure 5-18 shows the recommended USB connection circuit.

Figure 5-18 Reference USB connection design



Schematic Design Guidelines:

- Connect a 1 μF (C1) and a 33 Pf (C2) filter capacitors in parallel to the USB_VBUS pin. An ESD component must be added for the power cable.
- The junction capacitance of the ESD components D2 and D3 on the USB_DP and USB_DM data lines must be smaller than 0.5 pF.
- Connecting a resistor less than 10 Ω in series to each of the USB_DP and USB_DM cables can effectively improve the ESD performance of the USB.

PCB Design Guidelines:

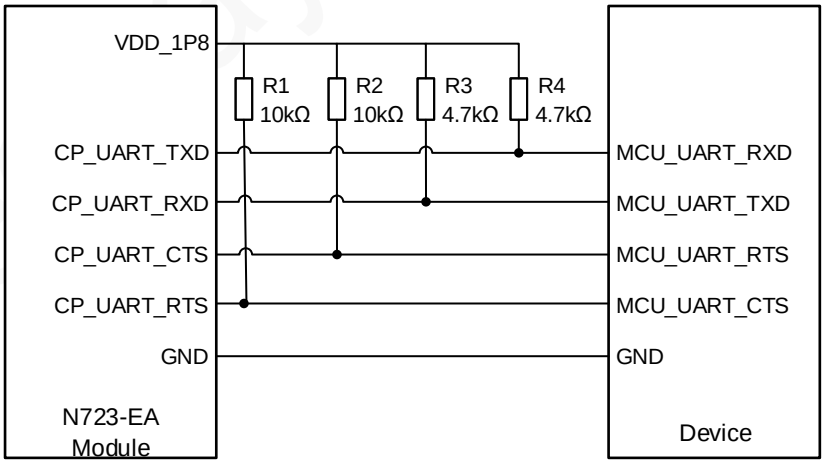
- Place the filter capacitor on the USB_VBUS as close as possible to the module pins, and place the ESD component as close as possible to the USB connector.
- Place the ESD component on the USB_DP and USB_DM as close to the USB connector as possible.
- USB data lines must adopt differential routing, and the differential impedance must be 90 Ω. The cable from the port to the module must be isolated from other signal cables and must be wrapped by ground cables.

5.3.2 UART

Signal	Pin	I/O	Function description	Remarks
CP_UART_TXD	46	DO	Data transmitting	Used for AT commands communication and support hardware flow control. Leave this pin floating if it is not used.
CP_UART_RXD	47	DI	Data receiving	
CP_UART_CTS	51	DI	The user allows the module to send data.	
CP_UART_RTS	52	DO	The module requests the user to send data.	
DEBUG_UART1_TXD	65	DO	Data transmitting	Only used for debug. Leave this pin floating if it is not used.
DEBUG_UART1_RXD	66	DI	Data receiving	
UART2_TXD	69	DO	Data transmitting	Used for data transmission. Leave this pin floating if it is not used.
UART2_RXD	70	DI	Data receiving	

N723-EA provides three UART interfaces, of which the CP_UART interface supports hardware flow control and a maximum rate of 3.6 Mbps. DEBUG_UART1 only supports for debugging, there will be Log information output after the module boots up, and the baud rate supports up to 115200 bps. UART2 can be used for data communication of external devices, and the baud rate supports up to 115200 bps. Figure 5-19 shows the reference design of the UART interface. All the UART interfaces of the module are 1.8 V level.

Figure 5-19 Reference design of the UART connection



Schematic Design Guidelines:

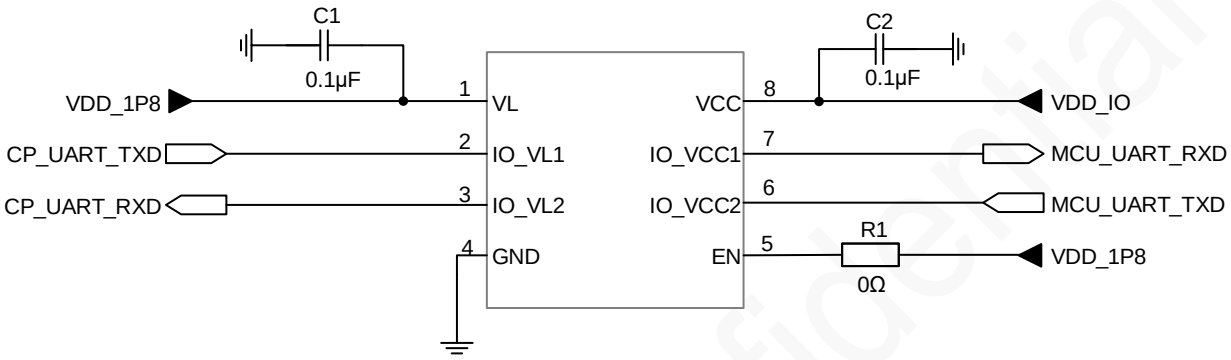
- Pay attention to the corresponding relations between the signal direction and the connection.

- It is prohibited to use diodes for level shifting.

If the UART does not match the logic voltage of the MCU, add a level shifting circuit outside of the module. Three level shifting circuits are recommended based on the differences in logic levels and rates.

- If the serial port baud rate is greater than 115200 bps, it is recommended to refer to the recommended level shifting circuit 1. See Figure 5-20.

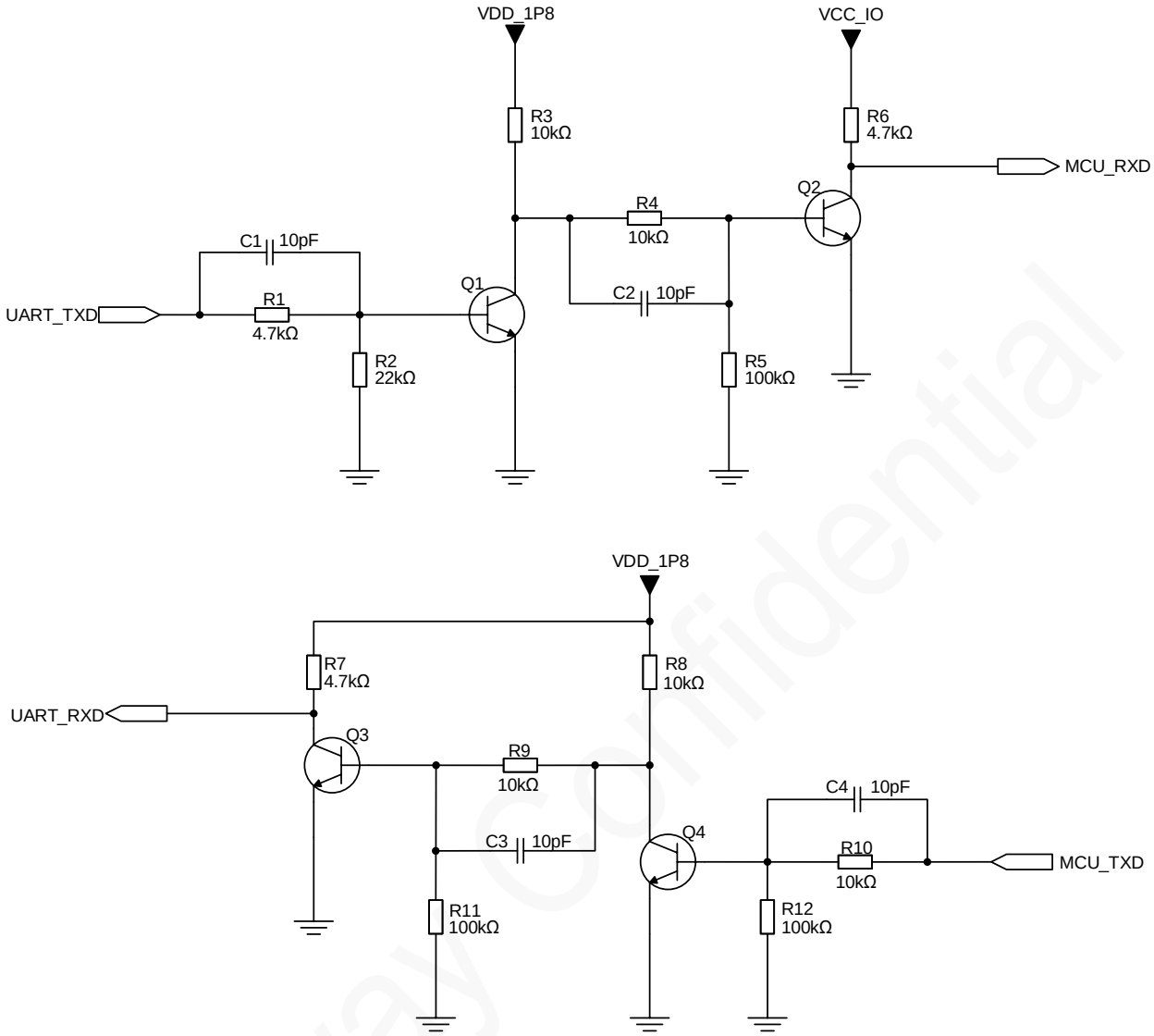
Figure 5-20 Recommended level shifting circuit 1



  - VL is the reference voltage of IO_VL1 and IO_VL2.
  - VCC is the reference voltage of IO_VCC1 and IO_VCC2.
  - EN is the enable pin. In the above circuit, the EN pin is connected to VDD_1P8 and the level shifter is always working.

- If the serial port baud rate is less than or equal to 115200 bps, designing the serial port TXD and RXD by referring to recommended level shifting circuit 2 is recommended. As shown in Figure 5-21.

Figure 5-21 Recommended level shifting circuit 2

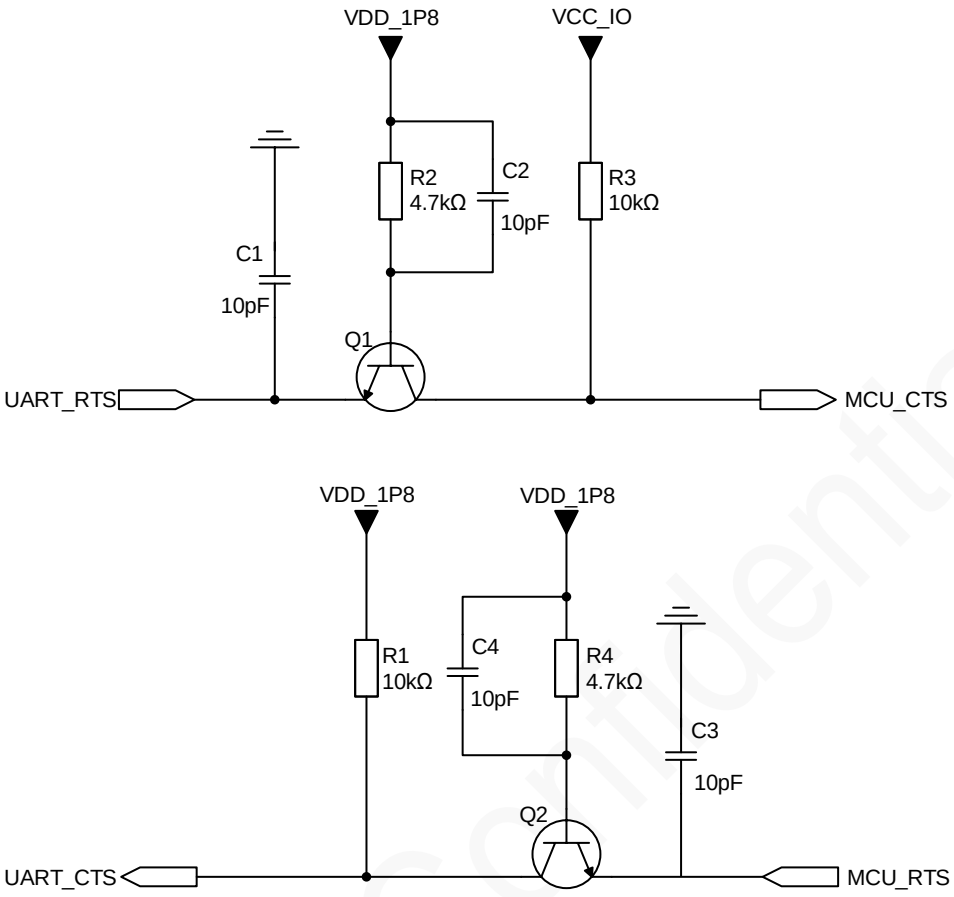


PCB design guideline:

- Q1/Q2: MMBT3904 or MMBT2222 High-speed transistors are better.
- MCU_TXD and MCU_RXD are the sending and receiving ports of the MCU respectively, and TXD and RXD are the sending and receiving ports of the module respectively. VCC_IO is the IO voltage of the MCU. VDD_1P8 is the IO voltage of the module.

- If the serial port baud rate is less than or equal to 115200 bps, designing the CTS and RTS circuit by referring to recommended level shifting circuit 3 is recommended. As shown in Figure 5-22.

Figure 5-22 Recommended level shifting circuit 3



MCU_CTS and MCU_RTS are the MCU-side signals; UART_CTS and UART_RTS are the module-side signals. VCC_IO is the IO voltage of the MCU. VDD_1P8 is the IO voltage of the module.

Schematic Design Guidelines:

- Ensure that the voltage difference between the high-level and low-level sides be equal to or less than 2 V.
- For the accelerating capacitor, adjust it according to the actual test conditions; it is recommended to reserve the capacitor.
- The base voltage of the transistor is the lower voltage between both sides.
- The circuit convert the voltage level through the turn-on and turn-off of the triode, and the level conversion is unidirectional. Pay attention to the signal flow.

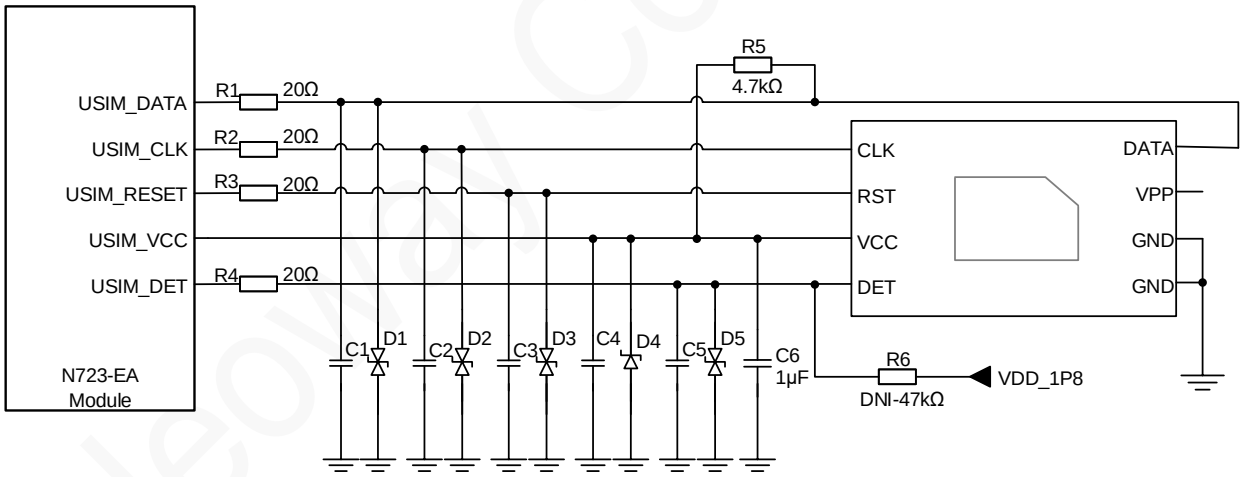
Do Not directly apply the voltage and resistance values in the circuit to your circuit design; they need to be adjusted according to the actual situations. Note the difference between different level shifting circuits.

5.3.3 USIM

Signal	Pin	I/O	Function description	Remarks
USIM_VCC	35	PO	USIM power output	1.8 V/3.0 V (self-adaptive)
USIM_DATA	36	B	USIM data input and output	Connecting a 4.7 kΩ pull-up resistor to USIM_VCC is required.
USIM_CLK	37	DO	USIM clock output	Leave this pin floating if it is not used.
USIM_RESET	38	DO	USIM reset	Leave this pin floating if it is not used.
USIM_DET	39	DI	USIM detection	Connecting this pin to VDD_1P8 through a 47 kΩ pull-up resistor is required.

N723-EA provides one USIM card interface. Figure 5-23 shows the reference design of the USIM card interface.

Figure 5-23 Reference design of the USIM card interface



Schematic Design Guidelines:

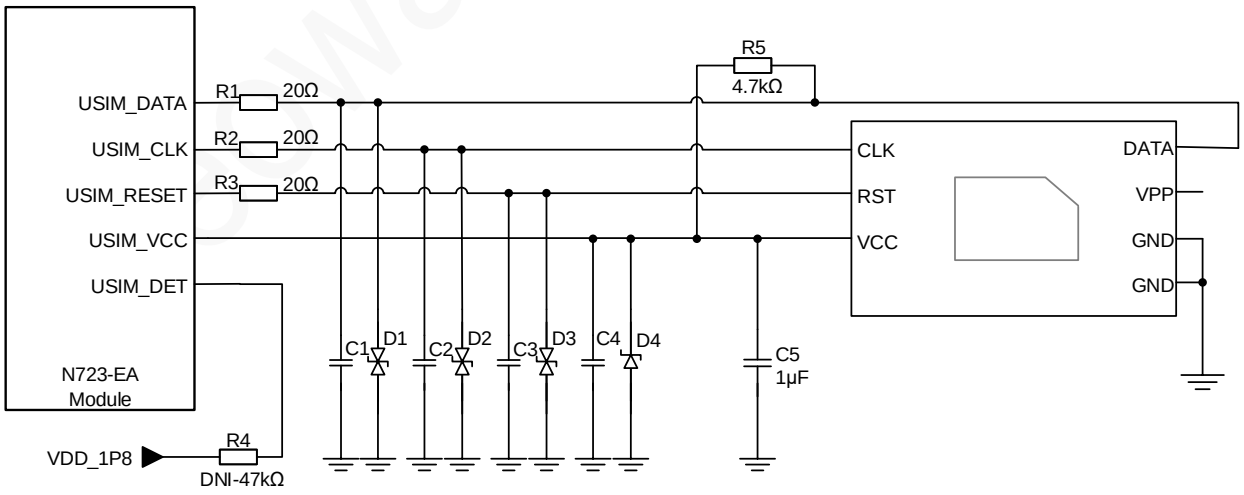
- USIM_VCC is the pin to supply power for USIM card and its maximum load is 50 mA. It is only used as power supply for USIM card (forbidden to supply power to other loads).
- Add a pull-up resistor externally to pull up the USIM_DATA pin to USIM_VCC since there is no internal pull-up on USIM_DATA.

- In applications with complex electromagnetic environments that have high requirements for ESD protection, it is recommended to add ESD protection diodes (junction capacitance ≤ 7 pF) on each signal cable.
- Connect a 20 Ω resistor respectively to USIM_DATA, USIM_RST, USIM_CLK, and USIM_DET (close to the card connector) in series to enhance the ESD performance.
- C1 - C5 are designed to place the high-frequency filter capacitors. The recommended capacitance value is less than or equal to 10 pF. No capacitors are placed on them by default in design. Please adjust it according to the actual debugging results.
- Connect a 20 Ω resistor respectively to USIM_DATA, USIM_RST, USIM_CLK, and USIM_DET (close to the module) in series to enhance the ESD performance.
- The DET pin status of the SIM card connector in Figure 5-23 is: when the SIM card is inserted, DET is connected to GND, and when the SIM card is pulled out, DET and GND are disconnected.

N723-EA supports USIM card detection. USIM_DET is a 1.8 V interrupt pin. The USIM detection circuit works by checking the levels across the USIM_DET pin before and after a USIM card is inserted. The reference design circuit assumes that the SIM-DET is unconnected before the USIM card is inserted, and the SIM-DET pin is grounded after the USIM card is inserted. At this time, the low level indicates that the USIM card is detected, and the high level indicates that the USIM card is not detected. If the insertion detection function is not required, refer to Figure 5-24.

The SIM card hot-swap function needs to be supported by the corresponding firmware version, and different the card connector types have different configurations in firmware. If you require the SIM card hot-swap function, it is recommended to confirm the current configuration of the module firmware with Neoway FAEs.

Figure 5-24 Reference design of the USIM card (without hot-swap) interface

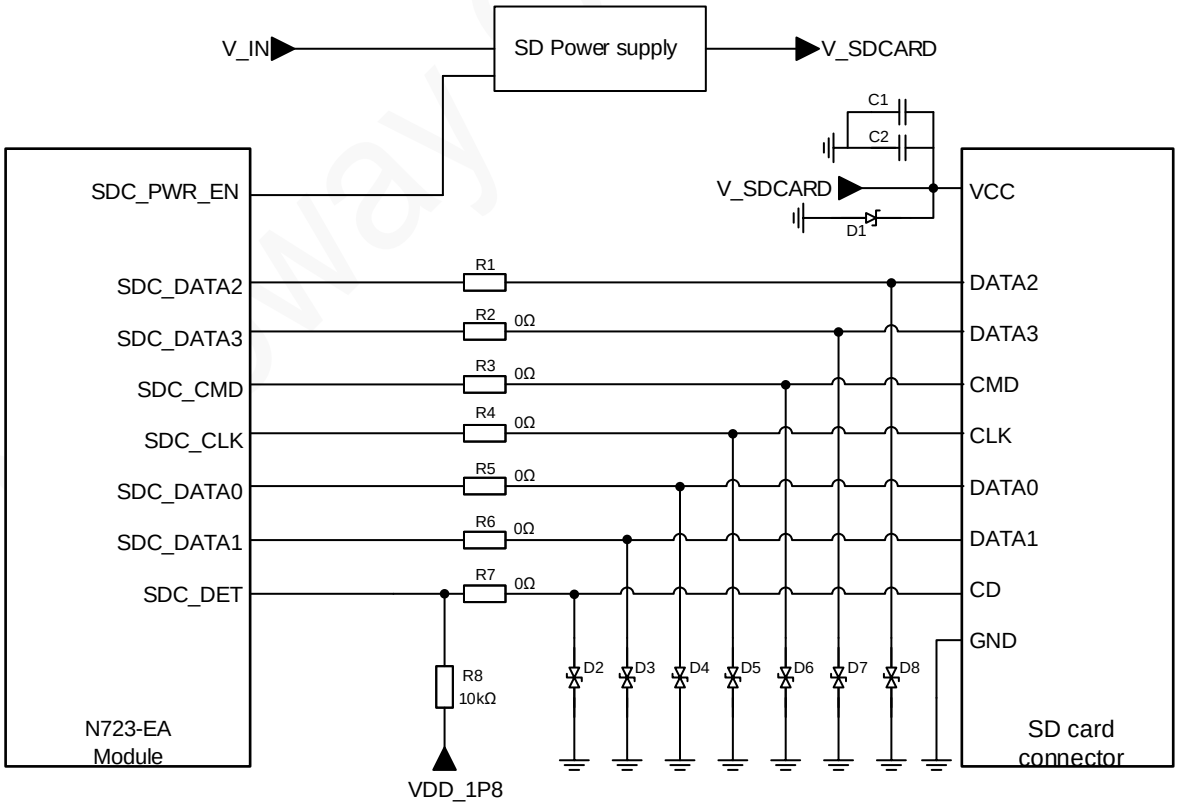


5.3.4 SD/eMMC

Signal	Pin	I/O	Function description	Remarks
SDC_PWR_EN	2	DO	Control of the external power supply for SD/eMMC	Leave these pins floating if not used.
SDC_DATA_2	3	B	SD/eMMC data 2	
SDC_DATA_3	4	B	SD/eMMC data 3	
SDC_CMD	5	DO	SD/eMMC command control	
SDC_CLK	6	DO	SD/eMMC clock	
SDC_DATA_0	7	B	SD/eMMC data 0	
SDC_DATA_1	8	B	SD/eMMC data 1	
SDC_DET	96	DI	SD/eMMC detect input	

N723-EA provides one SD/eMMC interface, which supports 1.8 V/3.0 V dual voltages, supports clock frequencies up to HS200-200MHz and DDR50-50MHz, and can be backwards compatible with the DS, HS, SDR12, SDR25, SDR50, and SDR104 modes. It can be connected to SD card or eMMC chip.

Figure 5-25 Reference design of the SDC interface



Schematic Design Guidelines:

- The SDC_PWR_EN and SDC_DET pins only support 1.8 V level.
- It is recommended to reserve the positions for pull-up resistors on the SD/eMMC lins.
- When using a SD card not supporting 1.8 V level, change the pull-up power supply of the SD/eMMC signal to the corresponding power supply domain.
- Control the equal length for the SDC/MMC interface. For the specific equal length requirements, see the requirements of the corresponding WLAN chip or module.

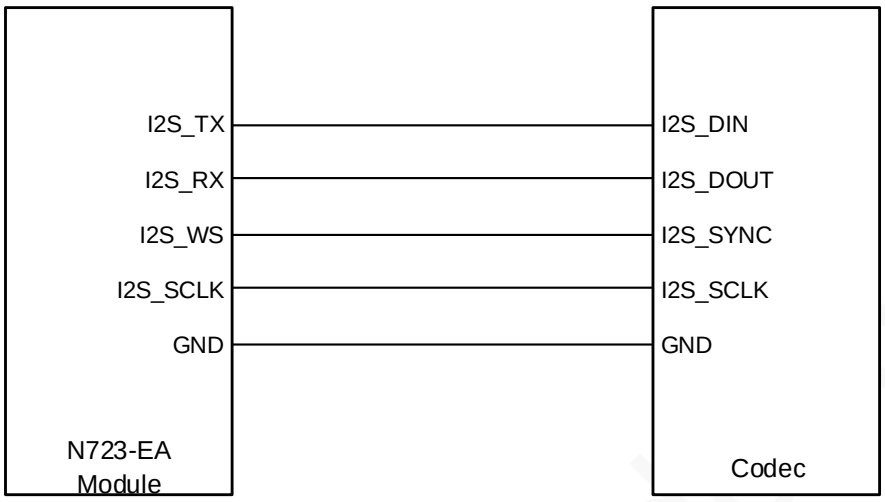
5.3.5 I2S

The I2S_MCLK pin has internal pull-up or pull down; do not add a pull-up or pull-down resistor outside the module when this pin is in use.

Signal	Pin	I/O	Function description	Remarks
I2S_SCLK	9	DO	I2S data clock	Leave this pin floating if it is not used.
I2S_TX	10	DO	I2S data sending	Leave this pin floating if it is not used.
I2S_RX	11	DI	I2S data receiving	Leave this pin floating if it is not used.
I2S_WS	12	B	I2S right and right channels selection	Leave this pin floating if it is not used.
I2S_MCLK	64	DO	I2S master clock	26 MHz by default

N723-EA provides one PCM/I2S interface, supporting 1.8 V level. The following figure shows the reference design of the I2C interface:

Figure 5-26 Reference design of the I2S



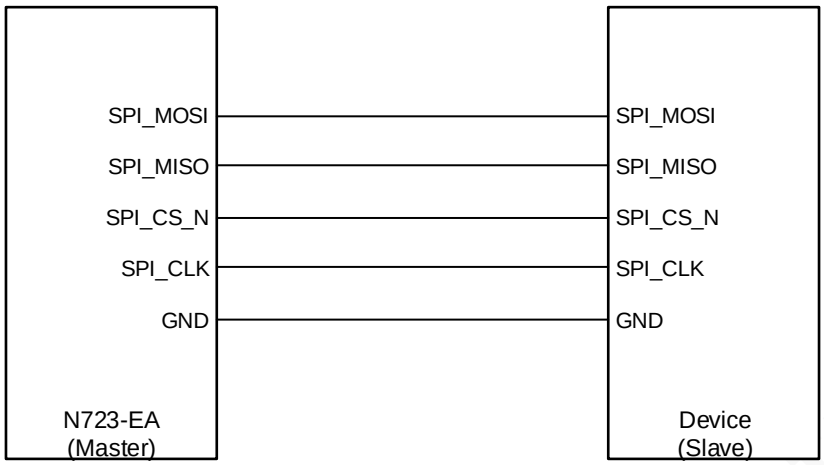
If you need to use the PCM/I2S function, contact Neoway FAEs.

5.3.6 SPI

Signal	Pin	I/O	Function description
SPI_CLK	84	DO	Clock signal
SPI_MISO	85	DI	Output of the slave device and input of the master device
SPI_MOSI	86	DO	Input of the slave device and output of the master device
SPI_CS_N	87	DO	Chip select signal of the slave device

The SPI interface supports 1.8 V and only master mode. The following figure provides the SPI connection.

Figure 5-27 SPI reference design



5.3.7 I2C

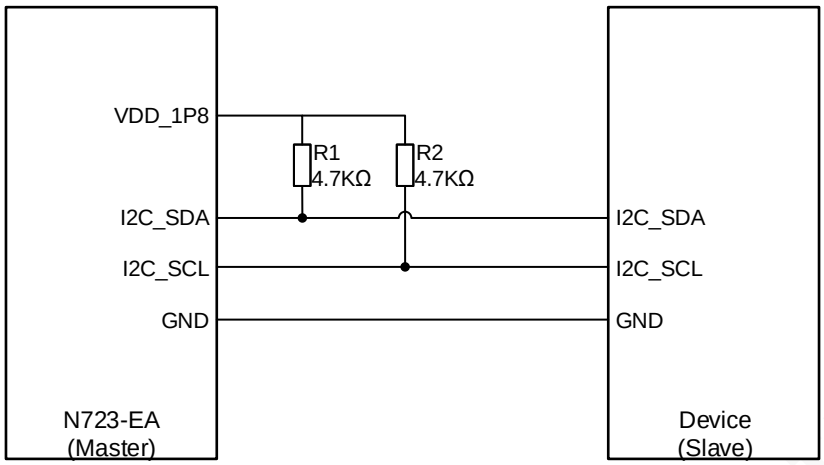
Signal	Pin	I/O	Function description	Remarks
I2C_SDA	81	B	I2C data	Connecting an external 4.7 kΩ pull-up resistor is required.
I2C_SCL	82	DO	I2C clock	

Table 5-1 I2C interface parameters

IO level	Supported mode	Supported speed
1.8 V	Standard mode	100 kbps
	Fast mode	400 kbps

N723-EA provides only one I2C interface, which supports only master mode and 1.8 V level. There are no pull-up resistors internally. Connecting an external pull-up resistor is required to prevent the lack of I2C drive capability. The following figure shows the reference design of the I2C interface:

Figure 5-28 Reference design of the I2C



Schematic Design Guidelines:

If the level of the slave device does not match that of the N723-EA, level conversion is required; see Figure 5-20 Recommended level shifting circuit 1.

PCB Design Guidelines:

- Avoid cross routing between the I2C cable and other signal cables as much as possible. If cross-routing cannot be avoided, keep the signal cables perpendicular to other cables to reduce coupling.
- Keep the signal cables away from areas where static electricity may be introduced as much as possible.
- It is recommended that signal cables be wrapped with left and right ground wires.

5.4 Network and Connection

N723-EA supports Ethernet and Wi-Fi network connection methods.

5.4.1 Ethernet

RMII

Signal	Pin	I/O	Function description	Remarks
RMII_TX_D0	16	DO	Data sending bit 0	Leave this pin floating if it is not used.
RMII_TX_D1	15	DO	Data sending bit 1	Leave this pin floating if it is not used.
RMII_RX_D0	19	DI	Data receiving bit 0	Leave this pin floating if it is not used.
RMII_RX_D1	18	DI	Data receiving bit 1	Leave this pin floating if it is not used.

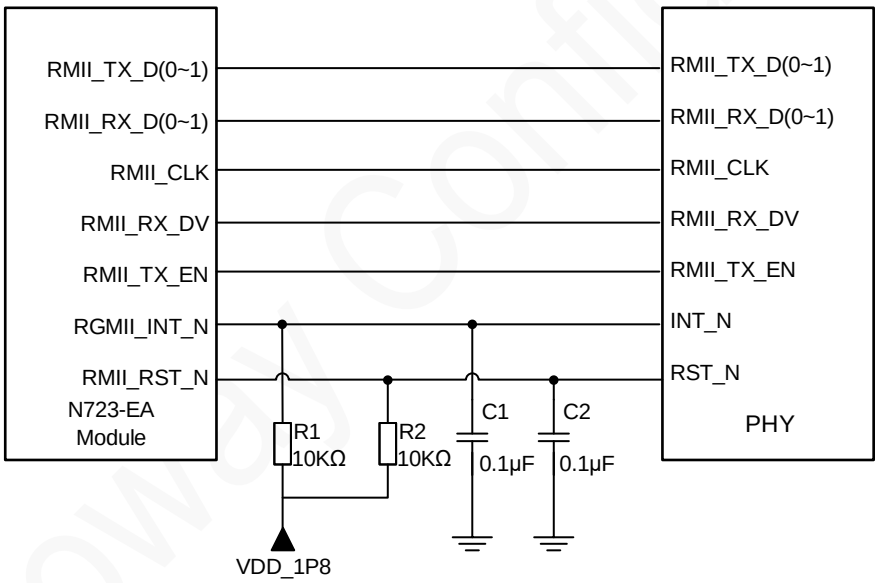
RMII_CLK	21	DI	Data clock	Leave this pin floating if it is not used.
RMII_RX_DV	24	DI	Valid when receiving data	Leave this pin floating if it is not used.
RMII_TX_EN	25	DO	Enable data sending	Leave this pin floating if it is not used.
RMII_INT_N	90	DI	Interrupt input	Leave this pin floating if it is not used.
RMII_RST_N	78	DO	Reset signal output	Leave this pin floating if it is not used.

If you need to use the RMII function, contact Neoway FAEs.

The RMII interface voltage is 1.8 V by default. Whether the interface supports 3.3 V level depends on the hardware; please contact Neoway FAEs if required.

The RMII interfaces are used for Ethernet connection, and the interface level is 1.8 V by default. The following figure shows the RMII interface reference design.

Figure 5-29 Reference design of the RMII interface



Design Guideline:

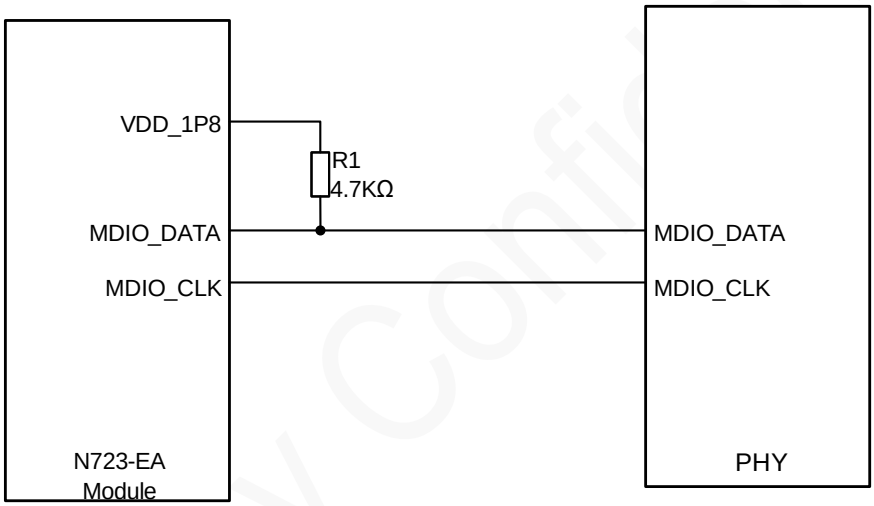
- Pay attention to the corresponding relationship of the RMII connection. For details, read the PHY chip manual.
- Control the equal length for the TX and RX traces. For the trace length, refer to the PHY chip manual.
- Control the impedance for the TX and RX traces to 50 Ω. The clock must be wrapped by ground.
- Ensure that the TX and RX trace spacing is larger than 3 times the trace width. Ensure that the RGMII and other trace spacing is larger than 3 times the trace width.

MDIO

Signal	Pin	I/O	Function description	Remarks
MDIO_CLK	22	DO	MDIO clock	-
MDIO_DATA	23	B	MDIO data input and output	Connecting an external 4.7 kΩ pull-up resistor is required.

MDIO supports up to 25 MHz frequency and only 1.8 V level. The following figure shows a reference design of the SDIO interface with a PHY chip:

Figure 5-30 Reference design of the SDIO interface with a PHY chip:



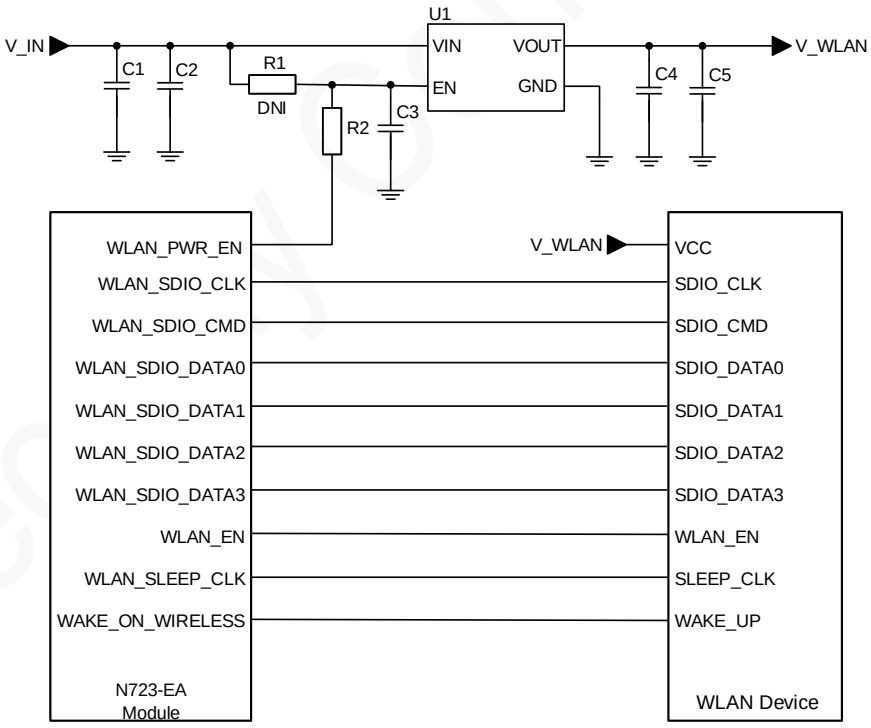
5.4.2 SDIO/WLAN

Signal	Pin	I/O	Function description	Remarks
WLAN_SDIO_CMD	54	B	SDIO command	Leave this pin floating if it is not used.
WLAN_SDIO_CLK	55	DO	SDIO clock	Leave this pin floating if it is not used.
WLAN_SDIO_DATA0	56	B	SDIO data bit 0	Leave this pin floating if it is not used.
WLAN_SDIO_DATA1	57	B	SDIO data bit 1	Leave this pin floating if it is not used.
WLAN_SDIO_DATA2	58	B	SDIO data bit 2	Leave this pin floating if it is not used.

WLAN_SDIO_DATA3	59	B	SDIO data bit 3	Leave this pin floating if it is not used.
WAKE_ON_WIRELESS	60	DO	WLAN wakeup control	Leave this pin floating if it is not used.
WLAN_SLEEP_CLK	61	DO	Wi-Fi sleep clock	Clock frequency: 32 KHz. Leave this pin floating if it is not used.
WLAN_EN	62	DO	WLAN enable control	Leave this pin floating if it is not used.
WLAN_PWR_EN	63	DO	Control of the external power supply for WLAN	Leave this pin floating if it is not used.

The SDIO interface supports only 1.8 V voltage and SDIO2.0 and SDIO3.0 for Wi-Fi connections. Its clock supports up to HS200-200MHz, SDR50-100MHz or DDR50-50MHz frequency. The following figure shows a reference design of the SDIO interface:

Figure 5-31 SDIO reference design



Design Guideline:

- If the load has a pull-up resistor requirement pay attention to the resistance. It is recommended to use VDD_1P8 of the module.

- Control the equal length for the SDIO interface. For the specific equal length requirements, see the requirements of the corresponding WLAN chip or module.
- Spacing between DATA traces should be larger than 2 times trace width.
- Control the impedance for each SDIO trace to 50 Ω.

5.5 GPIO interfaces

Signal	Pin	I/O	Function description	Remarks
GPIO_12	67	B	GPIO with interrupt	This pin is pulled up to V1.8 V by default. Leave this pin floating if it is not used.
GPIO_05	68	B	GPIO with interrupt	This pin is pulled up to V1.8 V by default. Leave this pin floating if it is not used.
GPIO_04	71	B	GPIO with interrupt	This pin is pulled up to V1.8 V by default. Leave this pin floating if it is not used.
GPIO_13	72	B	GPIO with interrupt	This pin is pulled down to GND by default. Leave this pin floating if it is not used.

N723-EA provides 4 GPIO interfaces, all of which have the interrupt function. The AT commands can be used to control the GPIO status. For more details about the GPIO interfaces, contact Neoway FAEs.

The default function of the GPIO pin may vary with different firmware versions. If you need to use the GPIO interrupt function, contact Neoway FAEs.

5.6 RF Interface

Signal	Pin	I/O	Function description	Remarks
ANT_MAIN	76	AI	2G/3G/4G main antenna pin	50 Ω impedance characteristics
ANT_DIV	94	AI	4G diversity antenna pin	

5.6.1 ANT_MAIN/ANT_DIV Antenna Interfaces

The MAIN/DIV antenna interface of the N723-EA module requires the 50 Ω impedance characteristic. The impedance of the cable from the module interface to the antenna needs to be kept within the impedance range to ensure RF performance. Therefore, you should control the impedance of the traces between the pins and antenna to ensure the RF performance. An impedance matching circuit,

such as the L network, split capacitor network, and pi network is mandatory in between. Pi network is recommended.

Figure 5-32 L-type network

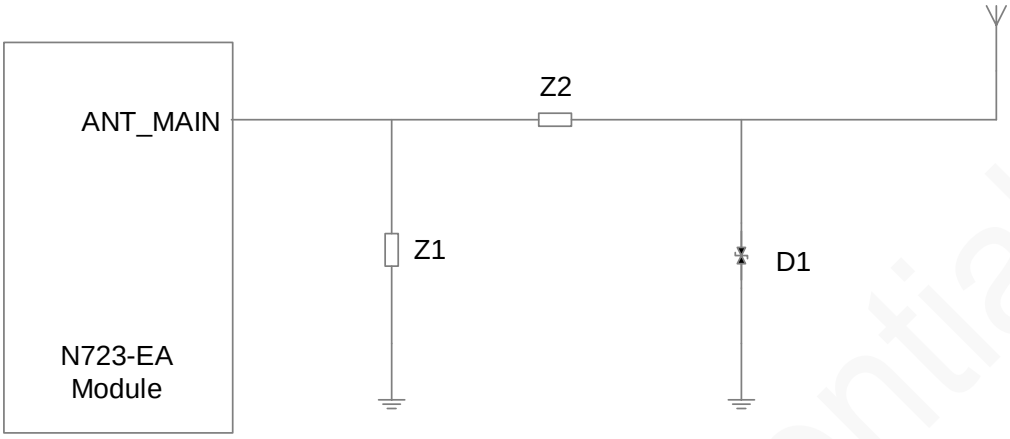


Figure 5-33 T-type network

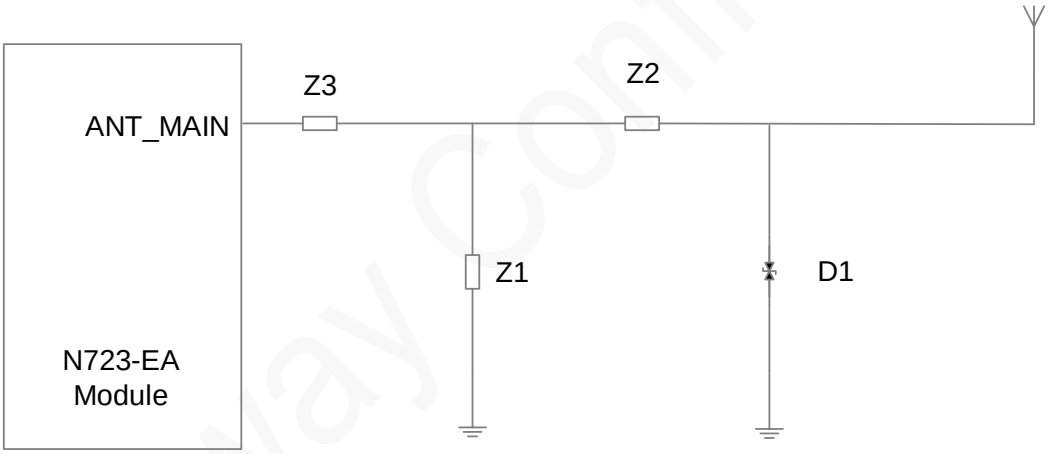
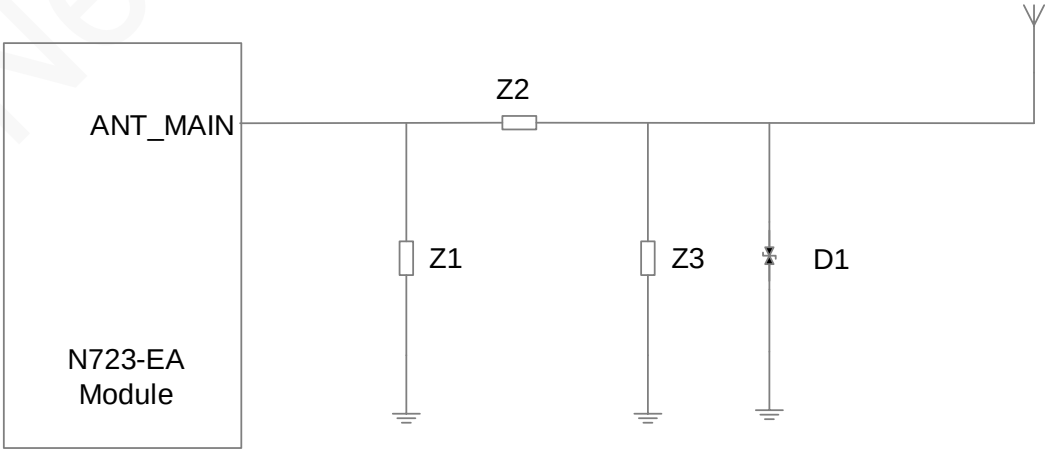


Figure 5-34 π-type network



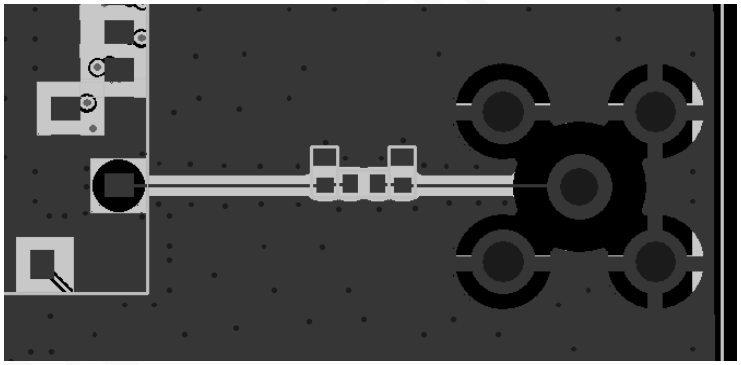
Schematic Design Guidelines:

- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- If static electricity is introduced at the antenna, it is recommended that electrostatic protection be added. You can use a TVS tube with ultra-low junction capacitance. It is recommended that you use a TVS tube with a junction capacitance less than 0.5pF. In addition, you must ensure that the reverse breakdown voltage of the TVS tube is greater than 10V. TVS tubes with a reverse breakdown voltage of 15V or more are recommended.

PCB Design Guidelines:

- Lay copper foil around the RF connector. Dig as many ground holes as possible on the copper to ensure 50 Ω impedance in the trace.
- The trace between the pin and the antenna connector should be as short as possible. Control the trace impedance to 50 Ω.
- If you adopt an SMA connector, a big RF solder pad might result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and fourth layers or all layers of a multiple-layer PCB under the RF solder pad.

Figure 5-35 Recommended RF PCB design



- A reasonable distance should be kept between ANT_MAIN and ANT_DIV to avoid mutual interference that may affect reception performance.
- On the PCB, keep the RF signals and components far away from high-speed circuits, power supplies, transformers, great inductors, the clock, etc.

5.6.2 Antenna Assembling

The antenna used by the module must comply with the mobile device standard. The standing wave ratio should be between 1.1 and 1.5, and the input impedance should be 50 Ω. Requirements for antenna gain vary according to the application environment. In general, the greater the in-band gain and the smaller the out-of-band gain, the better the performance of the antenna.

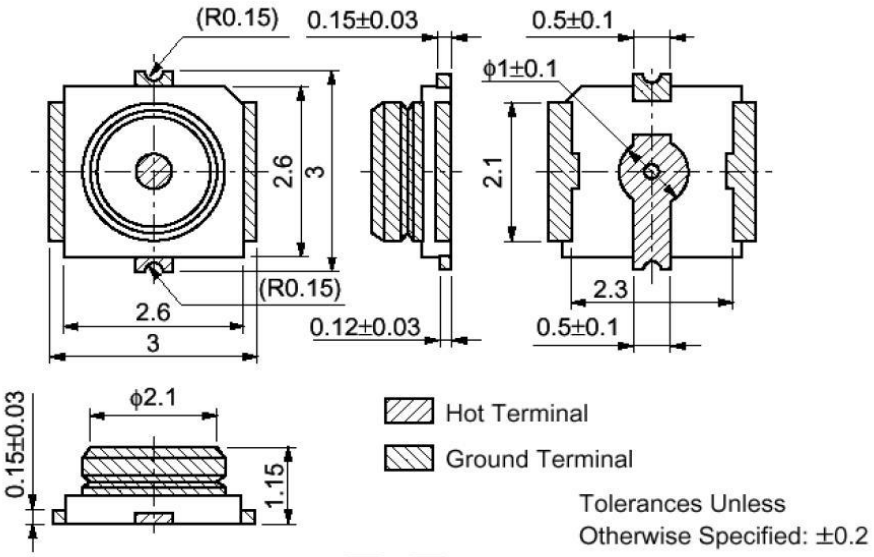
Antenna interfaces can be connected to a rubber ducky antenna, magnet antenna, or embedded

Planar Inverted F Antenna (PIFA). Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.

The following methods are commonly used to assemble antenna:

- GSC RF connector
  MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

Figure 5-36 Murata RF connector encapsulation specifications



- The RF cable is connected to the module by means of soldering. However, this method has the stability, consistency, and RF performance degradation issues, and therefore is not recommended.

  The following figure shows the effect of the connection methods.

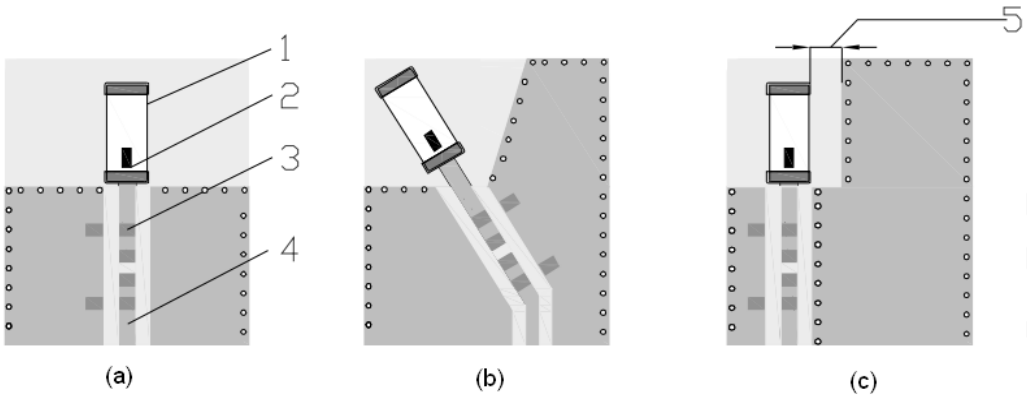
Figure 5-37 RF cable connections

- PCB Printing or SMT

  The module works in a wide frequency range, but it is difficult for PCB antennas or ceramic antennas to cover a wide frequency. Therefore, this connection method is recommended only for 2.4 GHz Wi-Fi or BT/BLE antennas.

The following figure shows the layout of the 2.4 GHz ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

Figure 5-38 Antenna layout

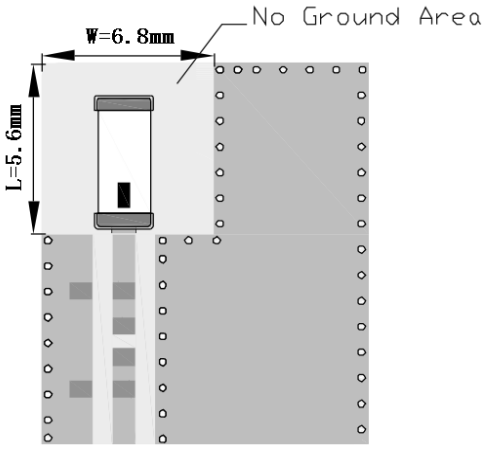


If your PCB is large enough, you can adopt the layout shown in Figure 5-38 (a).

- 1 Chip antenna
- 2 Feeding mark
- 3 Layout pad of the matching circuit
- 4 50 Ω transmission line

Figure 5-39 shows the layout for the area between the antenna and ground that is marked as "5" in Figure 5-38.

Figure 5-39 Layout around the antenna



For more details, refer to the antenna manuals and other documents.

5.7 Multi-Function Interfaces

Table 5-2 Pin definition description

Pin	Function (default)	Multiplexed function 1	Remarks
9	I2S_SCLK	PCM_CLK	-
10	I2S_TX	PCM_DOUT	-
11	I2S_RX	PCM_DIN	-
12	I2S_WS	PCM_SYNC	-

If you need to multiplex the pin function, ensure that the firmware supports multiplexing; for details, consult Neoway FAEs.

5.8 Other Interfaces

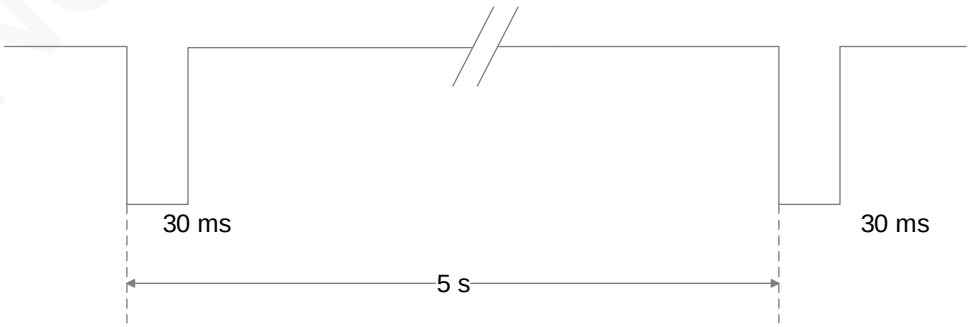
Signal	Pin	I/O	Function description	Remarks
RING	13	DO	Incoming call indicator control	-
NET_LIGHT	83	DO	Network indicator control	-

5.8.1 RING

- RING indicator for an incoming call

  Once a voice call is incoming, the UART port outputs "RING" character strings and meanwhile the RING pin outputs a negative pulse with a width of 30 ms and a period of 5 seconds. After the call is answered, the pin restores to high-level output.

Figure 5-40 Pulse wave for an incoming call



- RING indicator for SMS

  Upon receipt of an SMS message, the RING pin outputs a negative pulse of 35 ms. As shown in the following figure.

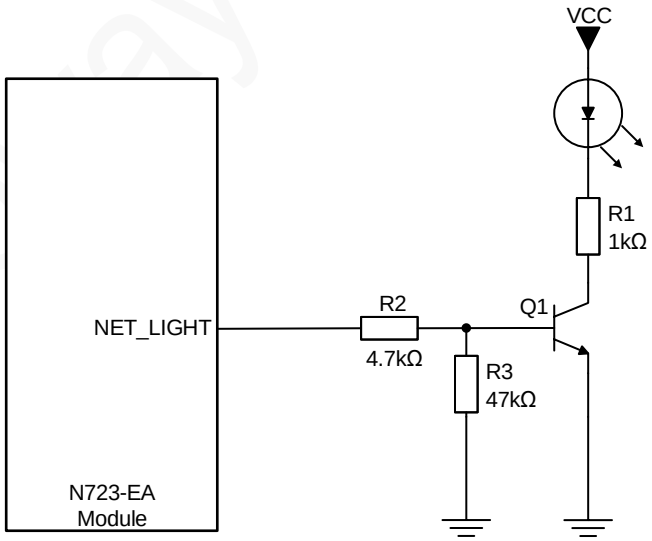
Figure 5-41 RING indicator for SMS

5.8.2 NET_LIGHT

NET_LIGHT is the network status indicator pin of the module. It outputs PMW waves of duty cycle varying with the status of the module and drives an LED indicator to blink at different frequencies. You can use the AT command to enable the LED indicator to blink in different states. For details, see *Neoway_N723-EA_AT_Command_Manual.*

Do not use NET_LIGHT to drive the LED indicator directly since it outputs a high level of 1.8 V. It is recommended to drive the LED indicator by controlling a triode.

Figure 5-42 Driving LED with a triode



6 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the N723-EA module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

6.1 Electrical Characteristics

- If the voltage is lower than threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it outputs at least 2.5 A current. The 2.5 A current occurs when the module is working at the maximum power level of the GSM mode. The peak current during burst transmission has a short duration. Placing a large capacitor on the VBAT pin of the module can effectively enhance the flyback capability of the power supply and avoid excessive voltage drops that may cause exceptions, such as module shutdown.

Table 6-1 N723-EAElectrical Characteristics

Parameter		Minimum Value	Typical Value	Maximum Value
VBAT	V_{in}	3.4 V	3.8 V	4.2 V
	I_{in}	N/A	N/A	2.5 A

Table 6-2 N723-EA current consumption (Typical)

Status / Network Standard and Band	Sleep (mA)	Idle (DRX) (mA)	Active (mA) @max power
LTE-FDD: B1, B3, B5, B8, B20, B28	≤4.0	≤31	≤630
LTE-TDD: B38, B40, B41	≤4.0	≤31	≤410
WCDMA: B1, B5, B8	≤4.0	≤31	≤596
GSM900	≤4.0	≤31	≤643
GSM1800	≤4.0	≤31	≤870

6.2 Temperature Characteristics

Table 6-3 N723-EA temperature features

Parameter	Minimum Value	Typical Value	Maximum Value
Operating	-30℃	25℃	75℃
Extended	-40℃	25℃	85℃
Storage	-40℃	25℃	90℃

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse but it can still work properly.

6.3 ESD Protection

During the process of R&D, production testing, assembly, and transportation, electronic products may discharge the product through some means, which may cause damage to the module, so the ESD protection design of the product is very important. The following is the ESD protection capability (test performed using the EVB) of the main pins of the module. When designing related products, you need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25℃

Table 6-4 N723-EA ESD protection features

Testing Point	Contact Discharge	Air Discharge
GND	±8 kV	±15 kV
ANT	±8 kV	±15 kV
Cover	±8 kV	±15 kV

7 RF Characteristics

N723-EA supports GSM, WCDMA, FDD-LTE, and TDD-LTE (Cat.4) network modes. This chapter describes the RF characteristics of N723-EA.

7.1 Operating Band

Table 7-1 N723-EA operating bands

Operating band	Uplink	Downlink
EGSM900	880 - 915MHz	925 - 960MHz
DCS1800	1710 - 1785 MHz	1805 - 1880MHz
WCDMA B1	1920 - 1980MHz	2110 - 2170MHz
WCDMA B5	824 - 849MHz	869 - 894MHz
WCDMA B8	880 - 915MHz	925 - 960MHz
FDD-LTE B1	1920 - 1980MHz	2110 - 2170MHz
FDD-LTE B3	1710 - 1785 MHz	1805 - 1880MHz
FDD-LTE B5	824 - 849MHz	869 - 894MHz
FDD-LTE B7	2500 - 2570MHz	2620 - 2690MHz
FDD-LTE B8	880 - 915MHz	925 - 960MHz
FDD-LTE B20	832 - 862MHz	791 - 821MHz
FDD-LTE B28	703 - 748MHz	758 - 803MHz
TDD-LTE B38	2570 - 2620MHz	2570 - 2620MHz
TDD-LTE B40	2300 - 2400MHz	2300 - 2400MHz
TDD-LTE B41	2535 - 2655 MHz	2535 - 2655 MHz

7.2 TX Power and RX Sensitivity

Table 7-2 N723-EA RF transmit power

Band	Max power	Min. power
EGSM900	33 dBm±2 dB	5 dBm±5 dB
DCS1800	30 dBm±2 dB	5 dBm±5 dB
WCDMA B1	23 dBm+1/-3 dB	<-50 dBm
WCDMA B5	23 dBm+1/-3 dB	<-50 dBm
WCDMA B8	23 dBm+1/-3 dB	<-50 dBm
FDD LTE B1	23 dBm±2 dB	<-39 dBm
FDD LTE B3	23 dBm±2 dB	<-39 dBm
FDD LTE B5	23 dBm±2 dB	<-39 dBm
FDD LTE B7	23 dBm±2 dB	<-39 dBm
FDD LTE B8	23 dBm±2 dB	<-39 dBm
FDD LTE B20	23 dBm±2 dB	<-39 dBm
FDD LTE B28	23 dBm±2 dB	<-39 dBm
TDD LTE B38	23 dBm±2 dB	<-39 dBm
TDD LTE B40	23 dBm±2 dB	<-39 dBm
TDD-LTE B41	23 dBm±2 dB	<-39 dBm

Table 7-3 GSM RX sensitivity of N723-EA

Band	Receiving sensitivity
EGSM900	≤-108 dBm
DCS1800	≤-108 dBm

Table 7-4 N723-EA WCDMA RX sensitivity

Band	Receiving sensitivity
WCDMA B1	≤-108 dBm
WCDMA B5	≤-108 dBm
WCDMA B8	≤-108 dBm

Table 7-5 LTE RX sensitivity of N723-EA

Band	Receiving sensitivity	Duplex mode
LTE B1	≤-97 dBm	FDD
LTE B3	≤-97 dBm	FDD
LTE B5	≤-97 dBm	FDD
LTE B7	≤-96.5 dBm	FDD
LTE B8	≤-97.5 dBm	FDD
LTE B20	≤-97.5 dBm	FDD
LTE B28	≤-97.5 dBm	FDD
LTE B38	≤-97.5 dBm	TDD
LTE B40	≤-97.5 dBm	TDD
LTE B41	≤-97.5 dBm	TDD

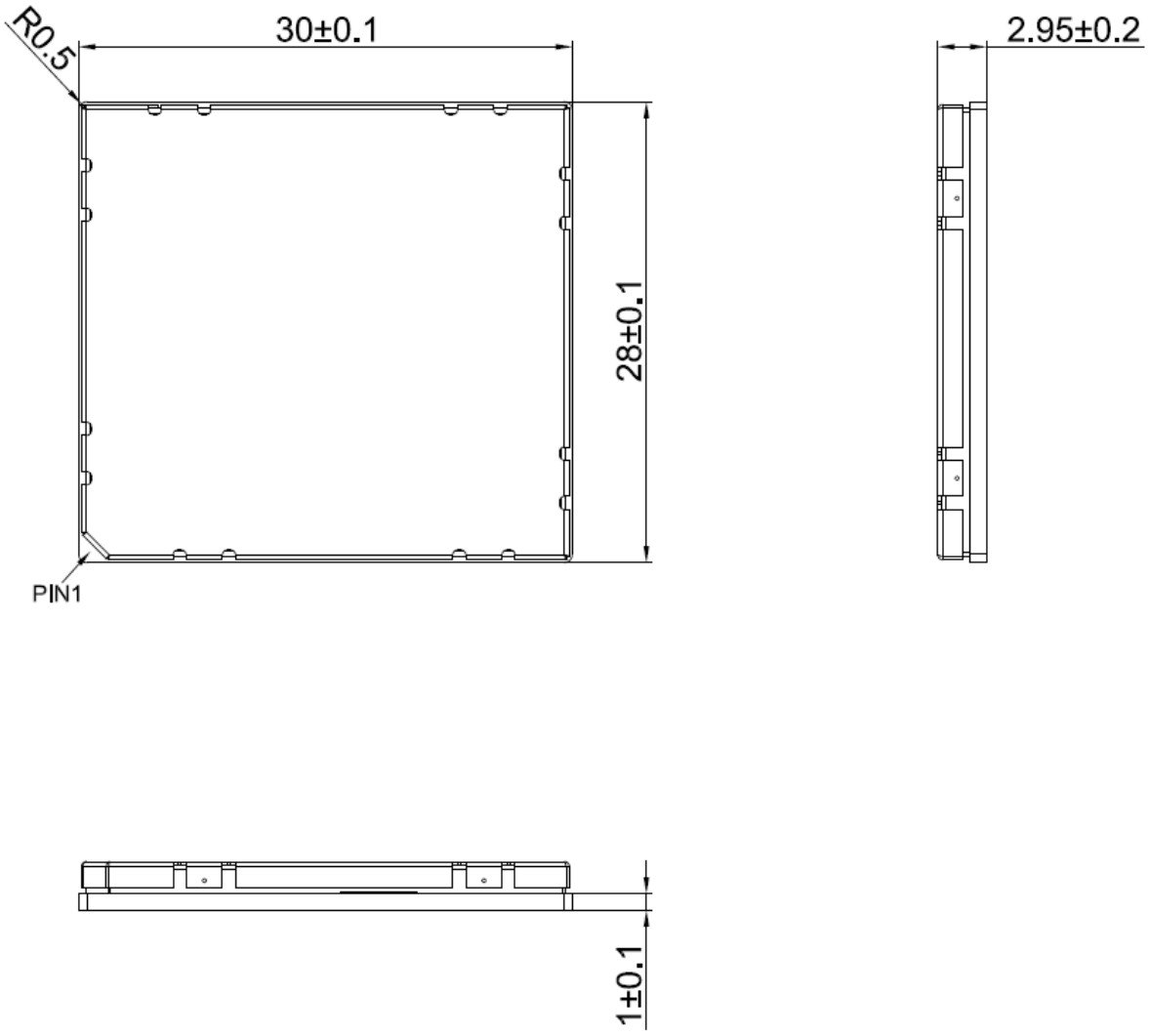
The preceding indexes are test data in a laboratory environment. The test results of LTE (Cat 4) in a bandwidth of 10 MHz will have a certain deviation due to the influence of the network environment.

8 Mechanical Characteristics

This chapter describes mechanical characteristics of the N723-EA module.

8.1 Dimensions

Figure 8-1 N723-EA dimensions (unit: mm)



8.2 Label

The label information is laser carved on the cover. The following figure shows the label of N723-EA.

Figure 8-2 N723-EA label

The picture above is only for reference.

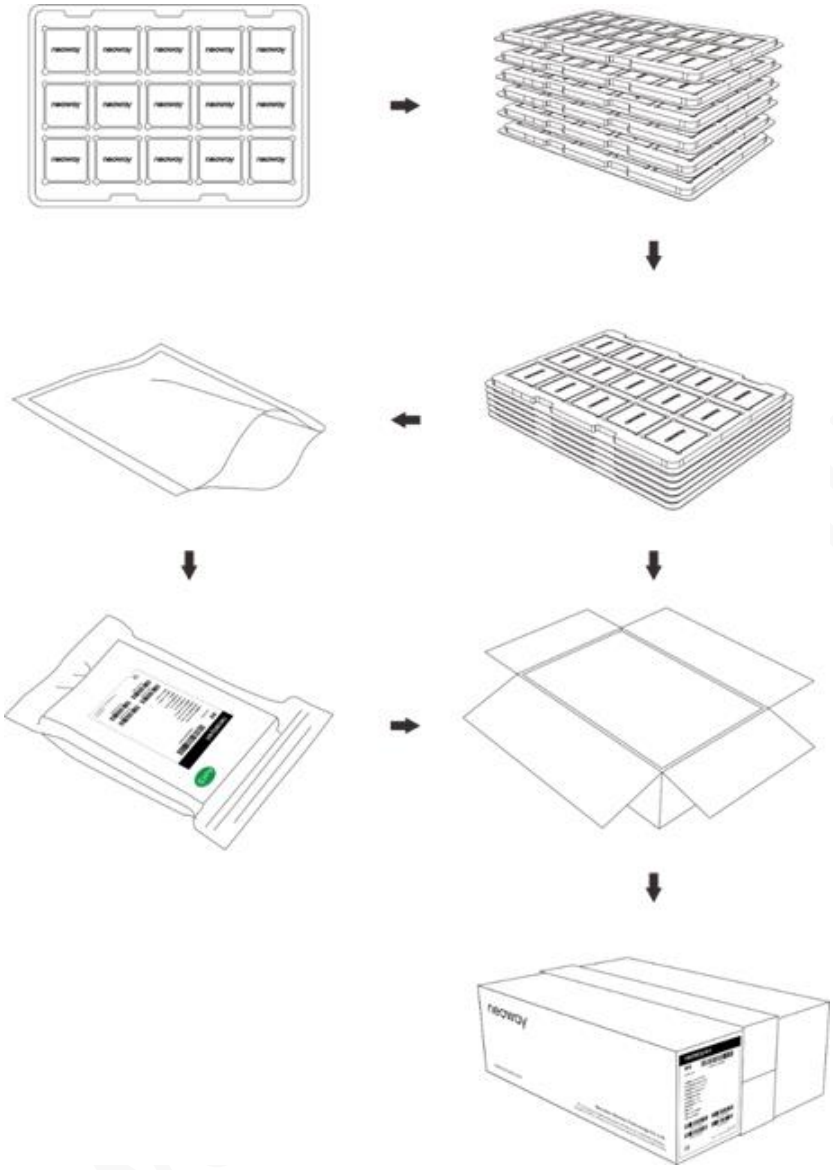
8.3 Packing

N723-EA adopts the SMT method for oven soldering. To prevent the product from being damp before it is delivered to customers, the tray is used for moisture-proof packaging. The aluminum foil bag, desiccant, humidity indicator card, tray, vacuum and other processing methods are used to ensure the dryness of the product and extend its service life.

8.3.1 Tray

The mass-produced is packaged and shipped using the following tray method:

Figure 8-3 Packing process



The picture above is only for reference.

8.3.2 Moisture

N723-EA is a level 3 moisture-sensitive electronic element, in compliance with IPC/JEDEC J-STD-020 standard.

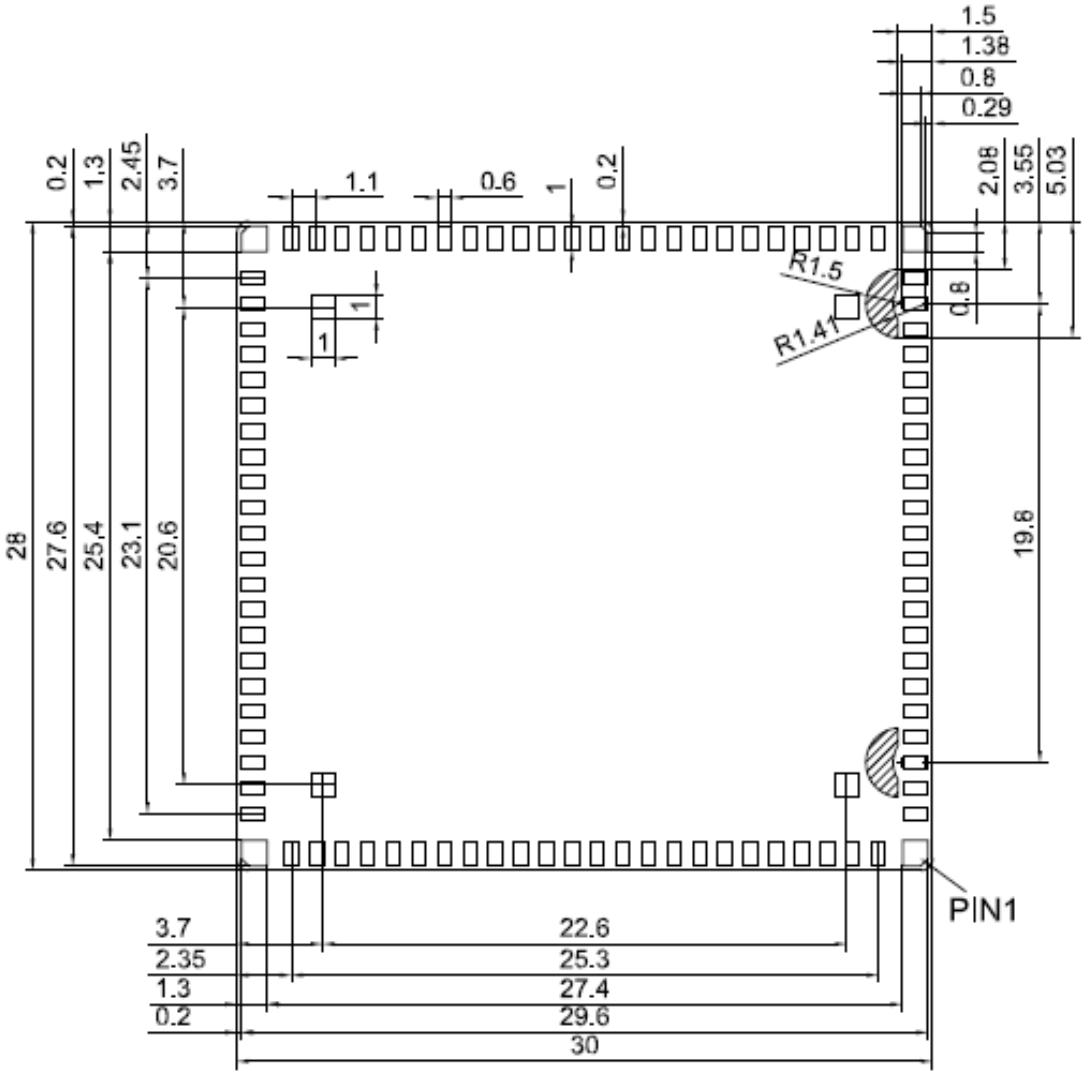
After the module is unpacked, if it is exposed to the air for a long time, the module will get damp, and may be damaged during reflow soldering or laboratory soldering. bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at a temperature higher than 90 degrees for more than 12 hours. In addition, since the package tray is made of non-high temperature resistant material, do not bake modules with the package tray directly.

9 Mounting

This chapter describes the module PCB package and application PCB package of N723-EA, as well as the key points of SMT related technology.

9.1 PCB Package

Figure 9-1 N723-EA bottom view of PCB package (unit: mm)

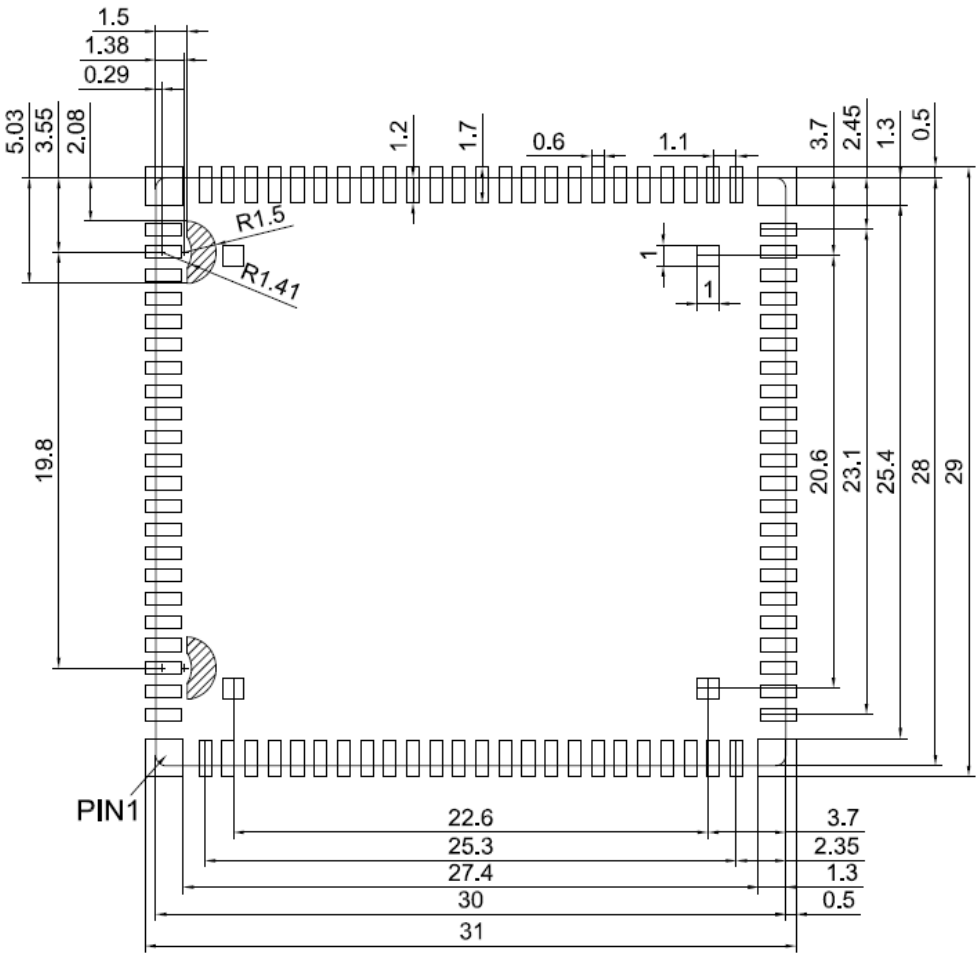


9.2 Application Foot Print

The N723-EA module has a total of 100 pins in LGA package, and the recommended application PCB package is as follows:

Only GND via-holes and pour coppers are allowed in the shaded area "▨" of the PCB package to ensure the proper operation of the module.

Figure 9-2 N723-EA recommended footprint of the pplication PCB (unit: mm)



9.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

9.4 Solder Paste

The thickness of the solder paste and the flatness of the PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

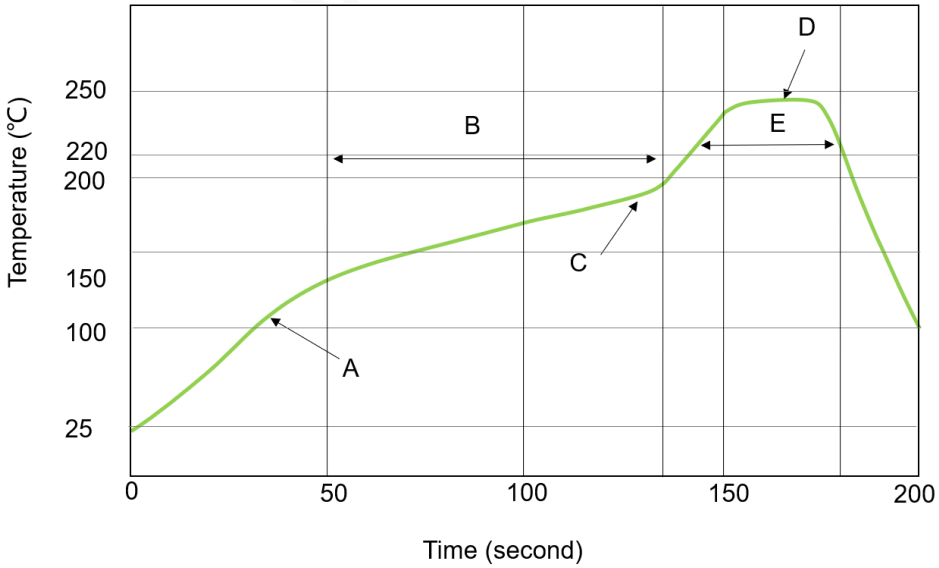
- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process parameters is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220 °C for more than 45 seconds and the peak temperature reaches 240 °C.

9.5 SMT Oven Temperature Profile

Neoway will not provide warranty for heat-responsive element abnormalities caused by improper temperature control.

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 9-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4 °C/sec
- Ramp down rate: -3 to -1 °C/sec
- Soaking zone: 150-180 °C, Time: 60-100 s
- Reflow zone: >220 °C, Time: 40-90 s
- Peak temperature: 235 - 245°C

For information about cautions in storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 245 °C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module at high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

A Abbreviation

Abbreviation	Full name
AI	Analog Input
AO	Analog Output
ARM	Advanced RISC Machine
Bps	Bits per Second
CCC	China Compulsory Certification
CS	Chip Select
CTS	Clear to Send
DC	Direct Current
DCS	Digital Cellular System
DI	Digital Input
DL	Downlink
DO	Digital Output
DRX	Discontinuous Reception
EGSM	Enhanced GSM
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance
EVK	Evaluation Kit
FDD	Frequency Division Duplexing
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
3GPP	3rd Generation Partnership Project
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
IO	Input/Output
LCC	Leadless Chip Carriers
LED	Light Emitting Diode

LGA	Land Grid Array
LTE	Long Term Evolution
MCLK	Main Clock
MCU	Microcontroller Unit
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage
WiFi	Wireless Fidelity
WCDMA	Wide-band Code Division Multiple Access
WLAN	Wireless Local Area Network

