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N717-EA

Hardware User Guide

LTE Cat.1
Issue 1.0
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Notice

This document provides guide for users to use N717-EA.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to N717-EA.

It defines the features, indicators, and test standards of the N717-EA module and provides reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2022-12	Initial draft	Wu Yongqiang

Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

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Related Documents

Neoway_N717-EA_Datasheet

Neoway_N717-EA_Product_Specifications

Neoway_N717_AT_Command_Mannual

Neoway_N717-EA_EVK_User_Guide

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1 About N717-EA

This chapter introduces the product overview, block diagram, and basic features of N717-EA.

1.1 Product Overview

N717-EA is an LTE industrial-grade cellular modules with dimensions of (29.0 ± 0.10) mm × (25.0 ± 0.10) mm × (2.35 ± 0.15) mm. It provides with dimensions of on GSM, FDD-LTE (Cat 1) and TDD-LTE (Cat 1) networks, especially on B31 (450 MHz). It provides various hardware interfaces and is suitable for developing IoT communications devices such as wireless meter reading terminal and industrial router that are widely used in power and industrial markets.

N717-EA has the following features:

- ARM Cortex-R5 processor, 614 MHz CPU clock speed, 32 KB L1 cache
- Available networks: GSM/GPRS & LTE Cat 1
- Supported interfaces: USB2.0/USIM/UART/PCM/I2C/MIC/SPK

Table 1-1 lists variants and frequency bands that N717-EA supports.

Table 1-1 Models and frequency bands

Model	Region	Category	Frequency band
EA	Europe	Cat1	FDD-LTE: B1, B3, B5, B7, B8, B20, B28, B31 TDD-LTE: B38, B40, B41 GSM: 900/1800 MHz

1.2 Block Diagram

N717-EA includes the following functional units:

- Baseband chip
- 26 MHz crystal
- Power management
- RF functional

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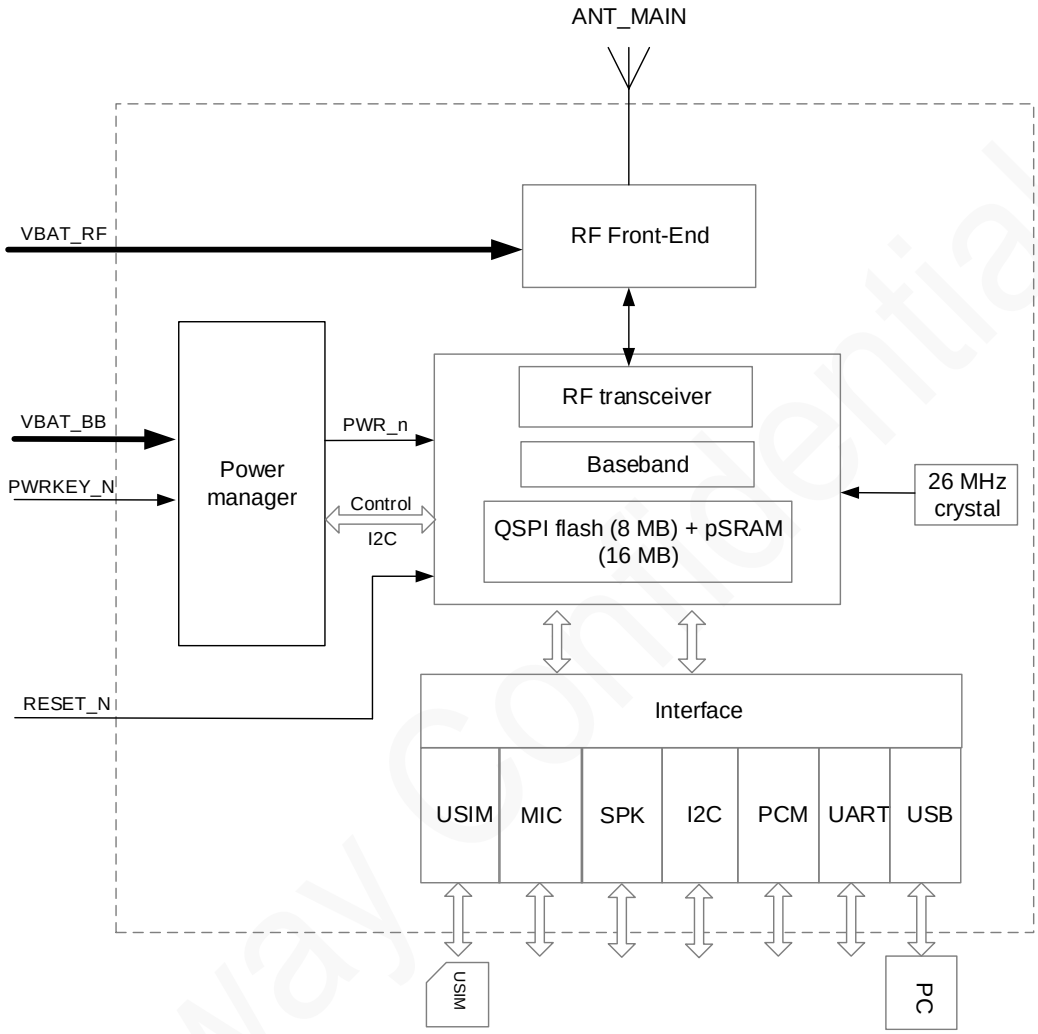
- Digital interfaces (USIM, I2C, UART, USB, and PCM)
- Analog interfaces (MIC, SPK)

Figure 1-1 Block diagram



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1.3 Basic Features

Features	Description
Physical features	• Dimensions: (29.0 ± 0.10) mm × (25.0 ± 0.10) mm × (2.35 ± 0.15) mm • Package: LGA (126 pads) • Weight: about TBD
Temperature ranges	• Operating: -30°C to +75°C • Extended: -40°C to +85°C • Operating: -40°C to +90°C

Operating voltage (DC)	VBAT: 3.4 V to 4.2 V, typical value: 3.6 V
Operating current (DC)	Sleep mode[1]: TBD
	[2]: TBD
	Operating mode[3] (LTE system): TBD
Embedded processor	ARM Cortex-R5 processor, 614 MHz CPU clock speed, 32 KB L1 cache
Memory	RAM: 16 MB ROM: 8 MB
Frequency band	See Table 1-1.
Wireless rate	GPRS: Max 85.6 Kbps (DL)/Max 85.6 Kbps (UL) EDGE: Max 236.8 Kbps(DL)/Max 236.8 Kbps(UL) FDD-LTE: Cat1, Max 10 Mbps (DL)/Max 5 Mbps (UL) TDD-LTE: Cat1, Max 8 Mbps (DL)/Max 2 Mbps (UL)
Transmit power	EGSM900: 33 dBm ±2 dB (Power Class 4) DCS1800: 30 dBm ±2 dB (Power Class 1) EGSM900 8-PSK: 27 dBm ±3 dB (Power Class E2) DCS1800 8-PSK: 26 dBm ±3 dB (Power Class E2) LTE: 23 dBm ±2 dB (Power Class 3)
Application Interfaces	2G/4G antenna, with a characteristic impedance of 50 Ω.
	Two UART interfaces, one of which for debug. Default baud rate: 115200 bps
	Two USIM interfaces, either 1.8 V or 3.0 V USIM card is supported. (Currently USIM2 is not supported.)
	One USB 2.0 interface, for slave mode only.
	One PCM interface
	One I2C interface, for master mode only.
	One MIC interface
	One SPK interface, supports driving power of up to 37 mW with a 32 Ω load. If higher driving power is required, connect this interface to an external power amplifier.

[1] means the current drawn by the module in sleep mode, a low power consumption state, in which its RF function is functioning properly but its peripheral interfaces are disabled. If there is an incoming call or SMS, the module will exit from the sleep mode, and after the incoming call or voice instant messaging has ended, the module will re-enter the sleep mode.

[2] means the current drawn by the module in a normal operating mode, but no data service is being processed.

[3] means the current drawn by the module when there are on-going data services. In the operating mode, only the current value on LTE network is exemplified. For other current values on other network modes, please refer to the current test report.

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SD card AT bus command	3GPP Release 9 Neoway extended AT commands
SMS	PDU, TXT
Data	PPP
Protocol	TCP, UDP, FTP/FTPS
Certification approval	RoHS*, CE*

* means under development.

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2 Reference Standard

N717-EA is designed by referring to the following standards:

- 3GPP TS 36.521-1 V9.10.0 User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Radio Resource Management (RRM) conformance testing
- 3GPP TS 21.111 V9.0.0 USIM and IC card requirements
- 3GPP TS 31.102 V9.10.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V9.11.0 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V9.4.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V9.0.0 Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE-DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

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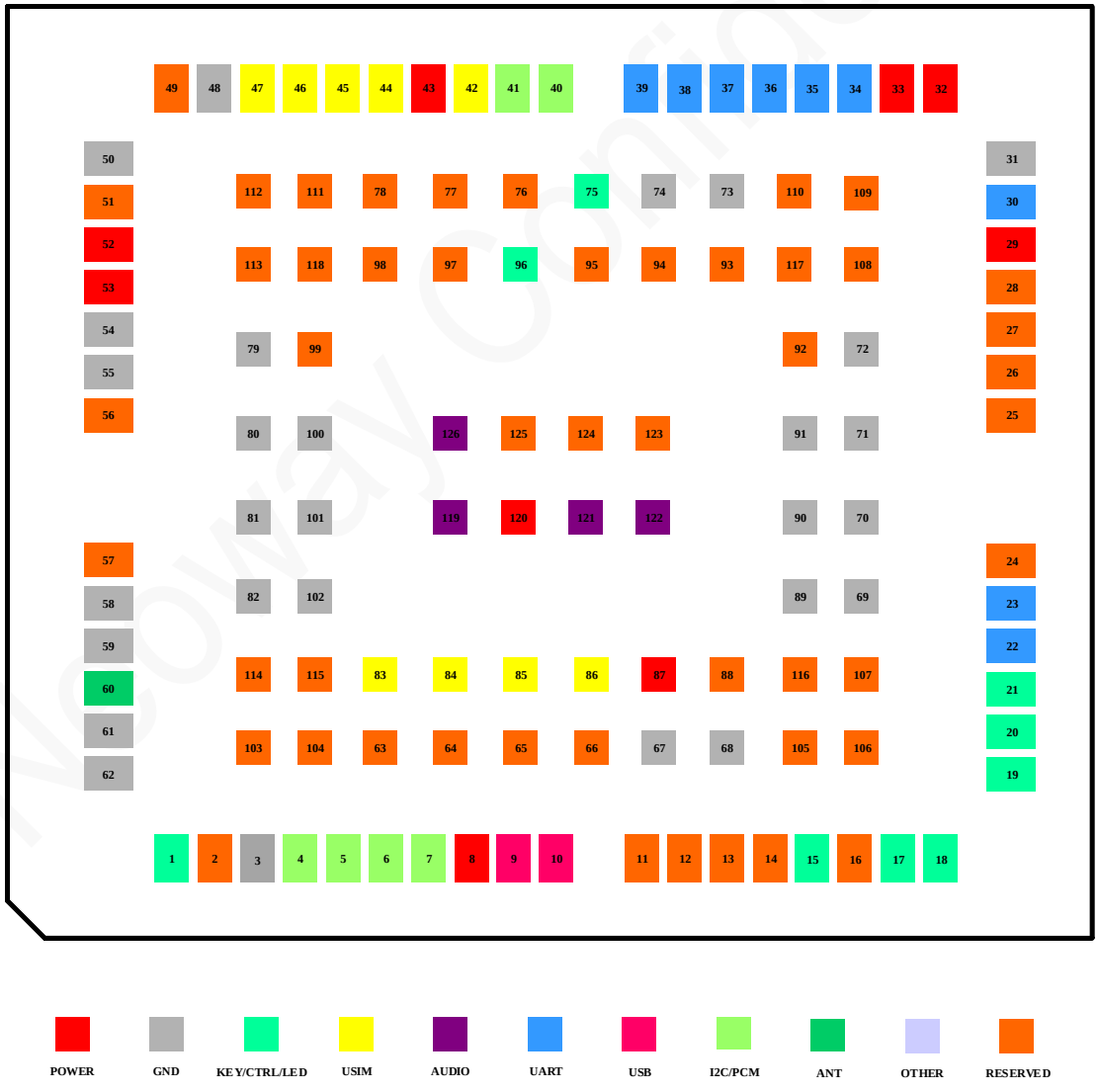
3 Pin Definitions

N717-EA is equipped with 126 pads, which are introduced in LGA package. Available functional interfaces include: power supply, USB, UART, USIM, PCM, I2C, etc.

3.1 Pad Layout

The following figure shows the pad layout of N717-EA.

Figure 3-1 N717-EA pad layout (top view)



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3.2 Pin Description

The following table lists the IO types and DC characteristics.

Table 3-1 IO types and DC characteristics

IO type			
B	Digital input and output, CMOS logic level		
DO	Digital output, CMOS logic level		
DI	Digital input, CMOS logic level		
PO	Power output		
PI	Power input		
AO	Analog output		
AI	Analog input		
AIO	Analog input and output		
DC characteristics			
Interface type	Power domain	Logic level characteristics	
USIM	P1: Either 1.8 V or 3.0 V USIM card is supported	1.8 V DC characteristics V_{IH}=0.65V_{DD_P1}~1.98V V_{IL}=-0.3V~0.35V_{DD_P1} V_{OH}=1.35V~V_{DD_P1} V_{OL}=0V~0.45V	3.0 V DC characteristics V_{IH}=2V~V_{DD_P1}+0.3V V_{IL}=-0.3V~0.8V V_{OH}=2.4V ~V_{DD_P1} V_{OL}=0V~0.4V
RESET_N	P2: 1.6V	V_{ILmax}=0.5V	

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GPIO	P3: 1.8V	V_{IH}=0.65V_{DD_P3}~1.98V V_{IL}=-0.3V~0.35V_{DD_P3} V_{OH}=1.35V~V_{DD_P3} V_{OL}=0V~0.45V

Table 3-2 Pin definitions

Signal	Pin SN	I/O type	Function description	DC characteristics/ power domain	Remarks
Power interfaces					
VBAT_BB	32, 33	PI	Module baseband supply input	V_{min}=3.4V, V_{norm}=3.6V, V_{max}=4.2V	The external power supply must ensure at least 0.8 A current for VBAT_BB.
VBAT_RF	52, 53	PI	RF supply input		The external power supply must ensure at least 2.2 A current for VBAT_RF.
VDD_1P8	29	PO	1.8 V power output	V_{norm} = 1.8 V, I_{max} = 50 mA	Only used for voltage-level translation. Leave this pin open if unused.
GND	3, 31, 47 - 48, 50, 54 - 55, 58 - 59, 61- 62, 67- 74, 79 - 82, 89 - 91, 100 - 102				Make sure all GND pins are grounded.
Control interfaces					
PWRKEY_N	15	DI	Module on/off control	VBAT_BB power domain	A low-voltage level for a valid time period can trigger on/off of the module (see section 4.2).
RESET_N	17	DI	Module reset input	P2	Active low
WAKEUP_IN*	96	DI	Wake up the module.	P3	For details, see section 4.6.1 .

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Network status indication interface					
STATUS	20	DO	Working status indication	P3	-
NET_LIGHT	21	DO	Network status indicator	P3	-
SLEEP_IND	1	DO	Sleep mode indicator	P3	-
UART1 interface					
UART_DTR	30	DI	Data terminal ready	P3	Software version (Standard): For communication based on AT commands. Software version (Open): For data transmission.
UART_RXD	34	DI	UART data input	P3	
UART_TXD	35	DO	UART data output	P3	
UART_RTS	36	DO	UART ready to send	P3	
UART_CTS	37	DI	UART clear to send	P3	
UART_DCD	38	DO	Data carrier detect	P3	
UART_RI	39	DO	Ring indication	P3	
DEBUG UART interface					
DEBUG_UART_RXD	22	DI	Debug UART data input	P3	For module debugging only.
DEBUG_UART_TXD	23	DO	DEBUG UART data out	P3	
USIM interfaces					
USIM1_DET	42	DI	USIM1 hot-swapping detection	P3	-
USIM1_VCC	43	PO	USIM1 power output	Either 1.8 V or 3.0 V USIM card is supported	-
USIM1_RESET	44	DO	USIM1 reset	P1	-
USIM1_DATA	45	B	USIM1 data input and output	P1	Pulling up this pin to USIM1_VCC via a 4.7 kΩ resistor is required.

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USIM1_CLK	46	DO	USIM1 clock output	P1	-
USIM2_DET*	83	DI	USIM2 hot-swapping detection	P3	Currently not supported.
USIM2_CLK*	84	DO	USIM2 clock output	P1	
USIM2_RESET*	85	DO	USIM2 reset	P1	
USIM2_DATA*	86	B	USIM2 data input and output	P1	
USIM2_VCC*	87	PO	USIM2 power output	Either 1.8 V or 3.0 V USIM card is supported	
USB interfaces					
USB_VBUS	8	AI	Voltage detection	3.5 V - 5.25 V, typical value: 5.0V	-
USB_DP	9	AIO	USB data +	-	USB 2.0. This pin is used for software download and data transmission. Route the DM and DP traces as differential pairs, and the impedance of the differential pairs is 90 Ω.
USB_DM	10	AIO	USB data -	-	
I2C interface					
I2C_SCL	40	DO	I2C clock	P3	Connecting this pin through a pull-up resistor (4.7 kΩ recommended) to VDD_1P8 is required.
I2C_SDA	41	B	I2C data	P3	
PCM interface					
PCM_CLK	4	DO	PCM data clock	P3	Leave this pin open if unused.
PCM_SYNC	5	DO	PCM data frame synchronization	P3	Leave this pin open if unused.
PCM_DIN	6	DI	PCM data input	P3	Leave this pin open if unused.

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PCM_DOUT	7	DO	PCM data output	P3	Leave this pin open if unused.
Analog audio interface					
SPK_P	121	AO	Analog audio output +	-	Supports driving power of up to 37 mW with a 32 Ω load. If higher driving power is required, connect this interface to an external power amplifier.
SPK_N	122	AO	Analog audio output -	-	
MIC_BIAS	120	PO	Microphone bias voltage output	-	-
MIC_N	119	AI	MIC analog input -	-	-
MIC_P	126	AI	MIC analog input +	-	-
Antenna interface					
ANT_MAIN	60	AIO	Main antenna	/	Control the impedance of antenna traces at 50 Ω.
Other functional interfaces					
USB_BOOT	75	DI	Emergency download control	P3	Active high. Pulling this pin high to VDD_1P8 can set the module into USB emergency download mode.
RF_DISABLE*	18	DI	Flight mode control	P3	-
AP_READY*	19	DI	Application processor ready	P3	-
RESERVED	2, 11 - 14, 16, 24 - 28, 49, 51, 56 - 57, 63 -66, 76 - 78, 88, 92 -95, 97 - 99, 103 - 118, 123 - 125		Reserved pin	-	It is reserved for future function expansion or functions not open to the user. There may be more than one pin named RESERVED, which may have different functions or definitions. Leave these RESERVED pins open.

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4 Application Interfaces

N717-EA provides interfaces for control, communications, peripherals RF and other functions to meet the requirements of different product application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

4.1 Power Interfaces

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of the actual applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin SN	I/O	Function description	Remarks
VBAT_BB	32, 33	PI	Module baseband supply input	The external power supply must ensure at least 0.8 A current for VBAT_BB.
VBAT_RF	52, 53	PI	RF supply input	The external power supply must ensure at least 2.2 A current for VBAT_RF.
VDD_1P8	29	PO	1.8 V power output	With output currents of up to 50 mA, used only for voltage-level translation. It is recommended to add ESD protection when used.
GND	3, 31, 47 - 48, 50, 54 - 55, 58 - 59, 61-62, 67- 74, 79- 82, 89 - 91, 100 - 102			Make sure all GND pins are grounded.

4.1.1 VBAT

The design of power supply includes two parts: schematic design and PCB layout.

Power Supply Design

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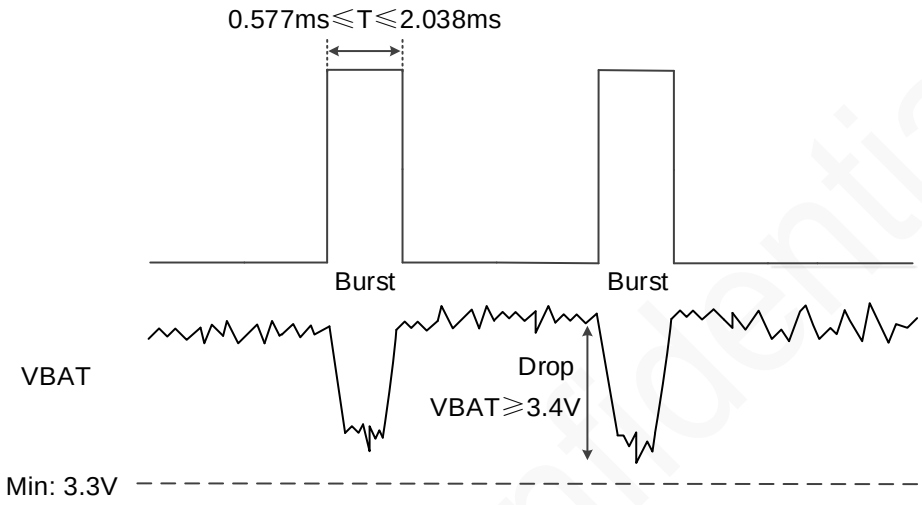
In GSM/GPRS mode, RF data transmission is intermittent, the frequency of burst transmission is about 217 Hz and the peak current is up to 3 A. Therefore, it is necessary to ensure the following conditions: The driving capacity of the power supply is sufficient, the power supply trace is wide enough to reduce the impedance, and a large capacitance is provided to improve the freewheeling current, thereby ensuring that the voltage will not drop below the minimum operating voltage of the module at the instantaneous peak current.

Figure 4-1 Voltage drops of the power supply.



Never use a diode to make the voltage drop between a higher input and the module power supply. The forward voltage drop V_f of diode has two characteristics: one is that it increases with the increase of the forward current. the other is that it increases significantly at a low temperature. Note that, if there is an instantaneous high current, the above characteristics will lead to unstable operating voltage of the module, and even damage the module.

The power supply design of the N717-EA module depends on the input voltage of power supply. There are three power input types:

- 3.4 V - 4.2 V power input (typical value: 3.6 V, provided by a battery)
- 4.2 V - 5.5 V power input (typical value: 5.0 V, provided by a computer internal rectifier)
- 5.5 V - 24 V power input (typical value: 12 V, provided by a DC-DC power supply solution)

The design recommendations for 3.4 V - 4.2 V power input are as follows:

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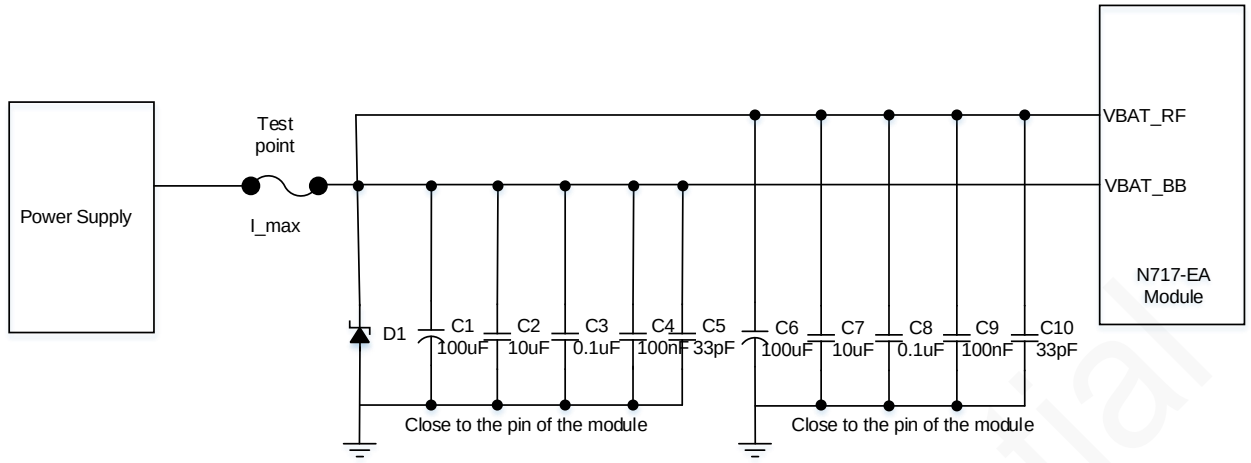
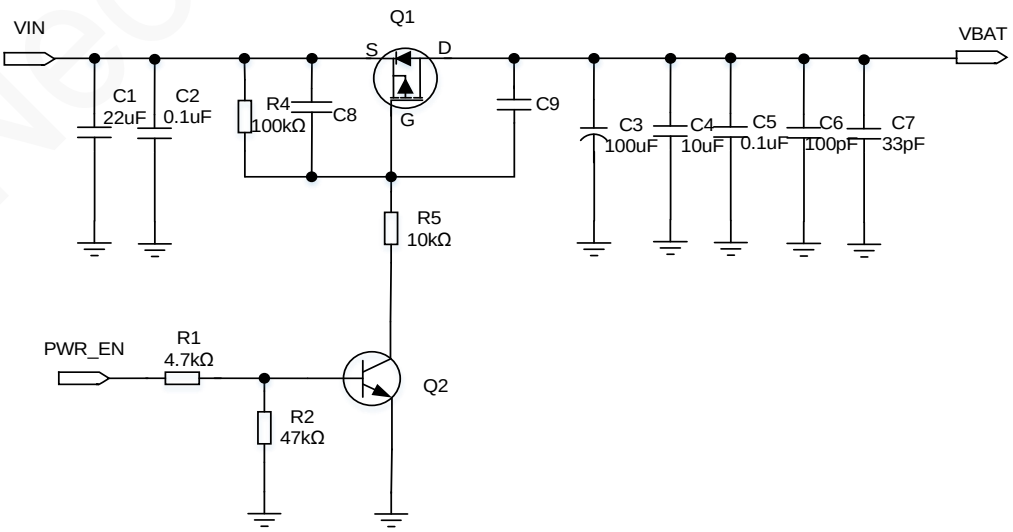
Figure 4-2 Recommended power supply design 1



- The maximum input voltage of the module power supply is 4.2 V, and the typical value is 3.6 V.
- In order to get a stable power source, it is recommended to use a TVS diode with suggested low reverse voltage (VRWM 4.5 V) and peak power (Ppp = 2800 W (tp = 8/20 us)) at D1. Keep the placement of the TVS diode close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and the module.
- To decrease voltage drops during bursts, a large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 and C6. Their maximum safe operating voltage should be larger than 2 times the voltage of the power supply.
- Keep the low ESR bypass capacitors (C2, C3, C4, C5) as close to the module as possible to filter out high-frequency interference in the power supply.

If it is necessary to control the power supply, the following circuit design is recommended:

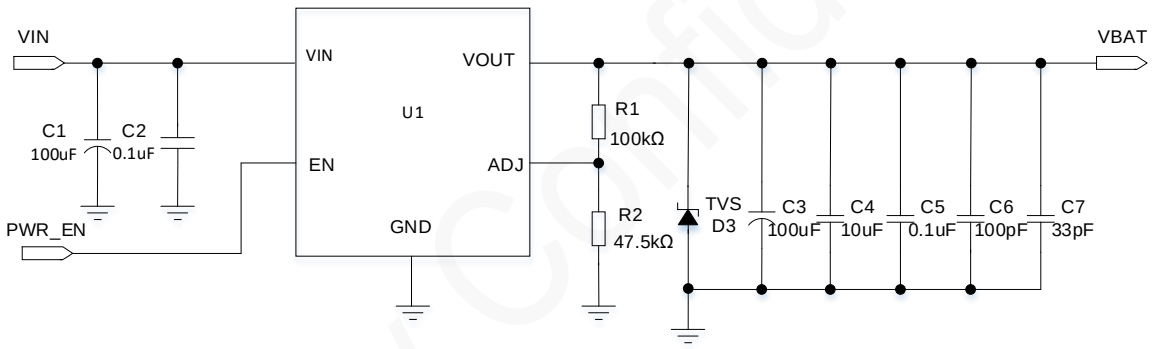
Figure 4-3 Recommended power supply design 2



- Select an enhanced P-MOSFET at Q1, of which the withstand voltage is high (V_{dss} = -12 V), drain current is high ($I_{D(MAX)}$ = -3.5 A) and RDS is low ($R_{ds(on)}$ = 108 mΩ).
- Select a common NPN transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which the break-over voltage on the base of the transistor increases at a low temperature; it is recommended that the value of R2 be at least 10 times that of R1.
- Keep the placement of C3 close to the module. Select a large-capacity tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) at C3 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be larger than 2 times the power supply voltage.
- Keep the low ESR bypass capacitors (C4, C5, C6, C7) as close to the module as possible to filter out high-frequency interference in the power supply.

The design recommendations for the 4.2 V - 5.5 V power input are as follows:

Figure 4-4 Recommended power supply design3



- If the power input voltage at VIN is similar to the VBAT voltage, it is recommended to use an LDO while supplying power for the module, which is simple with high efficiency.
- Select an LDO with a maximum output current of no greater than 3 A at U1 to ensure the normal performance of the module.
- Keep the placement of the TVS diode close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and modules.
- Keep the placement of C3 close to the module. Select a large-capacity tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) at C3 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be larger than 2 times the power supply voltage.
- Keep the low ESR bypass capacitors (C4, C5, C6, C7) as close to the module as possible to filter out high-frequency interference in the power supply.

The design recommendations for the 5.5 V - 24 V power input are as follows:

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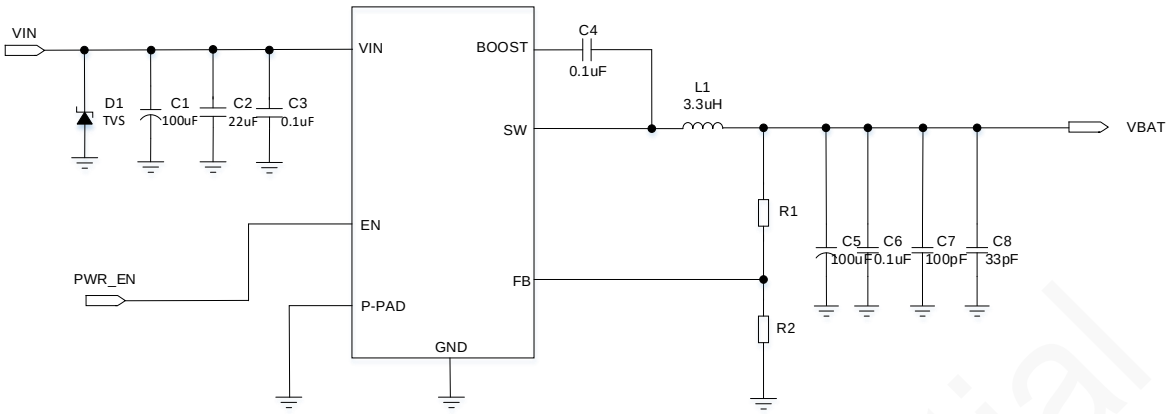
Figure 4-5 Recommended power supply design4



- If there is a high voltage drop between the power input and VBAT, a DC-DC design should be selected for higher efficiency, and the output current should be at least 3 A.
- Keep the TVS diode (D1) close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and modules.
- Keep the placement of C5 close to the module. Select a large-capacity aluminum electrolytic capacitor (220 μF or 100 μF) or tantalum electrolytic capacitor (470 μF or 1000 μF) at C5 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be more than 2 times the power supply voltage.
- Keep the low ESR bypass capacitors (C6, C7, C8) as close to the module as possible to filter out high-frequency interference in the power supply.

When the module encounters a running exception and cannot be switched off in a normal method, it is recommended to disconnect the power of the module and then power and turn it on to restore the module.

PCB Layout

Place an ESR capacitor at the output of the power source to suppress peak current. In order to protect the back-end components, it is necessary to add a TVS diodes at the input of the power supply to suppress voltage spikes. The circuit design is important, and the component placement and PCB routing are equally important. Several key points in power supply design are as follows:

- The TVS diode can absorb instantaneous high-power pulse and can withstand instantaneous pulse current peaks up to tens or even hundreds of amperes, with extremely short response time of voltage clamping. Keep the TVS diode as close to the power input as possible, ensuring that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB traces.

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- Place the bypass capacitor as close as possible to the power supply pin of the module to filter out high-frequency noise signals in the power supply.
- For the main power circuit of the module, ensure that the PCB trace is wide enough that 3 A current can be safely passed, with no significant loop voltage drop. Keep the VBAT_BB trace width be at least 0.8 mm and the VBAT_RF trace width be at least 2.2 mm and ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make power traces short and wide.
- Keep noise-sensitive circuits, such as audio circuits and RF circuits far away from the power circuitry, especially when the DC-DC power supply is used.
- The voltage frequency of the SW pin of the DC-DC power supply is high, so the loop area should be minimized. Keep sensitive components far away from the SW pin of the DC-DC component to prevent noise coupling. Place feedback components as close as possible to the FB pin.
- The thermal-dissipation pads and GND pins of the DC-DC chip should be grounded to ensure good thermal dissipation and noise signal isolation.

4.1.2 VDD_1P8

VDD_1P8 power is normally on and cannot be turned off even in sleep mode. If an external circuit is connected, the sleep power consumption will increase. It is recommended that VDD_1P8 is used only for voltage-level translation, not for other purpose, and ESD protection is required when using VDD_1P8.

N717-EA provides one VDD_1P8 interface with a 1.8 V voltage and output currents up to mA.

4.2 Control Interfaces

Signal	Pin SN	I/O	Function description	Remarks
PWRKEY_N	15	DI	Module on/off control	Active low
RESET_N	17	DI	Module reset input	Active low

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4.2.1 Module Power-on

Table 4-1 Power-on description

Power-on trigger method	Supported or not	Power-off method	Notice
Key	Supported	Press the power-on key for no less than 2s and then release it.	When the module is in power-on mode, do not disconnect the power supply directly; otherwise, the flash inside the module will be damaged.
Pulse	Supported	Inputting a low level at PWRKEY_N for no less than 2s.	
Auto power-on (PWRKEY_N be grounded)	Supported	Send the power-off AT command to the module and then disconnect its power source.	When you need to design an auto power-on circuit for the module by referring to Figure 4-9, and repeated power-on/off operations are required, you should to add a module reset solution using the RESET_N pin by referring toFigure 4-12, since powering off the module while it is using the auto power-on solution may result in a startup failure.

Power-on via PWRKEY_N

The following describes two reference design circuits for module power-on.

- Figure 4-6 shows the reference design of key-control startup.

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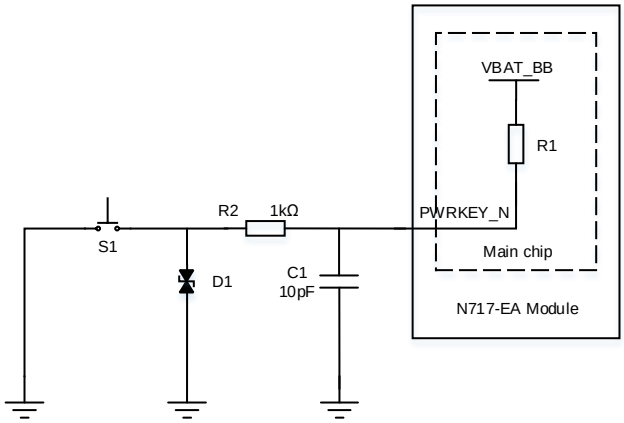
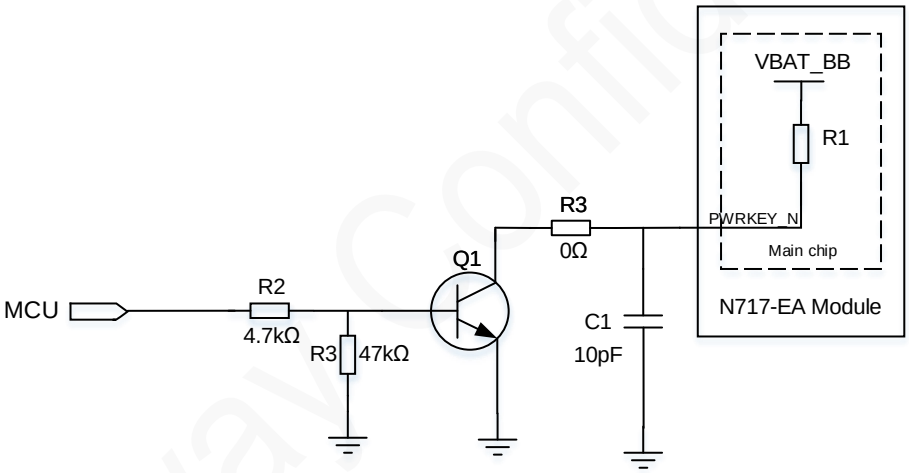
Figure 4-6 Reference design of key-control startup



- Figure 4-7 shows the reference design of MCU-control startup.

Figure 4-7 Reference design of MCU-control startup



- Power-on process

  After the VBAT input is powered, to switch the module on, the PWRKEY_N interface must be asserted low for 3s and then released. The AT function is available 5 seconds after the assertion of PWRKEY_N.

After turning on the module, it is not yet activated because the SW initialization process of the module is still in process internally. It takes some time to fully complete the HW and SW initialization of the module. During the Initialization state, AT commands are not available. Please access the module after the Initialization state completes. The module startup process is shown in the following figure.

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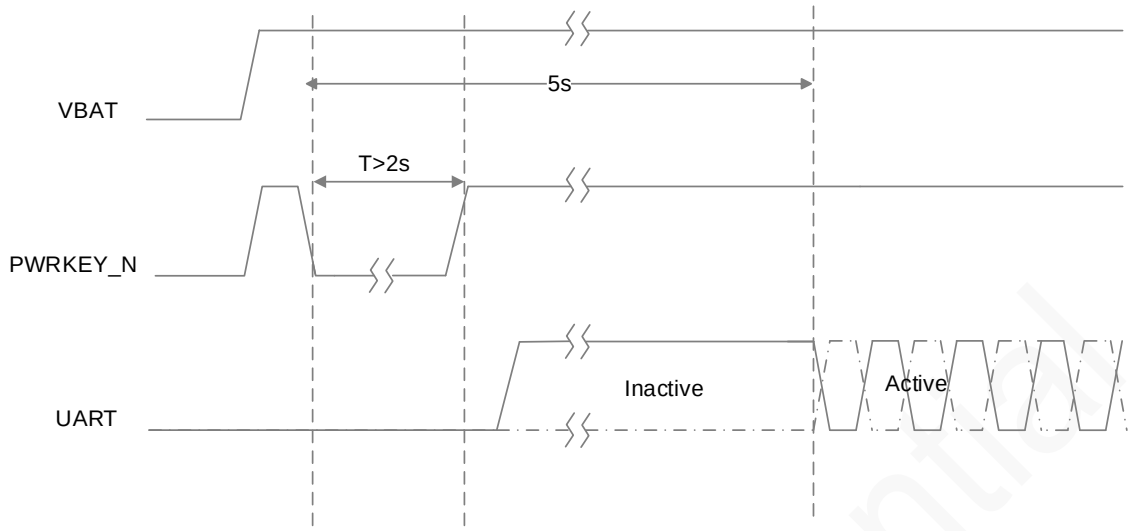
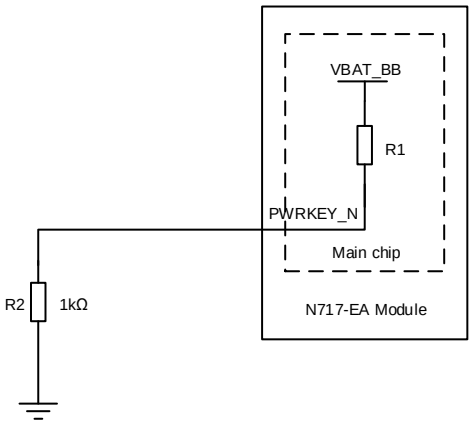
Figure 4-8 Power-on process



Auto Power-on

- When you need to design an auto power-on circuit for the module and do not require a power-off function, you should connect the PWRKEY_N pin through a pull-down resistor (1kΩ recommended) to ground.
- Note that adding a reset solution during designing the auto power-on circuit is a must when the module requires to be repeatedly turned on and off. To ensure a proper power-on/off operation, reset the module at least one time after power-on. For the reset circuit, see Figure 4-12.

Figure 4-9 Reference design of automatic startup once powered up



4.2.2 Module Power-off

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- When the module is in power-on mode, do not disconnect the power supply directly; otherwise, the flash inside the module will be damaged. Do not directly disconnect the power of the module in power-on mode, if there is not any abnormality.
- When you are using the AT command to switch off the module, ensure that PWRKEY_N will at a high-level voltage all the time. Otherwise, the module will start up automatically after the AT command execution.

Two methods are available to switch off the module: hardware shutdown and software shutdown

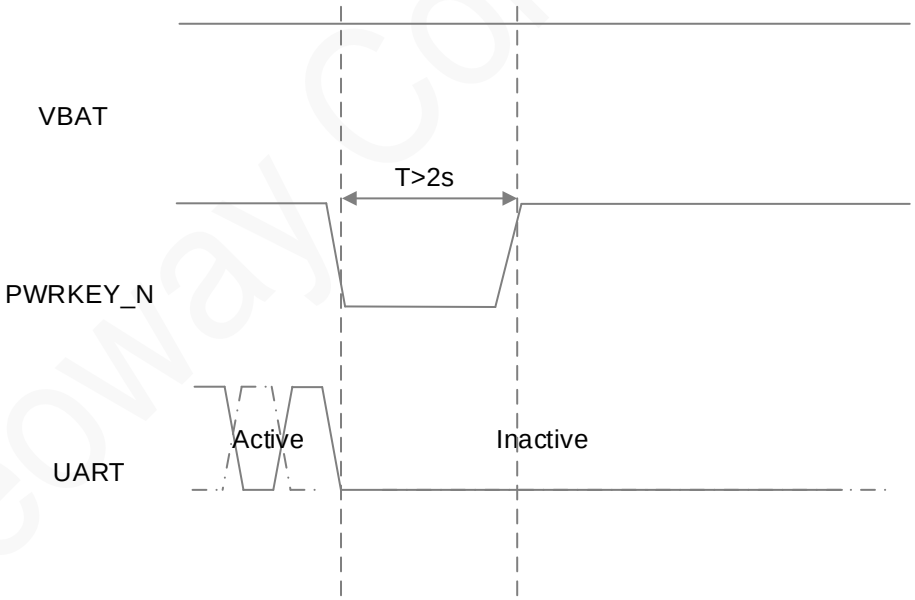
- Hardware power-off via PWRKEY_N
- Software power-off via AT command

Hardware Power-off via PWRKEY_N

When the module is in power-on mode, to turn off the module, the PWRKEY_N pin must be asserted low for greater than 2s and then released.

The following figure shows the hardware power-off process:

Figure 4-10 N717-EA hardware power-off process



Software Power-off via AT Command

When the module is in power-on mode, to turn off the module, send it the power-off AT command. For details of the AT command, see *Neoway_N717_AT_Commands_Manual*.

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4.2.3 Module Reset

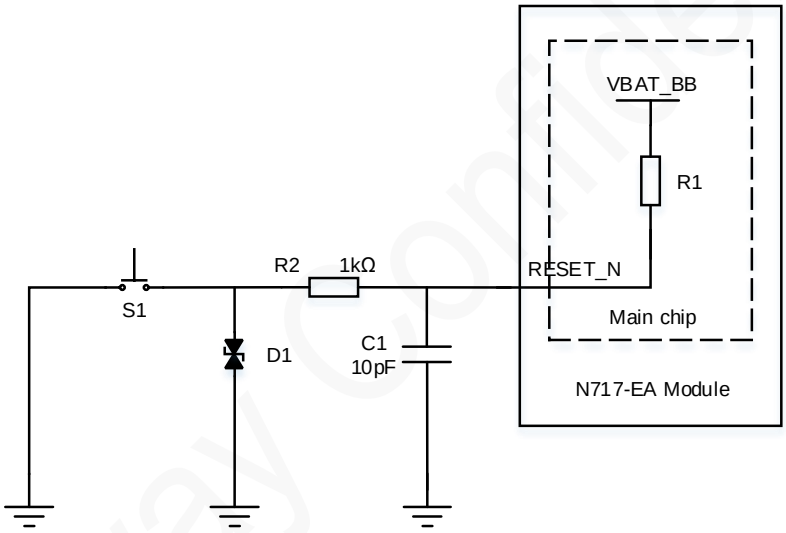
If the module encounters abnormalities such as system crash, you can reset the module system using the RESET_N pin to restore it. Therefore, it is strongly recommended to add a reset solution using the RESET_N pin when designing your PCB by referring to Figure 4-11 or Figure 4-12.

When the module is in power-on mode, inputting a low voltage at RESET_N for more than 50 ms can reset the module. For the module reset process, see Figure 4-13.

The following describes two reference design circuits for module reset.

- Key-control reset

Figure 4-11 Key-control reset



- MCU-control reset

  If you use a 1.8 V / 2.8 V / 3.3 V MCU system, it is recommended to add a triode to for isolation. Refer to the following figure for specific design.

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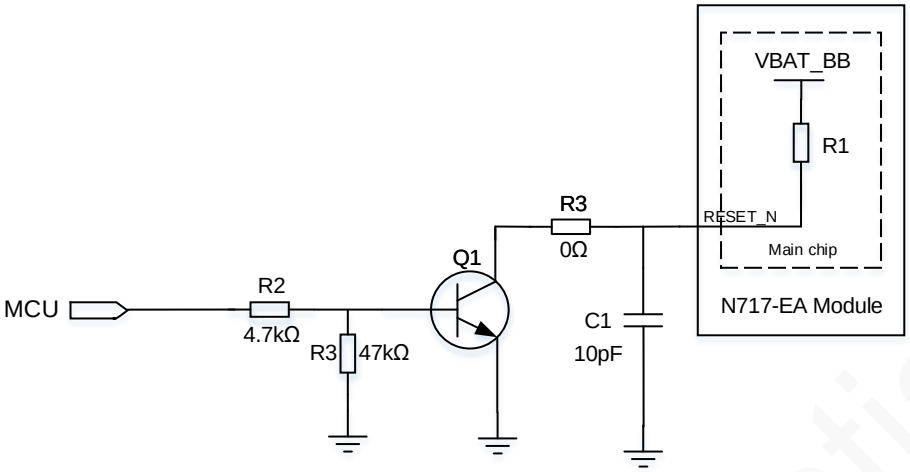
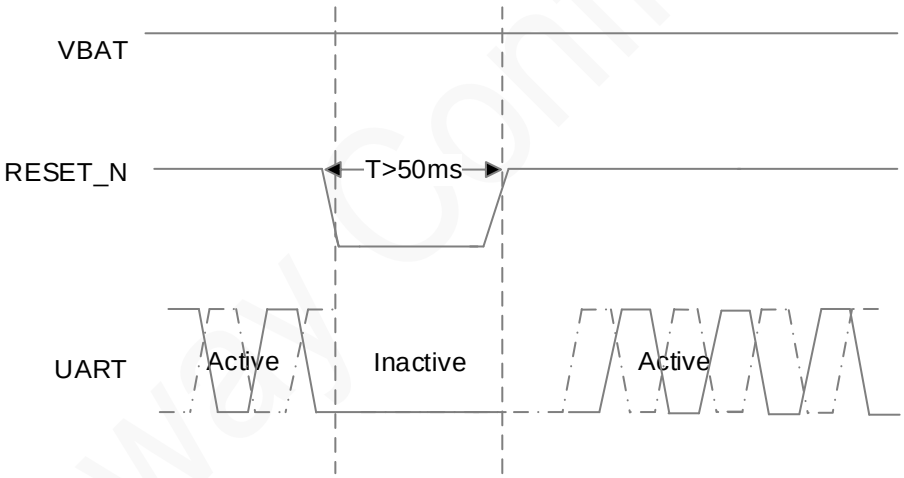
Figure 4-12 MCU-control reset



N717-EA module reset process is shown in the following figure.

Figure 4-13 Module reset process



4.3 Peripheral Interfaces

N717-EA provides a variety of peripheral interfaces.

In all reference designs in this section, the I/O direction indicated by the module peripheral interface pin name is based on the module, while the peripheral pin naming is based on the peripheral component itself. For example, UART_TXD of the module indicates the pin of the module for sending data, and MCU_RXD indicates the pin for MCU receiving data, so two pins should be connected.

In the process of peripheral model selection and design, please check the pin naming is based on the

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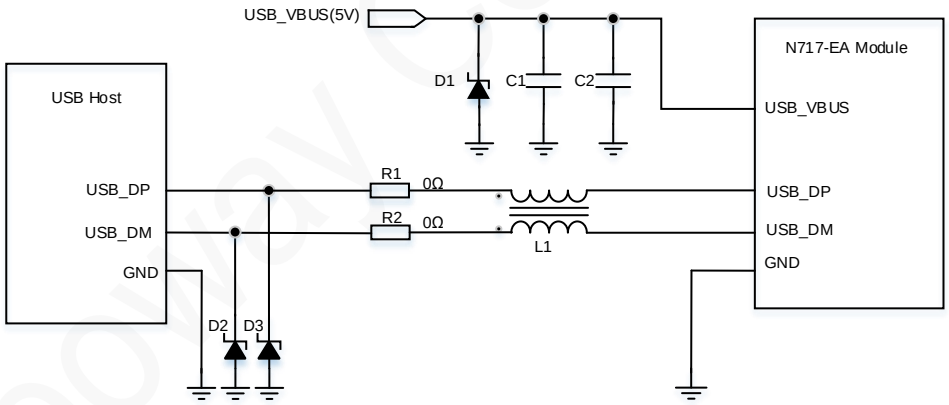
module or peripheral.

4.3.1 USB

Signal	Pin SN	I/O	Function description	Remarks
USB_VBUS	8	AI	Voltage detection	3.5 V < USB_VBUS < 5.25 V, typical value: 5 V.
USB_DP	9	AIO	USB data +	USB 2.0. This pin is used for software download and data transmission. Route the DM and DP traces as differential pairs, and the impedance of the differential pairs is 90 Ω.
USB_DM	10	AIO	USB data -	

N717-EA can implement program download, data communications, and debugging through the USB interface. Only slave mode is supported for USB of the module, which can be used as required. The recommended USB connection circuit is shown in Figure 4-14.

Figure 4-14 Recommended design of the USB interface



Schematic Design Guidelines

- Connect a 1 μF (C1) and a 33 pF (C2) filter capacitors as well as an ESD component (D1) in parallel to the USB_VBUS trace.
- Ensure that the junction capacitance of the ESD components (D2 and D3) in parallel to the USB_DP and USB_DM traces be smaller than 0.5 pF.
- Connecting a resistor of less than 10 Ω in series between the USB_DM and USB_DP pins of the module and the USB_DP and USB_DM pins of the USB host can effectively improve the EMI performance of the USB.

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PCB Design Guidelines

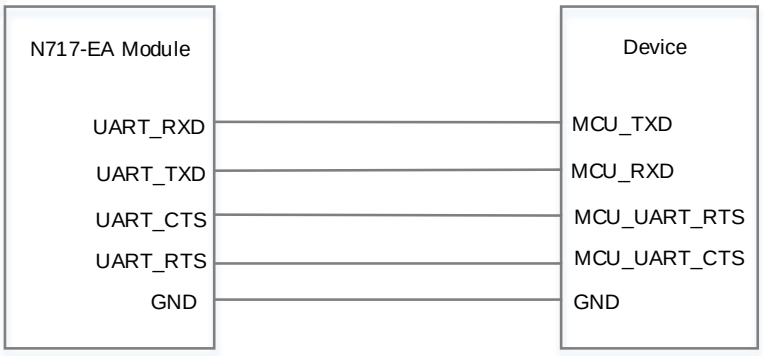
- Place the filter capacitor on the USB_VBUS as close to the module pins as possible, and place the ESD component as close to the USB connector as possible.
- Place the paralleled ESD component of the USB_DP and USB_DM traces as close to the USB connector as possible.
- It is important to route USB signal traces as differential pairs with ground surrounded. The impedance of the USB differential traces should be 90 Ω. The traces from the USB interface of your application PCB to the module must be isolated from other signal traces.

4.3.2 UART

Signal	Pin SN	I/O	Function description	Remarks
UART_DTR	30	DI	Data terminal ready	Software version (Standard): For communication based on AT commands. Software version (Open): For data transmission.
UART_RXD	34	DI	UART data input	
UART_TXD	35	DO	UART data output	
UART_RTS	36	DO	UART ready to send	
UART_CTS	37	DI	UART clear to send	
UART_DCD	38	DO	Data carrier detect	
UART_RI	39	DO	Ring indication	
DEBUG_UART_RXD	22	DI	DEBUG data input	For module debugging only.
DEBUG_UART_TXD	23	DO	DEBUG data output	

N717-EA provides two UART interfaces, one of which supports hardware flow control. The UART interface supports a 1.8 V voltage and its default buad rate is 115200 bps. The following figure shows recommended design of the interface.

Figure 4-15 Reference design of the UART interface



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Schematic Design Guidelines

- Pay attention to the correspondence between signal flow direction and connection.
- It is prohibited to use diodes for voltage-level translation.

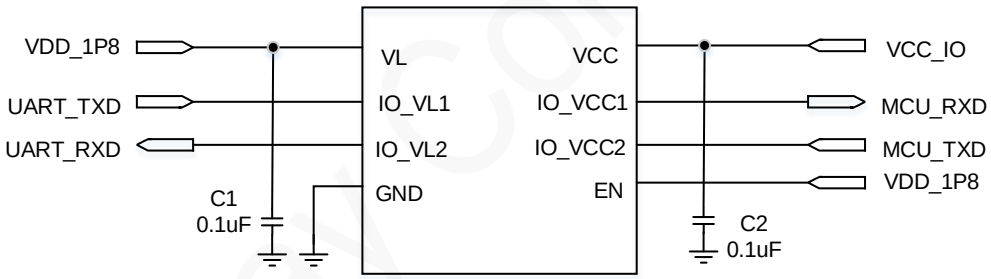
If the the logic voltage of UART does not match that of the MCU, add a voltage-level translation circuit outside the module. Three voltage-level translation circuits are recommended based on the differences in logic levels and rates.

The actual parameter values of the components used in the voltage-level translation circuit should be adjusted according to the actual test results. Note the differences between different circuit voltage-level translation solutions.

- Voltage-level translation chip circuit

  If the UART baud rate is greater than 115200 bps, it is recommended to design the voltage-level translation solution by referring to the recommended voltage-level translation circuit 1. As shown in Figure 4-16.

Figure 4-16 Recommended voltage-level translation circuit 1



  - VL is the reference voltage for IO_VL1 and IO_VL2, and the voltage range is 1.5 V - 5.5 V.
  - VCC is the reference voltage for IO_VCC1 and IO_VCC2, and the voltage range is 1.5 V - 5.5 V.
  - EN is an enable pin, which works at a voltage of greater than VL-0.2 V. In the above circuit, the EN pin is directly connected to VDD_1P8 and the level translator chip is always working.

- Dual-triode voltage-level translation circuit

  If the UART baud rate is not greater than 115200 bps, it is recommended to design the voltage-level translation solution by referring to the recommended voltage-level translation circuit 2.

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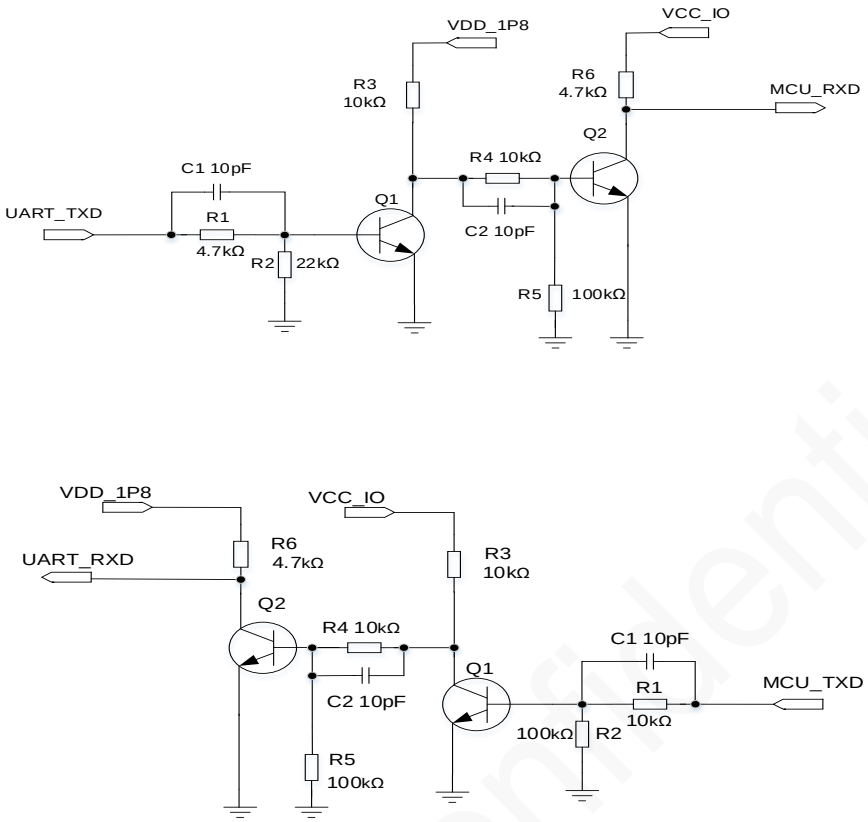
Figure 4-17 Recommended voltage-level translation circuit 2



MCU_TXD and MCU_RXD are the sending and receiving ports of MCU respectively, and UART_TXD and UART_RXD are the sending and receiving ports of module respectively. VCC_IO is the IO voltage of MCU and VDD_1P8 is the IO voltage of the module.

The circuit translates the voltage level through the turn-on and turn-off of the triode, and the dual triode can achieve higher voltage difference after voltage-level translation.

Schematic Design Guidelines

- Ensure that the base voltage of the triode is operating within the temperature range and the transistor can be fully turned on.
- It is recommended to reserve the acceleration capacitor, which can adjust the delay of the voltage-level translation circuit in some cases.

- Single-triode voltage-level translation circuit

  For the CTS/RTS/DCD/RI pin, it is recommended to design the voltage-level translation solution by referring to Figure 4-18.

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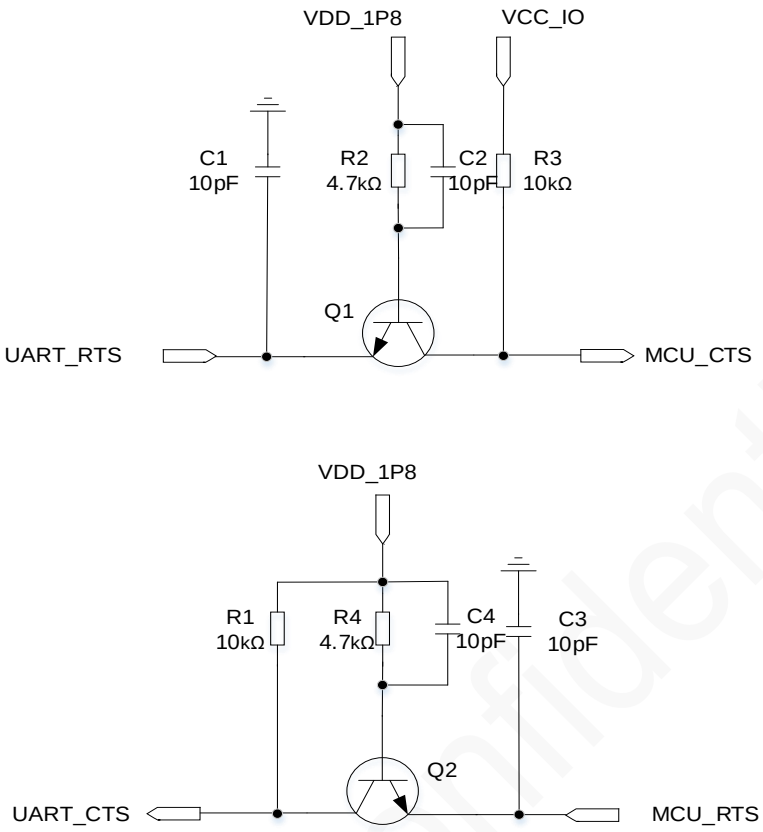
Figure 4-18 Recommended voltage-level translation circuit 3



MCU_CTS and MCU_RTS are the MCU-side signals, while UART_CTS and UART_RTS are the module-side signals. VCC_IO is the IO voltage of MCU and VDD_1P8 is the IO voltage of the module.

This single-triode voltage-level translation circuit is a one-way translation solution that works by conduction and cutoff of the triode. Please note the signal flow direction.

Schematic Design Guidelines

- The voltage difference between the high level and low level does not exceed 2 V.
- It is recommended to reserve the speed-up capacitor and adjust its capacitance value according to actual test results.
- The transistor base voltage is the lower value of the level between both sides.

4.3.3 USIM

Signal	Pin SN	I/O	Function description	Remarks
USIM1_DET	42	DI	USIM1 hot-swapping detection	-
USIM1_VCC	43	PO	USIM1 power output	-

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USIM1_RESET	44	DO	USIM1 reset	-
USIM1_DATA	45	B	USIM1 data input and output	This pin is pulled up to USIM1_VCC via a 4.7 kΩ resistor.
USIM1_CLK	46	DO	USIM1 clock output	-
USIM2_DET	83	DI	USIM2 hot-swapping detection	Currently not supported.
USIM2_CLK	84	DO	USIM2 clock output	
USIM2_RESET	85	DO	USIM2 reset	
USIM2_DATA	86	B	USIM2 data input and output	
USIM2_VCC	87	PO	USIM2 power output	

N717-EA provides two USIM interfaces that supports either 1.8 V or 3.0 V USIM card. USIM1 is valid by default. The recommended design of the USIM interface is shown in Figure 4-19 and Figure 4-20.

Figure 4-19 Recommended design of the USIM interface (normally close connector)

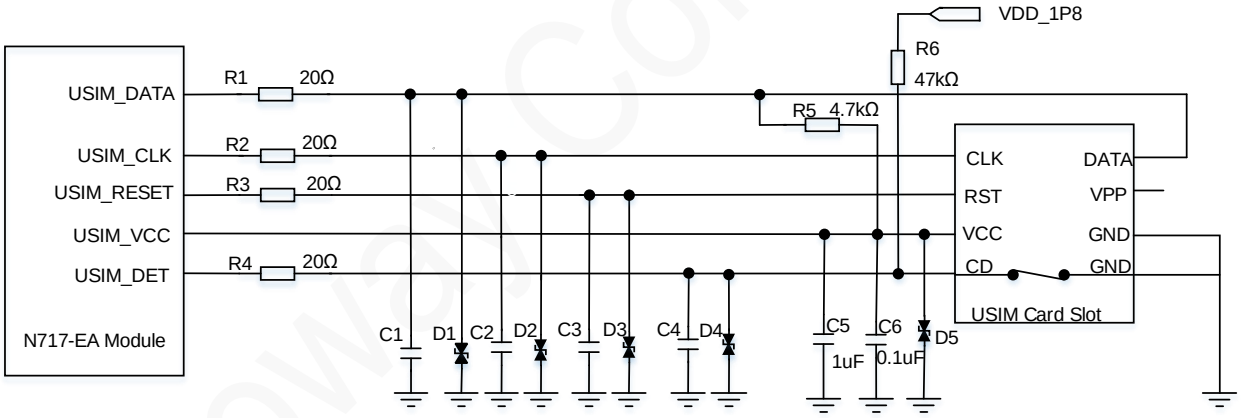

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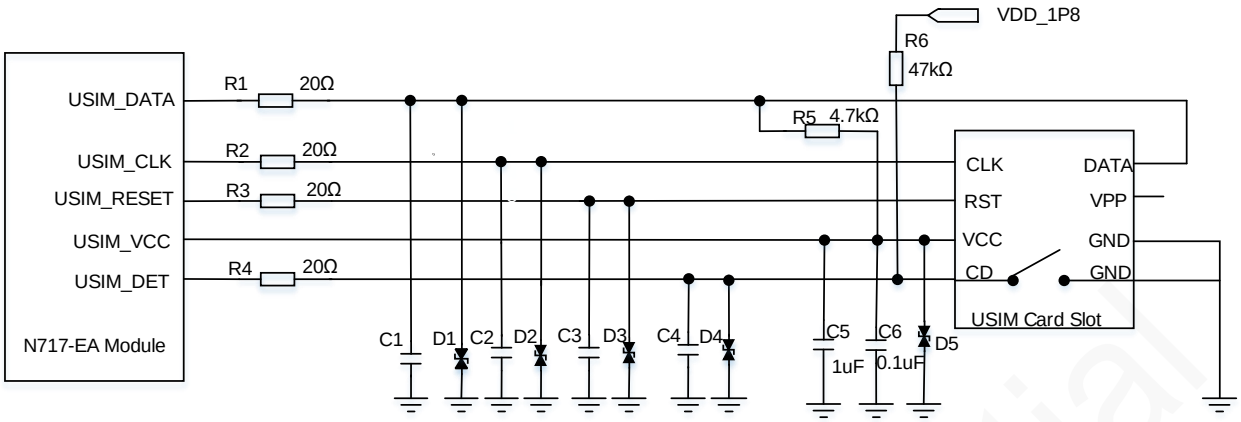
Figure 4-20 Recommended design of the USIM interface (normally open connector)



Schematic Design Guidelines

- USIM_VCC is the power supply of the USIM card, with load capacity of up to 50 mA. It is only used as power supply for the USIM card and shall not supply power to other loads.
- The USIM_DATA pin is not pulled up internally, so connecting it through a 4.7 kΩ external pull-up resistor to USIM_VCC is required.
- USIM_CLK is the clock signal pin for USIM card. The applications in complex electromagnetic environment require ESD protection of high quality, so it is recommended to add ESD protection components (junction capacitance no more than 7 pF) on each signal traces or directly add an integrated ESD device for alternative.
- Add a series resistor of no more than 20 Ω between each of the USIM_DATA, USIM_RESET, USIM_CLK, and USIM_DET pin and the card connector to enhance ESD performance. The resistors should be placed close to the card connector.
- C1 - C4 are in parallel to each USIM signal trace and are used to attach high-frequency filter capacitors. Their capacitance value should be not more than 10 pF.
- N717-EA supports USIM card detection, and USIM_DET is a 1.8 V interrupt pin. The USIM detection circuit works by checking the level of the voltage across the USIM_DET pin before and after a USIM card is inserted.
  - For the reference design circuit in Figure 4-19, SIM_DET is grounded before a USIM card is inserted and is pulled up to a 1.8 V voltage after a USIM card is inserted, so the high voltage level means USIM card detected while the low voltage level means no USIM card detected.
  - For the reference design circuit in Figure 4-20, SIM_DET is in a 1.8 V voltage before a USIM card is inserted and is grounded after a USIM card is inserted, so the high voltage level means no USIM card detected while the low voltage level means USIM card detected.

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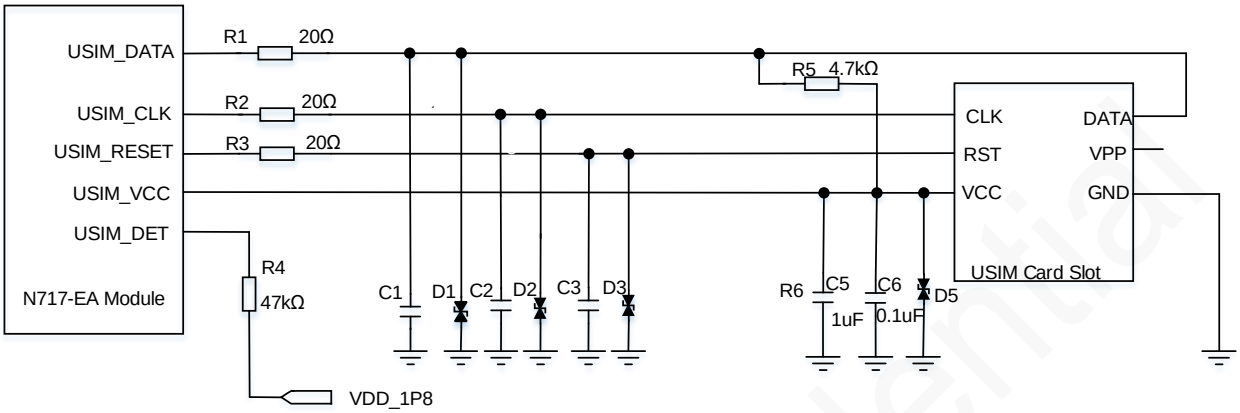
If the USIM hot-swapping function is not required, the USIM_DET pin must be pulled up to 1.8 V via a 47 kΩ resistor in series, and the USIM hot-swapping detection function must be disabled in the software. Figure 4-21 shows the reference design of the USIM card interface (without hot-swapping function) .

Figure 4-21 Reference design of USIM card interface (without hot swap function)



PCB Design Guidelines

- USIM cards and their signal traces often be jammed by RF radiation, resulting in USIM abnormalities. Therefore, keep the USIM card connector far away from the antenna and RF circuits.
- Keep the USIM card connector close to the module and keep USIM traces as short as possible.
- On the USIM traces, connect the series resistors and ESD protection components close to the USIM card connector.
- To avoid cross-talk between USIM signal traces, shield them with surrounded ground.

4.3.4 PCM

Signal	Pin SN	I/O	Function description	Remarks
PCM_CLK	4	DO	PCM data clock	-
PCM_SYNC	5	DO	PCM data frame synchronization	-
PCM_DIN	6	DI	PCM data input	-
PCM_DOUT	7	DO	PCM data output	-

N717-EA provides one PCM interface, supporting a 1.8 V voltage. The following shows the reference design of the PCM interface.

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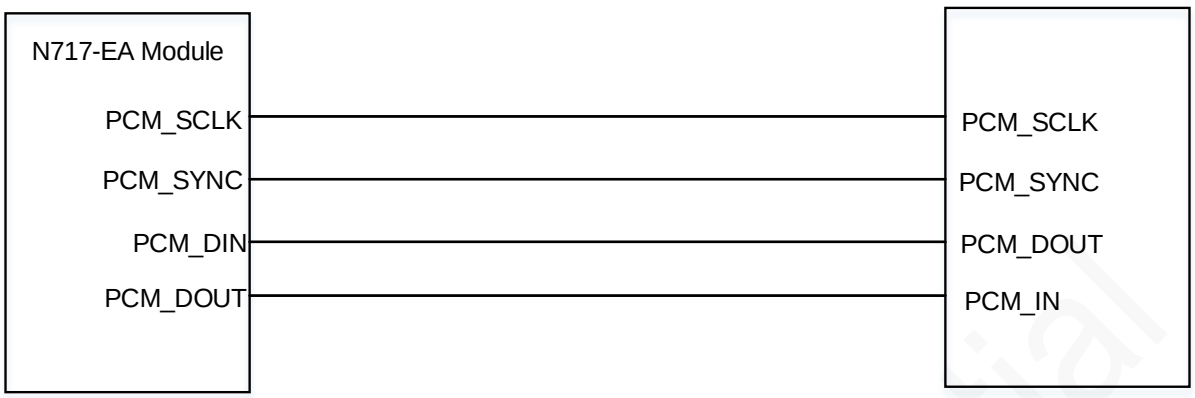
Figure 4-22 Reference design of the PCM interface



Schematic Design Guidelines

If the logic levels between the N717-EA module and Codec do not match, you should add a voltage-level translation solution.

PCB Design Guidelines

- Avoid crossing of PCM signal traces with other traces. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the traces.
- Route PCM traces as far away as possible from areas that may introduce ESD.
- Shield the PCM_SCLK trace with surrounded ground, and for other PCM traces, shielding with surrounded ground is also recommended.

4.3.5 I2C

Signal	Pin SN	I/O	Function description	Remarks
I2C_SCL	40	DO	I2C clock	Connecting this pin through a pull-up resistor (4.7 kΩ recommended) to VDD_1P8 is required.
I2C_SDA	41	B	I2C data	

N717-EA provides one 1.8 V I2C interface, supporting only master mode and speed rates up to 3.4 Mbps. The following figure shows the recommended reference design of the interface.

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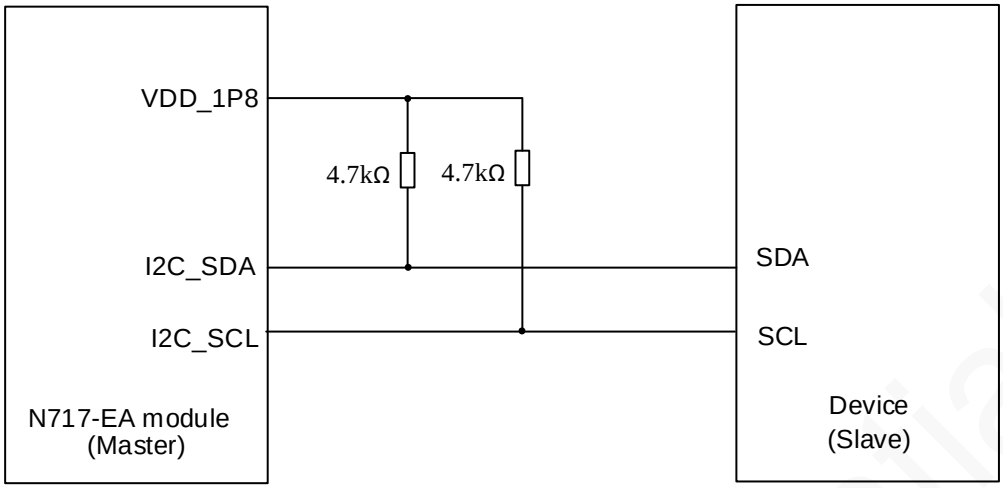
Figure 4-23 Reference design of the I2C interface



4.4 Audio Interfaces

N717-EA provides many audio input and output interfaces to meet the needs of audio in different environments.

4.4.1 Analog Audio Input

Signal	Pin SN	I/O	Function description	Remarks
MIC_BIAS	120	PO	Microphone bias voltage output	-
MIC_N	119	AI	MIC analog input -	-
MIC_P	126	AI	MIC analog input +	-

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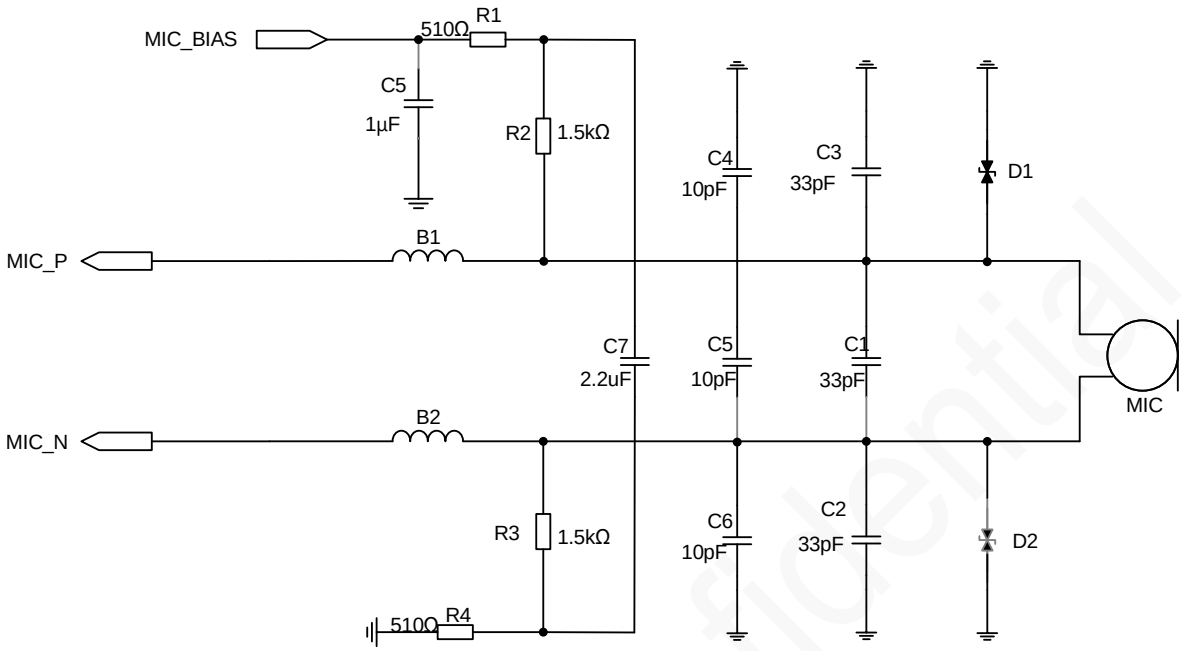
N717-EA supports one MIC differential input. The following figure shows the reference design.

Figure 4-24 Reference design of the differential MIC input



Schematic Design Guidelines

- D1 and D2 are designed to attach TVS diodes, which are used to prevent MIC from introducing ESD and damaging the module.
- C1 and C6 are designed to attach filter capacitors, which are mainly used to filter out interference signals and their capacitance values can be adjusted according to actual debugging result.
- B1 and B2 are designed to attach magnetic beads, which are used to filter out high-frequency noise. Magnetic beads with 1800 Ω @ 100 MHz or higher and DC impedance less than 1.5 Ω are preferred. It is recommended to use dedicated magnetic beads for audio.
- It is recommended to use an electret microphone with built-in RF filter dual capacitors (such as 10 pF and 33 pF) to filter RF interference from the source and reduce TDD coupling noise.

PCB Design Guidelines

- MIC_P and MIC_N traces should comply with the differential rules.
- Shield the audio traces with surrounded ground. Keep them not less than 3 times the audio trace width away from other signal traces.
- Place RF filter capacitors close to the audio components or pins.
- Keep the audio traces far away from interference sources, such as DC-DC power supply.

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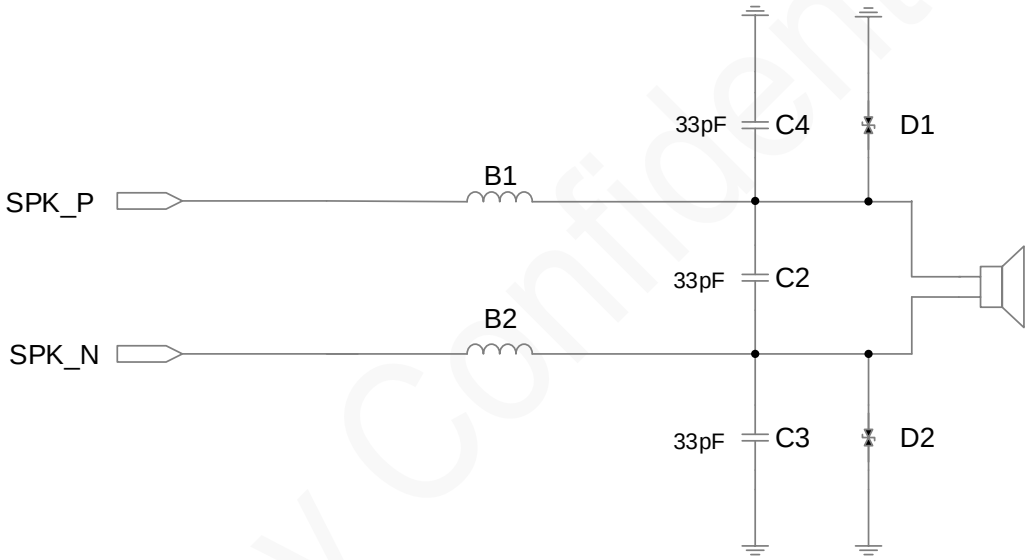
4.4.2 Analog Audio Output

Signal	Pin SN	I/O	Function description	Remarks
SPK_P	121	AO	Analog audio output +	Supports driving power of up to 37 mW with a 32 Ω load. If higher driving power is required, connect this interface to an external power amplifier.
SPK_N	122	AO	Analog audio output -	

The following shows the reference design of the audio output interface.

Figure 4-25 Reference design of the differential SPK input



Schematic Design Guidelines

- C2, C3 and C4 are designed to attach filter capacitors, which are used to filter out high-frequency interference.
- D1 and D2 are designed to attach TVS diodes, which are used to prevent ESD from damaging the module.
- B1 and B2 are designed to attach magnetic beads, which are used to filter out high-frequency noise. It is recommended to use dedicated magnetic beads for audio frequency.

  Special attention should be paid to the DC resistance of the magnetic bead. The impedance of the audio output device is generally small, so if the DC resistance of magnetic bead is too large, too much audio power will be consumed. In principle, the smaller DC resistance of the magnetic bead is preferred. It is recommended to select the magnetic bead with DC resistance less than 0.1 Ω.

PCB Design Guidelines

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- The audio signal traces should be wide enough (0.5 mm is recommended) to bear large current when audios are outputted at a highest volume. Isolate the audio traces from high-speed digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough ground via-holes and ground reference layer protection.
- Keep the audio traces far away from antenna to reduce jamming. Avoid parallel layout between power supply traces and the audio traces.
- It is important to route the audio signal traces as differential pairs.

4.5 RF Interface

Signal	Pin SN	I/O	Function description	Remarks
ANT_MAIN	60	AIO	Main antenna	-

4.5.1 ANT_MAIN Antenna Interface

For the N717-EA module to be applicable to your PCB, the characteristic impedance of the ANT_MAIN antenna interface should be controlled at 50 Ω and the impedance of the trace from the module's antenna interface to the antenna needs to be kept at 50 Ω to allow reception of radio frequency (RF) signals. In the circuit design, a matching network is essential for antenna matching in the circuit design. The matching network is generally divided into three types: L type, T type, and π type, which are shown in the following figure. The π-type matching circuitry is preferred.

Figure 4-26 L-type RF matching schematics

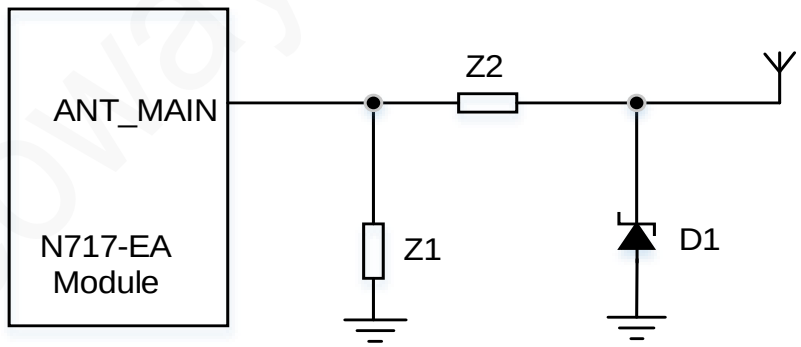

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Figure 4-27 T-type RF matching schematics

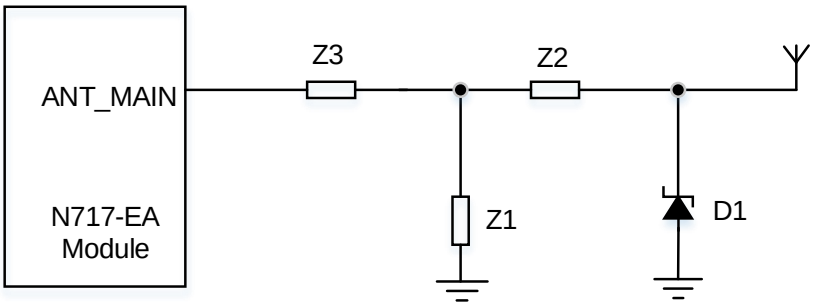
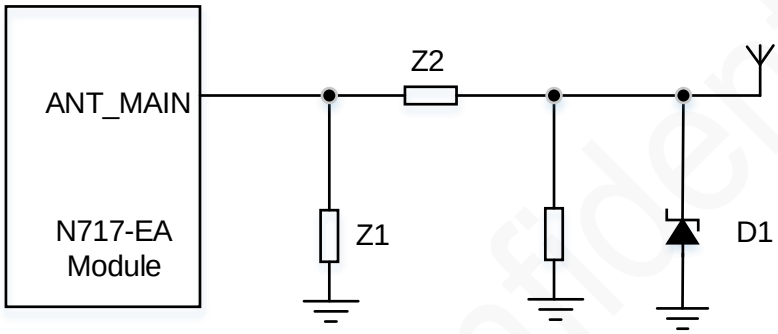


Figure 4-28 π-type RF matching schematics



Schematic Design Guidelines

- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- If static electricity may be introduced through the antenna, it is recommended to add ESD components with ultra-low junction capacitance for static electricity protection. ESD components with junction capacitance less than 0.5 pF are preferred. Besides, it is necessary to ensure that the reverse breakdown voltage of the ESD component is greater than 10 V, and ESD components with reverse breakdown voltage above 15 V are preferred.

PCB Design Guidelines

- Lay grounding copper foil and dig dense ground via-holes around the RF traces for isolation. Keep the RF traces as short as possible and control their characteristic impedance at 50 Ω
- To avoid antenna performance being affected significantly by the parasitic capacitance of a large RF pad when using SMA connector, the first layer and fourth layer under the module's RF pad or all layers must be drilled to form a through-hole structure. The following is the recommended RF PCB design.

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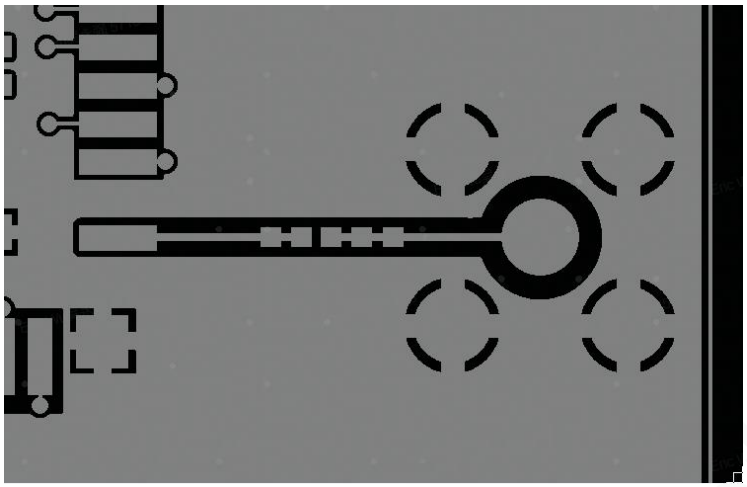
Figure 4-29 Recommended RF PCB design



- On the PCB, keep the RF signals and components far away from digital circuits, switching power supplies, power transformers, power inductors, clock signals, etc.

4.5.2 Antenna Assembling

The antenna used by the module must comply with the mobile device standard. The standing wave ratio should be between 1.1 and 1.5, and the input impedance should be 50 Ω. Requirements for antenna gain vary according to the application environment. You can choose an appropriate antenna according to specific application scenarios and environments.

The module antenna interface can be connected with rubber rod antenna, sucker antenna or internal Picofarad antenna, and good shielding is required between the external antenna and the RF pin. While using an external RF antenna, keep the external RF cables far away from all interference sources, especially digital signals and switching power supply.

The following methods are commonly used to assemble antennas:

- Reference design for external antennas (GSC RF connector)

  MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

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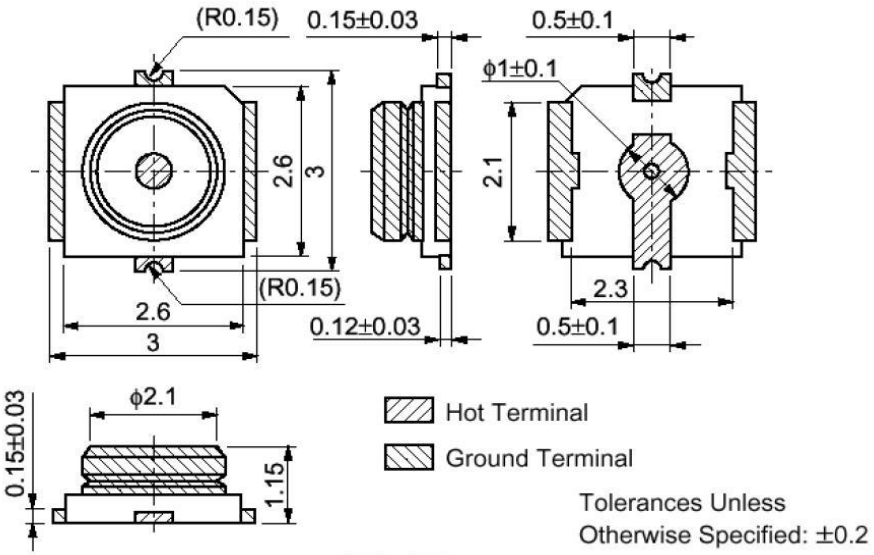
Figure 4-30 Murata RF connector encapsulation specifications



- Connecting to an external antenna by soldering

  It is not recommended to solder the RF cables to the module directly since the stability, consistency, and RF performance are not good.

The following show the two types of connections.

Figure 4-31 RF cable connections

- PCB printing or SMT

  The module works in a wide frequency range, but it is difficult for PCB antennas or ceramic antennas to cover a wide frequency. Therefore, this connection method is recommended only for 2.4 GHz Wi-Fi or BT/ BLE antennas.

The following figure shows the layout of the 2.4 GHz ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

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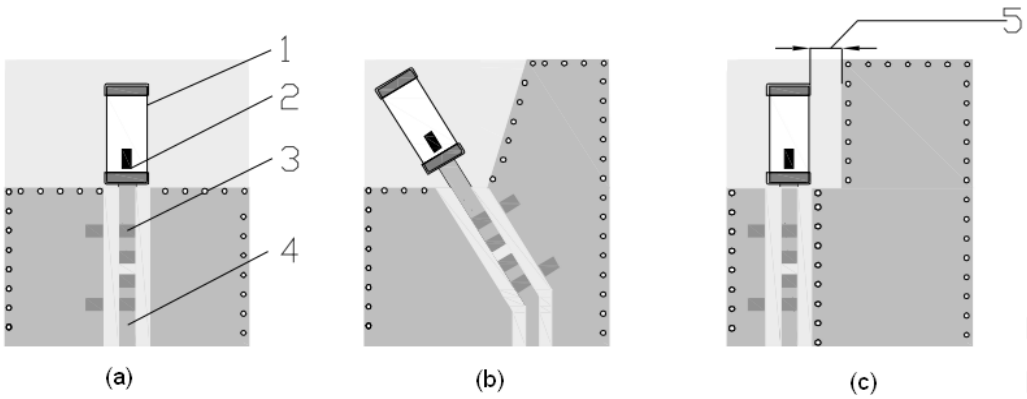
Figure 4-32 Antenna layout

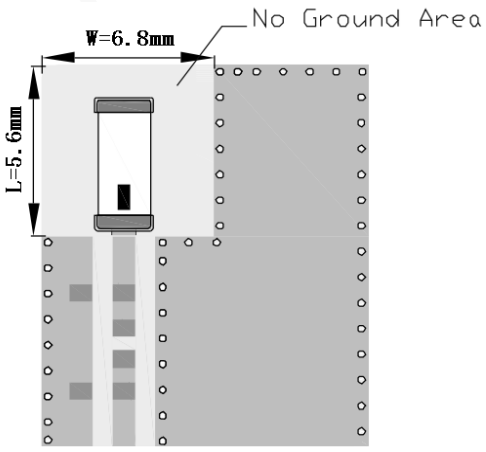


If your PCB is large enough, you can adopt the layout shown in Figure 4-32 (a).

- 1 Chip antenna
- 2 Feeding mark
- 3 Solder pad of the matching circuitry
- 4 50 Ω characteristic impedance RF trace

Figure 4-33 shows the "No Dround Area" between the antenna and ground that is marked as "5" in Figure 4-32.

Figure 4-33 Clearance area around the antenna on the PCB board



For more details, please refer to the antenna manual and instruction documentation.

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4.6 Other Functional Interfaces

4.6.1 WAKEUP_IN

Signal	Pin SN	I/O	Function description	Remarks
WAKEUP_IN*	96	DI	Wake up the module.	Under development

WAKEUP_IN is used to set the module into sleep mode and needs to be used together with the AT command. For details of the AT command, see *Neoway_N717-EA_AT_Commands_Manual.* In sleep mode, the module can still responds to voice calls, SMS, and processes data services normally.

The following shows the process of entering sleep mode.

Figure 4-34 Process of entering into sleep mode

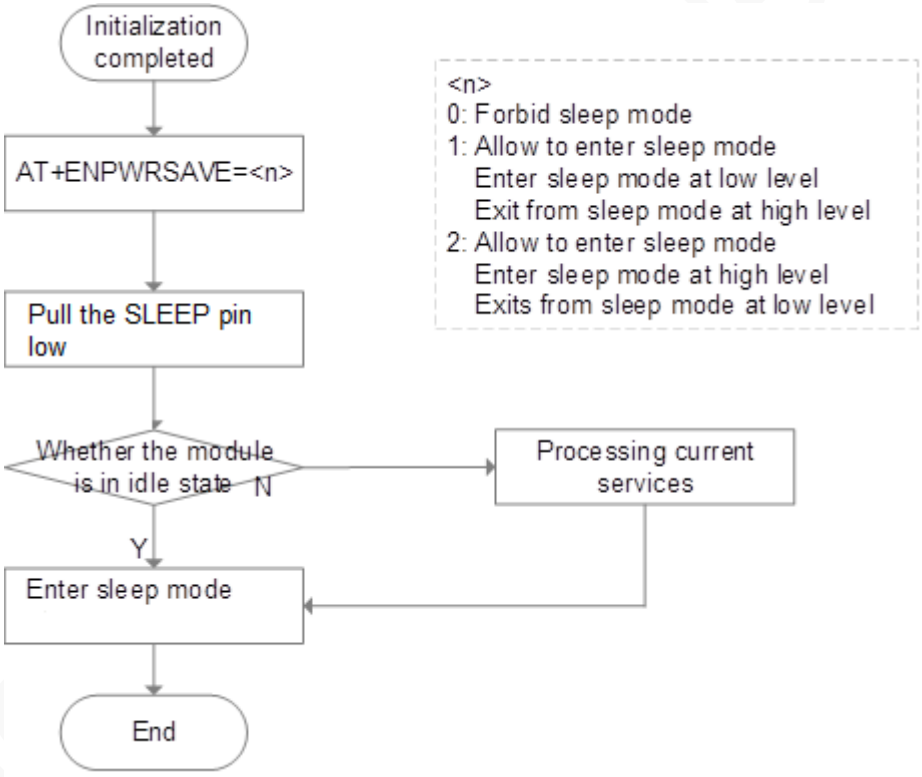

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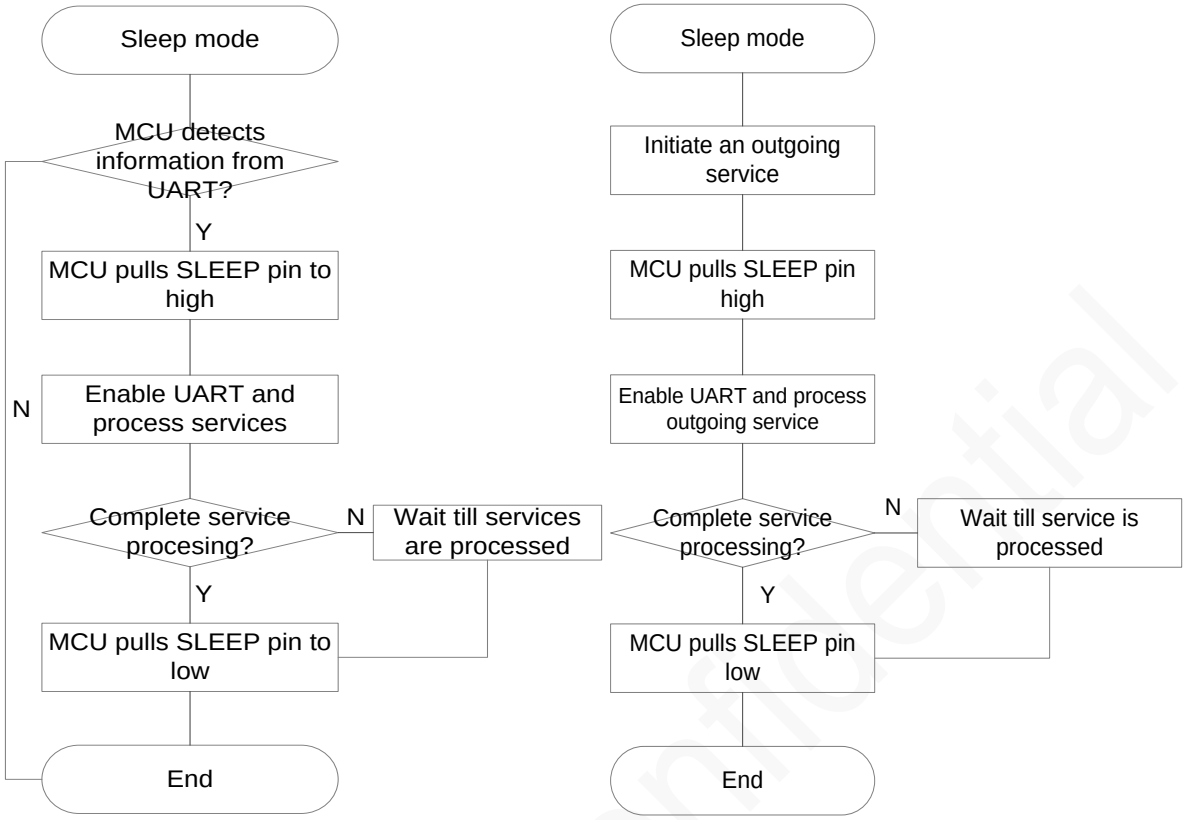
Figure 4-35 Process of processing data services in sleep mode



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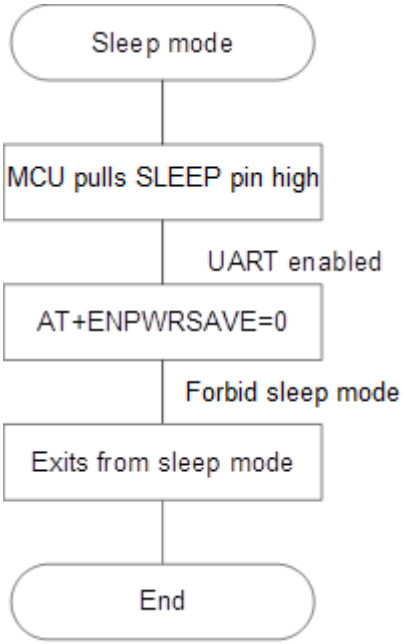
The following shows the process of waking up the module from sleep mode.

Figure 4-36 Process of waking up the module



4.6.2 Network Status Indication

Signal	Pin SN	I/O	Function description	Remarks
SLEEP_IND	1	DO	Sleep mode indicator	-
STATUS	20	DO	Working status indication	-
NET_LIGHT	21	DO	Network status indicator	-

SLEEP_IND, STATUS, and NET_LIGHT are respectively the sleep mode indication, running status indication, and network status indication pin. The indication pin can output PWM waveforms with different duty cycles according to different operating states of the module and drive LED indicators to flash at different frequencies. Through AT + SIGNAL command, the LED indicator can be set to flash according to different states. Please refer to *Neoway_N717-EA_AT_Commands_Manual* for details.

It is recommended to add a triode between the indication pins and the LED indicators instead of directly driving LED indicator since they only output a 1.8 V voltage. The following figure shows the recommended reference design.

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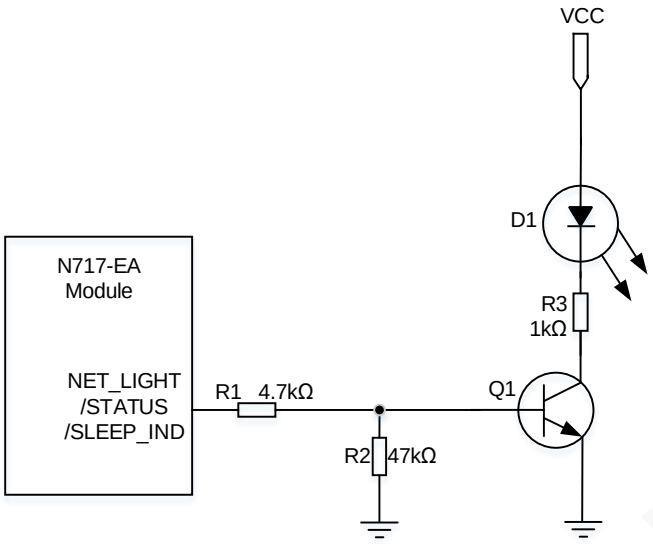
Figure 4-37 Driving LED indicators with a triode

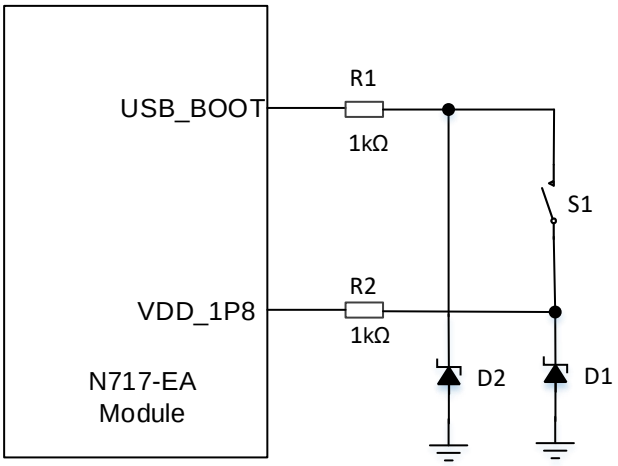


4.6.3 USB_BOOT

Signal	Pin SN	I/O	Function description	Remarks
USB_BOOT	75	DI	Emergency download control	-

N717-EA provides a USB_BOOT pin, which is used to enter the emergency download mode. After the USB_BOOT pin is pulled up to VDD_1P8 before the module is powered up, the module can enter the emergency download mode when it is powered on. This method is used as an emergency solution for product startup failure or malfunction. It is recommended to reserve this pin. The following figure shows the reference design of this pin. Adding an ESD component to protect USB_BOOT in the circuit is required.

Figure 4-38 Reference design of USB_BOOT pin



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5 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

5.1 Electrical Characteristics

- If the voltage is lower than the threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it outputs a current not less than 3 A. The 3 A current corresponds to the maximum power level of the module at GSM mode, and the peak current during burst transmission lasts for a short time. Placing a large capacitor at the VBAT pin of the module can effectively enhance the freewheeling current of the power supply and avoid abnormalities such as module shutdown caused by excessive voltage drop.

Table 5-1 N717-EA electrical characteristics

Signal		Min. value	Typical value	Max. value
VBAT_BB	V_{in}	3.4 V	3.6 V	4.2 V
	I_{in}	N/A	N/A	0.8A
VBAT_RF	V_{in}	3.4 V	3.6 V	4.2 V
	I_{in}	N/A	N/A	2.2A

Table 5-2 N717-EA current consumption (typical)

States / Frequency band	Power (dBm)	Sleep(mA)	Idle(mA)	Active (mA) @ max power
LTE-FDD: B1, B3, B5, B7, B8, B20, B28, B31	23	TBD	TBD	TBD
LTE-TDD: B38, B40, B41	23	TBD	TBD	TBD
GSM900	33	TBD	TBD	TBD
GSM1800	30	TBD	TBD	TBD

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5.2 Temperature Characteristics

Table 5-3 N717-EA temperature characteristics

Parameters	Min. value	Typical value	Max. value
Operating	-30℃	25℃	75℃
Extended	-40℃	25℃	85℃
Storage	-40℃	25℃	90℃

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse and cannot meet the requirements of 3GPP specification, but it will not have a great impact on the normal use of the module. After the temperature is restored, the RF performance can be restored to meet the 3GPP specification.

5.3 ESD Protection Characteristics

As electronic products need to undergo strict ESD testing, the following items are the electrostatic protection capabilities of the main pins of the module. When designing related products, you need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25℃

Table 5-4 N717-EA ESD protection characteristics

Test point	Contact discharge	Air discharge
VBAT, GND	±8 kV	±15 kV
ANT interface	±8 kV	±15 kV
Shielding cover	±8 kV	±15 kV

The above test data are obtained from the test using a N717-EA_EVB of Neoway.

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6 RF Characteristics

The module provides connectivity on GSM, FDD-LTE (Cat.1) and TDD-LTE (Cat.1) networks. This chapter introduces the RF characteristics of N717-EA.

6.1 Operating Frequency Bands

Table 6-1 N717-EA operating frequency bands

Operating frequency band	Uplink	Downlink
EGSM900	880 - 915 MHz	925 - 960 MHz
DCS1800	1710 - 1785 MHz	1805 - 1880 MHz
FDD-LTE B1	1920 - 1980 MHz	2110 - 2170 MHz
FDD-LTE B3	1710 - 1785 MHz	1805 - 1880 MHz
FDD-LTE B5	824 - 849 MHz	869 - 894 MHz
FDD-LTE B7	2500 - 2570 MHz	2620 - 2690 MHz
FDD-LTE B8	880 - 915 MHz	925 - 960 MHz
FDD-LTE B20	832 - 862 MHz	791 - 821 MHz
FDD-LTE B28	703 - 748 MHz	758 - 803 MHz
FDD-LTE B31	452.5 - 457.5 MHz	462.5 - 467.5 MHz
TDD-LTE B38	2570 - 2620 MHz	2570 - 2620 MHz
TDD-LTE B40	2300 - 2400 MHz	2300 - 2400 MHz
TDD-LTE B41	2535 - 2655 MHz	2535 - 2655 MHz

6.2 Power and Sensitivity

Table 6-2 N717-EA RF transmitting power

Frequency band	Max power	Min. power
EGSM900	33 dBm ± 2 dB	5 dBm±5 dB

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DCS1800	30 dBm ± 2 dB	0 dBm±5 dB
EGSM900 (8-PSK)	27 dBm ± 3 dB	5 dBm ± 5 dB
DCS1800 (8-PSK)	26 dBm ± 3 dB	0 dBm ± 5 dB
FDD-LTE B1	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B3	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B5	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B7	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B8	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B20	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B28	23 dBm ± 2 dB	< -39 dBm
FDD-LTE B31	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B38	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B40	23 dBm ± 2 dB	< -39 dBm
TDD-LTE B41	23 dBm ± 2 dB	< -39 dBm

Table 6-3 N717-EA GSM RX sensitivity

Frequency band	RX sensitivity
EGSM900	≤ -108 dBm
DCS1800	≤ -106 dBm

Table 6-4 N717-EA LTE RX sensitivity

Frequency band	RX sensitivity	Duplex mode
FDD-LTE B1	≤ -96.3 dBm	FDD
FDD-LTE B3	≤ -96 dBm	FDD
FDD-LTE B5	≤ -97 dBm	FDD
FDD-LTE B7	≤ -95.5 dBm	FDD
FDD-LTE B8	≤ -97 dBm	FDD
FDD-LTE B20	≤ -97 dBm	FDD
FDD-LTE B28	≤ -97.5 dBm	FDD
FDD-LTE B31	≤ -97 dBm	FDD
TDD-LTE B38	≤ -97 dBm	TDD

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TDD-LTE B40	≤ -97 dBm	TDD
TDD-LTE B41	≤ -97 dBm	TDD

The preceding indicators are tested in a shielded environment in the laboratory.

- Test condition for the above all bands except for LTE B31: 10 MHz bandwidth, QPSK, 1 or full RB (set according to the protocol).
- Test condition for LTE B31: 5 MHz bandwidth, QPSK, 1 or full RB (set according to the protocol).
  On no-shielded environments, deviations may exist in the receiver sensitivity of some individual bands due to the interference.

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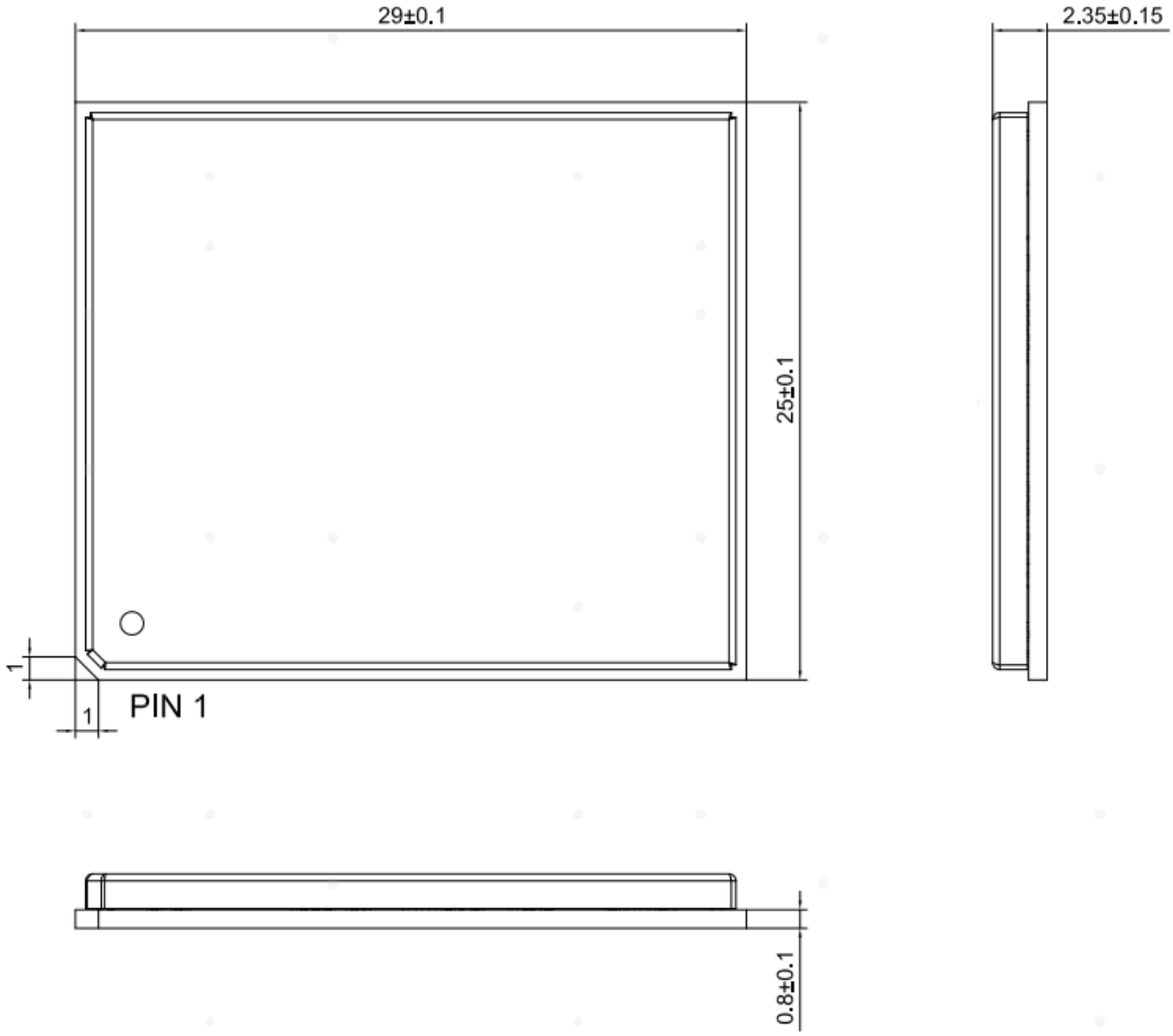
7 Mechanical Characteristics

This chapter describes mechanical characteristics of the N717-EA module.

7.1 Dimensions

Figure 7-1 N717-EA top and side view dimensions (unit: mm)



7.2 Labeling

The N717-EA label is laser etched, and can withstand a high temperature of 260°C. The following shows the label format of N717-EA.

The above figure is for reference only. For authentic appearance, please refer to the module that you receive from Neoway.

7.3 Packaging

N717-EA adopts the SMT method for oven soldering. To enable efficient production, production lot set-up and tear-down, the modules are delivered as hermetically sealed reeled tapes for moisture-proof packaging and use the aluminum foil bag, desiccant, humidity indicator card, vacuum and other processing methods to ensure the dryness of the product and extend its service life.

7.3.1 Reels

N717-EA in mass production is delivered in the following packaging.

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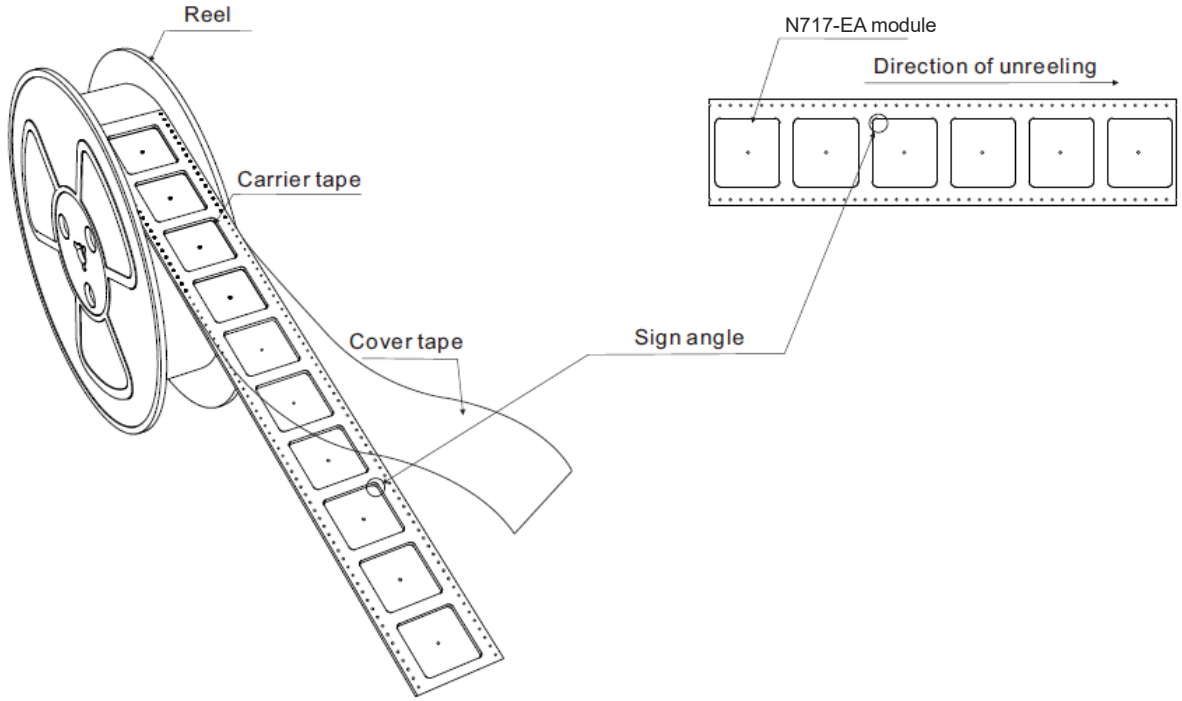

7.3.2 Moisture

N717-EA is a level 3 moisture-sensitive electronic element, in compliance IPC/ JEDEC J-STD-020 standard.

- Recommended storage condition: the temperature should be less than 40°C and the relative humidity should be less than 90%.
- The storage life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.
- Production environment condition: 30°C/60%

After the module is unpacked, if it is exposed to the air for a long time, the module will get damped, and may be damaged during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at a temperature higher than 120°C for more than 6 hours.

The module should be pre-baked under the following circumstances:

- 48 hours after the vacuum-sealed packaging is removed.
- The relative humidity is greater than 10% (you can see the humidity card that comes with the package).

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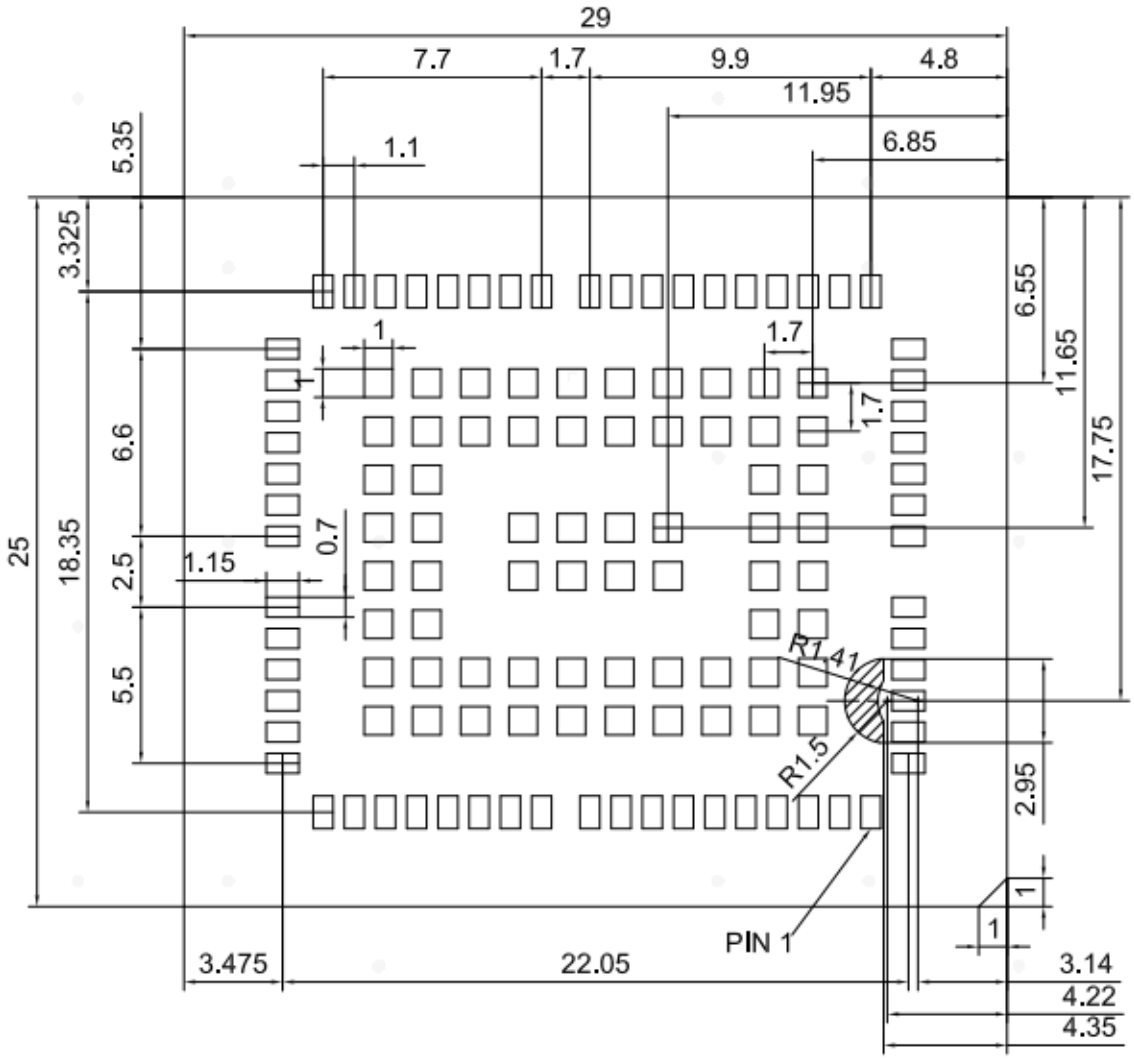
8 Mounting

This chapter describes the module PCB package and application PCB package, as well as the key points of SMT related technology.

8.1 PCB Package

Figure 8-1 N717-EA PCB package (bottom view, unit: mm)



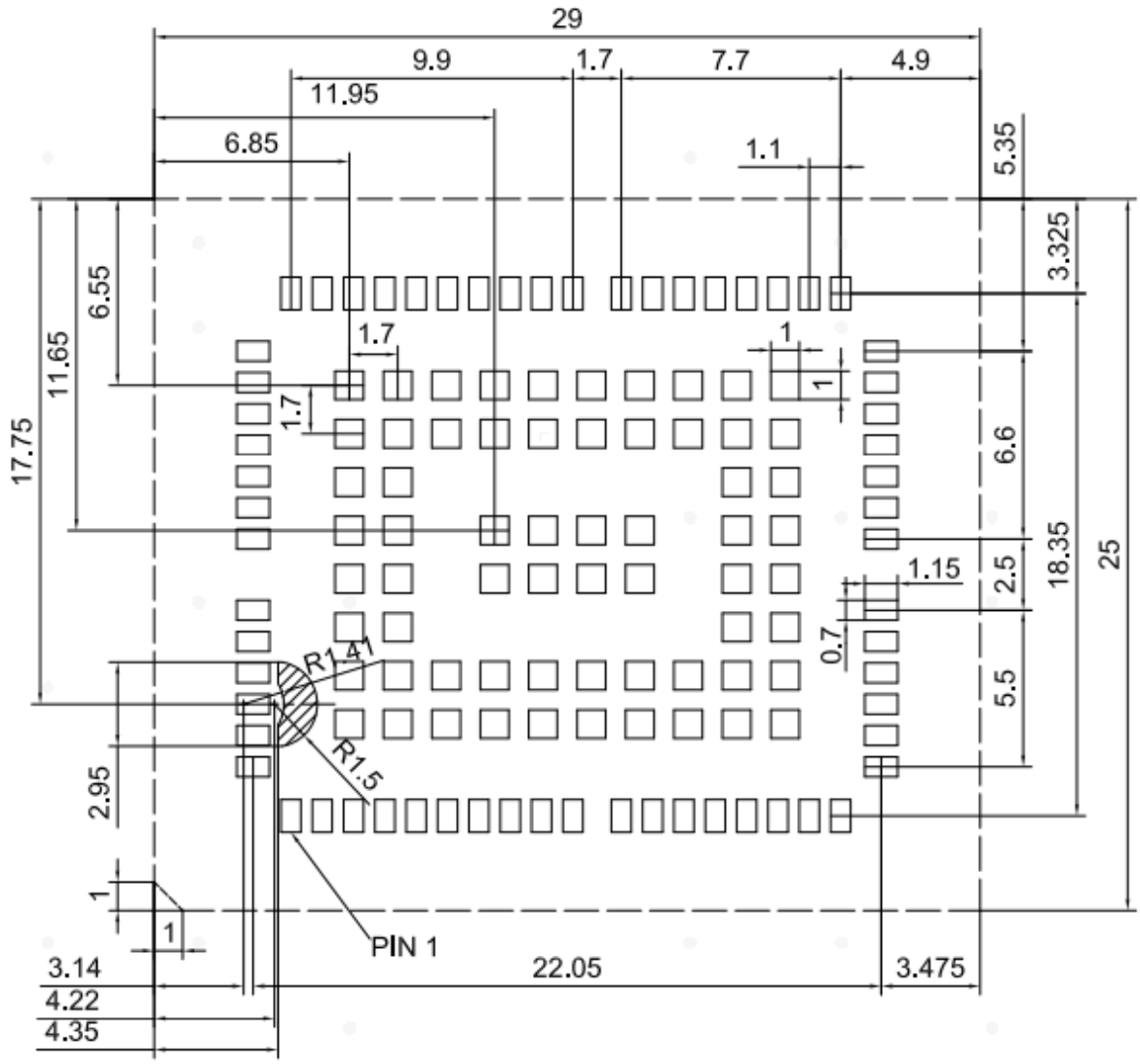
8.2 Application PCB Package

N717-EA adopts the 126-pin LGA form package. The recommended application PCB package is as follows:

Only GND via-holes and pour coppers are allowed in the shaded area "▨" of the PCB package to ensure the proper operation of the module.

To achieve higher yield during module production, it is recommended that the distance between other components on the PCB board and the module pads be at least 3 mm to avoid the risk of tin connection when using stepped stencil.

Figure 8-2 N717-EA application PCB package (top view, unit: mm)



8.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

8.4 Solder Paste

The thickness of the solder paste and the flatness of the PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process parameters is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220°C for more than 45 seconds and the peak temperature reaches 240°C.

8.5 SMT Oven Temperature Profile

Neoway will not provide warranties for heat-responsive element abnormalities caused by improper temperature control.

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

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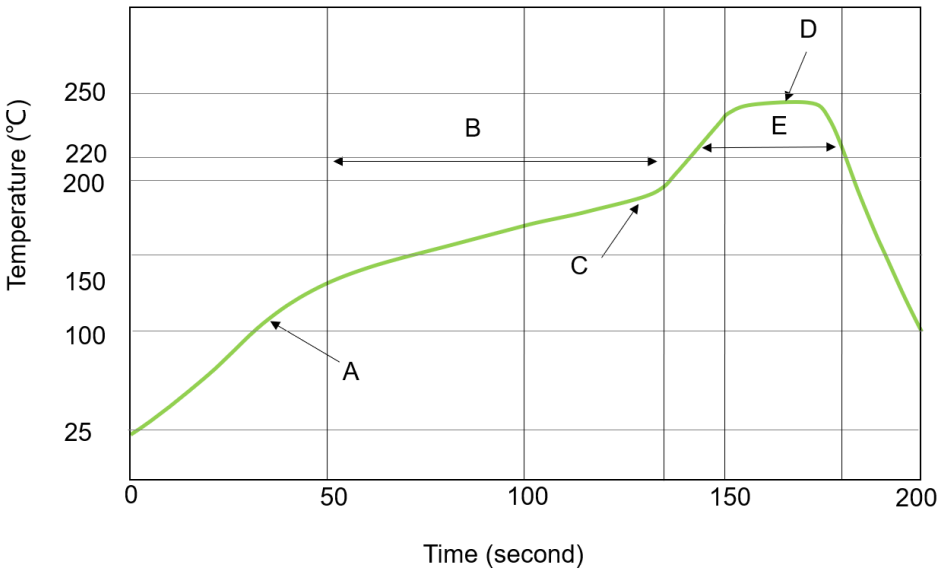
Figure 8-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4°C/sec
- Ramp down rate: -3 to -1°C/sec
- Soaking zone: 150 to 180°C, Time: 60 to 100s
- Reflow zone: > 220°C, Time: 40 to 90s
- Peak temperature: 235 - 245°C

For information about N717-EA storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 245°C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module at high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

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A Abbreviations

Abbreviation	Full name
AI	Analog Input
AO	Analog Output
AIO	Analog Input /Output
ARM	Advanced RISC Machine
bps	Bits per Second
CCC	China Compulsory Certification
CTS	Clear to Send
DC	Direct Current
DI	Digital Input
B	Digital Input/Output
DL	Downlink
DO	Digital Output
DRX	Discontinuous Reception
DTR	Data Terminal Ready
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance
EVK	Evaluation Kit
FDD	Frequency Division Duplexing
FTP	File Transfer Protocol
FTPS	FTP Secure
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
EGSM	Enhanced GSM
3GPP	3rd Generation Partnership Project
IO	Input/Output
ISP	Image Signal Processor
LCC	Leadless Chip Carriers

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LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
PCB	Printed Circuit Board
PCS	Personal Communications Service
PWM	Pulse Width Modulation
QVGA	Quarter Video Graphics Array
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
RTC	Real Time Clock
SPK	Speaker
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage

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