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N715-EA

Hardware User Guide

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Notice

This document provides guide for users to use N715-EA.

This document is intended for system engineers (SEs), development engineers, and test engineers.

THIS GUIDE PROVIDES INSTRUCTIONS FOR CUSTOMERS TO DESIGN THEIR APPLICATIONS. PLEASE FOLLOW THE RULES AND PARAMETERS IN THIS GUIDE TO DESIGN AND COMMISSION. NEOWAY WILL NOT TAKE ANY RESPONSIBILITY OF BODILY HURT OR ASSET LOSS CAUSED BY IMPROPER OPERATIONS.

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About This Document

Scope

This document is applicable to N715-EA.

It defines the features, indicators, and test standards of the N715-EA module and provides reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2022-11	Initial draft	Wu Yongqiang
1.1	2022-12	Added a note of the precautions for the pad lay-out in Figure 4-1. Updated the storage time and baking time after the module package is unpacked and damp. Updated the power consumption values in chapter 6.1 “Electrical Characteristics”. Updated the Table 6-4 “ESD protection characteristics”	Wu Yongqiang

Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

1 Safety Recommendations

Ensure that this product is used in compliance with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or workplace:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, and so on.

  If the product is used in a place with flammable gas or dust such as propane gas, gasoline, or flammable spray, the product will cause an explosion or fire.

- Do not use this product in environments such as hospital or airplane where it might interfere with other electronic equipment.

  If the product is used in medical institutions or on airplanes, electromagnetic waves emitted by this product may interfere with surrounding equipment.

Follow the requirements below in design and use of the application for this module:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not insert/remove a SIM card or memory card into/from the module while it is not powered off.

2 About N715-EA

This chapter introduces product overview, block diagram, and basic features of N715-EA.

2.1 Product Overview

N715-EA is a 4G industrial-grade cellular module developed based on UIS8910DM and its dimensions are (23.80 ± 0.1) mm × (22.80 ± 0.1) mm × (2.5 ± 0.15) mm. The module supports GSM, FDD-LTE (Cat.1), and TDD-LTE (Cat.1). With rich hardware interfaces and support for audio, video, Wi-Fi positioning, and BT/BLE, the module is applicable to developing IoT communications devices including wireless meter reading terminals, shared bikes, industrial smart communications device, and cloud horn.

N715-EA has the following characteristics:

- ARM Cortex-A5 processor, 500 MHz main frequency, 32 kB L1 cache.
- Supports LTE Cat.1
- Supports USB2.0/USIM/ADC/UART/SDIO/SPI/I2C/KEYPAD/MIC/EAR/SPK/HEADSET

Table 2-1 lists the variant and bands that N715-EA supports.

Table 2-1 Variants and frequency bands

Variant	Region	Category	Band	GNSS	Codec
EA	Europe	Cat1	FDD-LTE: B1, B3, B5, B7, B8, B20, B28 TDD-LTE: B38, B40, B41 GSM/GPRS: 900/1800 MHz	Not supported	Supported

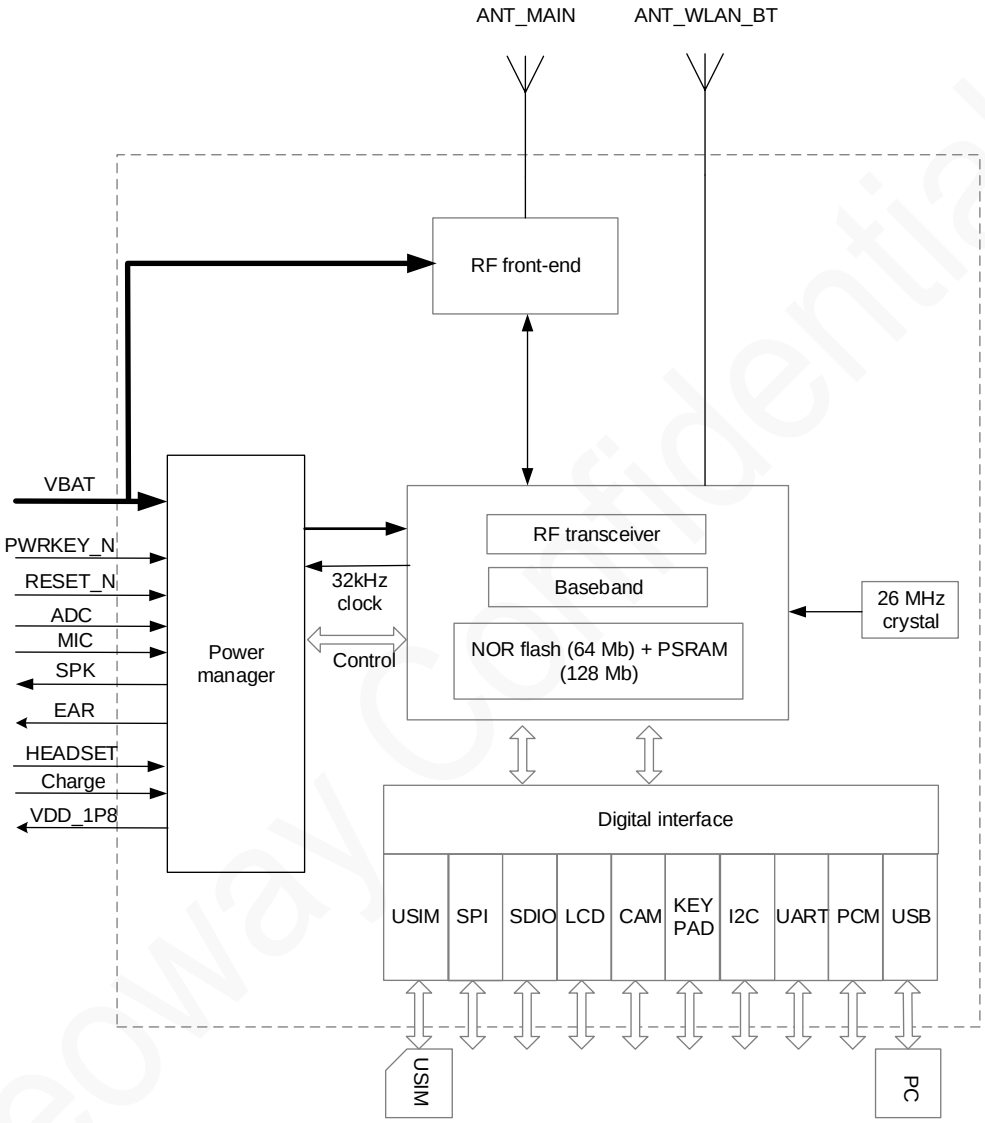
2.2 Block Diagram

N715-EA consists of the following functionality units:

- Baseband chip
- 26 MHz crystal
- Power management

- Radio frequency
- Digital interfaces (USIM, I2C, SPI, KEYPAD, UART, USB, SDIO, PCM, and LCD)
- Analog interfaces (ADC, MIC, ERA, SPK, HEADSET)

Figure 2-1 Block diagram



2.3 Basic Features

Parameter	Description
Physical features	• Dimensions: (23.80±0.1) mm × (22.80±0.1) mm × (2.5±0.15) mm • Package: 76-pin LCC + 72-pin LGA • Weight: TBD

Temperature ranges	• Operating: -30°C ~ +75°C • Extended: -40°C ~ +85°C • Storage: -40°C ~ +90°C
Operating voltage (DC)	VBAT: 3.4 V - 4.2 V, typical value: 3.6 V
Operating current (DC)	Sleep mode[1]: <3 mA
	Standby mode[2]: <15 mA
	Operating mode[3] (LTE mode): <610 mA
	Power-off mode[4]: <35 uA
Application processor	ARM Cortex-A5 processor, 500 MHz main frequency, 32 kB L1 cache.
Memory	RAM: 128 Mb ROM: 64 Mb
Band	See Table 2-1.
Wireless rate	GPRS: Max 85.6 kbps (DL)/Max 85.6 kbps (UL) FDD-LTE: Cat1, Max 10 Mbps (DL)/Max 5 Mbps (UL) TDD-LTE: Cat1, Max 8 Mbps (DL)/Max 2 Mbps (UL)
Transmit power	EGSM900: +33 dBm (Power Class 4) DCS1800: +30 dBm (Power Class 1) LTE: +23 dBm (Power Class 3)
Application interfaces	2G/4G antenna, BT/Wi-Fi antenna All of them have a characteristic impedance of 50 Ω.
	Three UART interfaces including UART1, UART2 and a debug UART interface Maximum baud rate supported: 961200 bps
	Two USIM interfaces, 1.8 V/3.0 V self-adaptive. Note: Using the USIM2 interface and the pins from 52 to 54 simultaneously are not allowed, that is, when connecting the USIM2 interface, you should keep these pins open.

Current in sleep mode[1] means the current drawn by the module in sleep mode, a low power consumption state, in which its RF function is functioning properly but its peripheral interfaces are disabled. If there is an incoming call or SMS, the module will exit from the sleep mode, and after the incoming call or voice instant messaging has ended, the module will re-enter the sleep mode.

Current in idle mode[2] means the current drawn by the module in a normal operating mode, but no data service is being processed.

Current in normal operation mode[3] means the current drawn by the module when there are on-going data services. In "operating mode", only the current value in LTE system is exemplified. For other current values in other network modes, please refer to the current test report.

Current in power-off mode[4]: when the module is in power-off mode, there is a voltage being applied at VBAT but the module does not run.

	One USB2.0 interface, slave mode only
	Three SPI interfaces One standard SPI interface supports only master mode One LCD-dedicated SPI interface One camera-dedicated SPI interface
	Four 12-bit ADC interfaces, can detect voltages ranging from 0 V to VBAT.
	Two SDIO interfaces SDIO2 for WLAN SDIO1 is used for SD card connection and needs to be multiplexed by a dedicated pin that supports multiplexing. For more details, see the pin multiplexing table.
	One PCM interface
	One I2C interface, master mode only
	One headset interface
	One MIC interface, bias voltage ranging from 2.2 V to 3 V, V_{norm}=2.2 V
	One SPK interface, supporting differential output only, with built-in class-AB or class-D power amplifier. Maximum output power: Class AB: 600 mW@4.2 V, with an 8 Ω load. Class D: 800 mW@4.2V, with an 8 Ω load.
	One EAR interface, for a maximum of 50 mV power when loading 32 Ω. If the output power is not enough, connect this interface to an external power amplifier.
	6x6 matrix keypad
AT commands	3GPP Release 13 Neoway extended commands
SMS	PDU, TXT
Data	PPP, RNDIS, ECM
Protocol	TCP, UDP, MQTT, FTP, HTTP/HTTPS, SSL, TLS
Certification approval	RoHS*, CE*

* means under development.

3 Reference Standards

N715-EA is designed by referring to the following standards:

- 3GPP TS 36.521-1 V13.0.0 User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance Testing
- 3GPP TS 21.111 V13.0.0 USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0 Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V13.0.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V13.0.0 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V13.0.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V13.0.0 Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- 3GPP TS 07.07 AT command set for GSM Mobile Equipment (ME)
- YD 1214-2006 Technical requirement of 900/1800MHz TDMA Digital Cellular Mobile Telecommunication Network General Packet Radio Service (GPRS)Equipment: Mobile Stations
- YD 1215-2006 Testing Methods of 900/1800MHz TDMA Digital Cellular Mobile Telecommunication Network General Packet Radio Service (GPRS)Equipment: Mobile Stations
- YD 1032-2000 Limits and Measurement Methods of Electromagnetic Compatibility for 900/1800MHz Digital Cellular Telecommunications System Part1: Mobile Station and Ancillary Equipment
- Ministry of Industry and Information Technology PRC, Measures for the Network Access Management of Telecommunication Equipment (2014 Amendment)
- GB4943.1-2011 Information technology equipment - Safety - Part 1: General requirements
- GB/T22450.1-2008 Limits and measurement methods of electromagnetic compatibility for 900/1800MHz TDMA digital cellular telecommunications system - Part 1: Mobile station and ancillary equipment
- CNCA-O7C-031:2007 Rules for Compulsory Certification of Telecommunication Equipment Telecommunication Terminal Equipment
- GSM/GPRS/EDGE 2G Communication Protocol

4 Module Pins

There are 148 pins on N715-EA and their pads are introduced in 76-pin LCC + 72-pin LGA package. It supports interfaces including power supply, USB, UART, USIM, PCM, ADC, I2C, and SDIO.

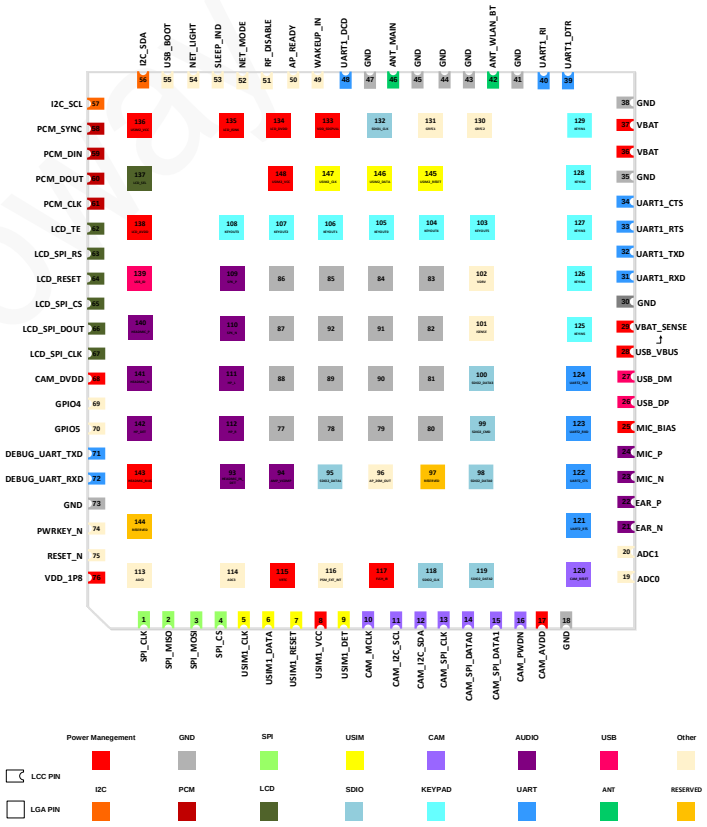
4.1 Pad Lay-out

The following figure shows the pad layout of N715-EA.

There are hardware conflicts between USIM2 interface (pins 145# to 147#) and status indication interface (pins 52# to pin 54#). if you use USIM2 interface, please be sure to leave the status indication interface open; if you use the status indication interface, leave the USIM2 interface open.

USIM2 is an optional signal, which is configured in the firmware. Therefore, please pay attention to the difference in firmware version. For more information about how to use the USIM2 interface, please contact Neoway FAEs.

Figure 4-1 N715-EA pad lay-out (top view)



4.2 Pin Descriptions

The following table lists the IO definitions and DC characteristics.

Table 4-1 IO definitions and DC characteristics

IO type			
B	Digital input/output, CMOS logic level		
DO	Digital output, CMOS logic level		
DI	Digital input, CMOS logic level		
PO	Power output		
PI	Power input		
AO	Analog output		
AI	Analog input		
AIO	Analog input/output		
Level feature			
Interface type	Power domain	Logic level	
USIM	P1: 1.8 V/3.0 V self-adaptive V_{DD_P1}: 1.62 V - 1.98 V (type: 1.8 V)/2.9 V - 3.3 V (type: 3 V)	1.8 V level feature: $V_{IH}=0.7V_{DD\_P1}$~V_{DD_P1} $V_{IL}=0V$~$0.3V_{DD\_P1}$ $V_{OH}=0.9V_{DD\_P1}$~V_{DD_P1} $V_{OL}=0V$~$0.1V_{DD\_P1}$	3.0 V level feature: $V_{IH}=0.7V_{DD\_P1}$~V_{DD_P1} $V_{IL}=0V$~$0.15V_{DD\_P1}$ $V_{OH}=0.9V_{DD\_P1}$~V_{DD_P1} $V_{OL}=0V$~$0.1V_{DD\_P1}$
SDIO1	P2: 1.8V/3.0V	1.8 V level feature:	3.0 V level feature:

	V_{DD_P2}: 1.62 V - 1.98 V (type: 1.8 V)/2.8 V - 3.3 V (type: 3 V)	V_{IH}=0.7V_{DD_P2}~V_{DD_P2} V_{IL}=0V~0.3V_{DD_P2} V_{OH}=0.9V_{DD_P2}~V_{DD_P2} V_{OL}=0V~0.1V_{DD_P2}	V_{IH}=0.7V_{DD_P2}~V_{DD_P2} V_{IL}=0V~0.3V_{DD_P2} V_{OH}=0.9V_{DD_P2}~V_{DD_P2} V_{OL}=0V~0.1V_{DD_P2}
GPIO	P3: 1.8 V V_{DD_P3}: 1.7 V - 1.9 V (type: 1.8 V)	V_{IH}=0.7V_{DD_P3}~V_{DD_P3} V_{IL}=0V~0.3V_{DD_P3} V_{OH}=0.8V_{DD_P3}~V_{DD_P3} V_{OL}=0V~0.2V_{DD_P3}	

Table 4-2 Pin descriptions

Signal	Pin	I/O type	Function description	DC feature/power domain	Remarks
Power interfaces					
VBAT	36, 37	PI	Main power supply of the module	V_{min}=3.4 V, V_{norm}=3.6 V, V_{max}=4.2 V	The external power supplies at least 2.5 A current to VBAT.
VBAT_SENSE	29	AI	VBAT voltage sampling pin		This pin must be connected to VBAT; otherwise, the module cannot start up.
VDD_1P8	76	PO	1.8 V power output	V_{norm} =1.8 V, I_{max} = 50 mA	Used only for voltage-level translation. Leave this pin open if unused.
GND	18, 30, 35, 38, 41, 43 - 45, 47, 73, 77 - 92				Ensure that all GND pins are grounded.
Control interfaces					
RESET_N	75	DI	Module Reset	V_{ILmax}=0.5 V	Active low; used to reset the module. This pin is connected to VBAT through

					a 20 kΩ pull-up resistor inside the module.
PWRKEY_N	74	DI	Module Power on/off	V_{ILmax}=0.5 V	Active low; used for module power-on/off. This pin is connected to VBAT through a 20 kΩ pull-up resistor inside the module.
WAKEUP_IN	49	DI	Module wakeup	P3	See 5.9.2 .
Status indication interfaces					
NET_MODE	52	DO	Registered network mode indication	P3	Note: If the USIM2 interface is not used, the pins from 52 to 54 can be used normally; otherwise, keep these pins open. If a status indication signal is required, it should be multiplexed from a dedicated pin by reference to the multiplexing signal table; for more information, contact Neoway.
SLEEP_IND	53	DO	Sleep mode indication	P3	
NET_LIGHT	54	DO	Network status indication	P3	
UART1 interface					
UART1_RXD	31	DI	UART data input	P3	FW in standard version: used for AT communications FW in open version: used for data transmission.
UART1_TXD	32	DO	UART data output	P3	
UART1_RTS	33	DO	UART ready to send	P3	
UART1_CTS	34	DI	UART clear to send	P3	
UART1_DTR	39	DI	UART data terminal ready	P3	
UART1_RI	40	DO	UART ring indicator	P3	
UART1_DCD	48	DO	Carrier detect output	P3	

UART2 interface					
UART2_RTS	121	DO	UART ready to send	P3	Used for data transmission. UART2_CTS (pin #122) can be used to capture CP-side log.
UART2_CTS	122	DI	UART clear to send	P3	
UART2_RXD	123	DI	UART data input	P3	
UART2_TXD	124	DO	Data transmitting	P3	
DEBUG UART					
DEBUG_UART_RXD	72	DI	DEBUG data receiving	P3	It is used for log capturing only. Leave this pin open if unused.
DEBUG_UART_TXD	71	DO	DEBUG data sending	P3	
USIM interfaces					
USIM1_VCC	8	PO	USIM1 power output	$I_{O\ max}$ = 50 mA	-
USIM1_DATA	6	B	USIM1 data input and output	P1	Connecting this pin to USIM1_VCC through a 4.7 kΩ pull-up resistor is required.
USIM1_CLK	5	DO	USIM1 clock output	P1	-
USIM1_RESET	7	DO	USIM1 reset	P1	-
USIM1_DET	9	DI	USIM1 plug detection	P3	-
USIM2_VCC	136, 148	PO	USIM2 power output	$I_{O\ max}$ = 50 mA	-
USIM2_RESET	145	DO	USIM2 reset	-	-
USIM2_DATA	146	B	USIM2 data input and output	P1	Connecting this pin to USIM2_VCC through a 4.7 kΩ pull-up resistor is required.
USIM2_CLK	147	DO	USIM2 clock output	P1	-

USB interfaces					
USB_VBUS	28	PI	USB insertion detection pin	4.5 V - 5.2 V, typical value: 5.0 V	-
USB_DM	27	AIO	USB data line -	-	USB 2.0. 90 nominal differential characteristic impedance. This pin is used for software download and data transmission.
USB_DP	26	AIO	USB data line +	-	
USB _ID*	139	DI	Master and slave device detection pins, reserved.	P3	–
ADC interfaces					
ADC0	19	AI	Universal ADC interface	Voltage range: 0 V - VBAT	Leave this pin open if unused.
ADC1	20	AI	Universal ADC interface		
ADC2	113	AI	Universal ADC interface		
ADC3	114	AI	Universal ADC interface		
I2C interface					
I2C_SDA	56	B	I2C data	P3	It should be pulled up to VDD_1P8 through a resistor (1.8 kΩ recommended).
I2C_SCL	57	DO	I2C clock	P3	
PCM interfaces					
PCM_SYNC	58	DI	PCM data frame sync	P3	Leave this pin open if unused.
PCM_DIN	59	DI	PCM data input	P3	Leave this pin open if unused.
PCM_DOUT	60	DO	PCM data output	P3	Leave this pin open if unused.
PCM_CLK	61	DO	PCM clock	P3	Leave this pin open if unused.

SDIO interfaces					
SDIO2_CMD	99	DO	SDIO2 command control	P3	Leave this pin open if unused.
SDIO2_CLK	118	DO	SDIO2 clock	P3	Leave this pin open if unused.
SDIO2_DATA0	98	B	SDIO2 data 0	P3	Leave this pin open if unused.
SDIO2_DATA1	95	B	SDIO2 data 1	P3	Leave this pin open if unused.
SDIO2_DATA2	119	B	SDIO2 data 2	P3	Leave this pin open if unused.
SDIO2_DATA3	100	B	SDIO2 data 3	P3	Leave this pin open if unused.
SDIO1_CLK	132	DO	SDIO1 clock	P2	Leave this pin open if unused.
VDD_SDCPULL	133	PO	SD card IO power supply	P2	Pull-up power supply for the SDIO signal; it cannot furnish power for the SD card interface. Leave this pin open if unused.
SPI interfaces					
SPI_CLK	1	DO	Clock signal	P3	Supporting only master mode. Leave this pin open if unused.
SPI_MISO	2	DI	Output of the slave device and input of the master device	P3	
SPI_MOSI	3	DO	Input of the slave device and output of the master device	P3	
SPI_CS_N	4	DO	Chip select signal of the slave device	P3	
LCD interfaces					
LCD_TE	62	DI	LCD frame synchronization	P3	Leave this pin open if unused.
LCD_SPI_RS	63	DO	LCD register selection	P3	Leave this pin open if unused.

LCD_RESET	64	DO	LCD reset	P3	Leave this pin open if unused.
LCD_SPI_CS	65	DO	LCD chip select	P3	Leave this pin open if unused.
LCD_SPI_DOUT	66	B	LCD data	P3	Leave this pin open if unused.
LCD_SPI_CLK	67	DO	LCD clock	P3	Leave this pin open if unused.
LCD_ISINK	135	PI	Sink current input pin, used to adjust backlight brightness.	Imax = 200 mA The current value is configurable.	LCD_ISINK is connected to the cathode of backlight and its brightness is adjusted by sinking a current to the pin.
LCD_SEL	137	DO	Reserved	-	-
LCD_DVDD	134	PO	LCD digital power	V_{nom} = 1.8 V	Leave this pin open if unused.
LCD_AVDD	138	PO	LCD analog power	V_{nom} = 3.0 V	Leave this pin open if unused.
Camera interfaces					
CAM_MCLK	10	DO	Camera main clock	P3	Leave this pin open if unused.
CAM_I2C_SCL	11	DO	Camera I2C clock	P3	It should be pulled up externally when used. Leave this pin open if unused.
CAM_I2C_SDA	12	B	Camera I2C data	P3	
CAM_SPI_CLK	13	DO	Camera SPI clock	P3	Leave this pin open if unused.
CAM_SPI_DATA0	14	B	Camera SPI data 0	P3	Leave this pin open if unused.
CAM_SPI_DATA1	15	B	Camera SPI data 1	P3	Leave this pin open if unused.
CAM_PWDN	16	DO	Camera power down	P3	Leave this pin open if unused.
CAM_RESET	120	DO	Camera reset	P3	Leave this pin open if unused.
CAM_AVDD	17	PO	Camera analog power	V_{nom} = 2.8 V	Disabled by default and after enabled, it outputs a 2.8 V voltage.
CAM_DVDD	68	PO	Camera digital power supply	V_{nom} = 1.8 V	Disabled by default and after enabled,

					it outputs a 1.8 V voltage.
Flashlight driver interface					
FLSH_IB	117	PI	Flashlight current sink	I_{max} = 240 mA The current value is configurable.	Connect this pin to the cathode of the diode when used. Leave this pin open if unused.
RF control interfaces					
GRFC1*	131	DO	General RF Control	P3	-
GRFC2*	130	DO	General RF Control	P3	-
Analog audio interfaces					
EAR_N	21	AO	Earpiece output -	-	50 mW maximum output power with a 32 Ω load. If the output power is not enough, connect this interface to an external power amplifier.
EAR_P	22	AO	Earpiece output +	-	
SPK_P	109	AO	Speaker output +	-	Support differential output only, with built-in class-AB or class-D power amplifier. Peak output power: Class AB: 600 mW@4.2V, with an 8 Ω load Class D: 800 mW@4.2V, with an 8 Ω load.
SPK_N	110	AO	Speaker output -	-	
MIC_N	23	AI	MIC input channel -	-	-
MIC_P	24	AI	MIC input channel +	-	-
MIC_BIAS	25	PO	Microphone bias power supply	V_O=2.2 V - 3 V, V_{norm}=2.2 V	-

AMP_VCOMP	94	-	Headset-dedicated ground	-	Route traces between the left and right sound channels of the headset, connect to the GND of the headset connector, and then the main ground.
HP_L	111	AO	Headset left channel	-	-
HP_P	112	AO	Headset right channel	-	-
HEADMIC_P	140	AI	Module-side differential input +	-	-
HEADMIC_N	141	AI	Module-side differential input -	-	-
HEADMIC_BIAS	143	PO	MIC bias power supply	V_O=2.2 V - 3 V, V_{norm}=2.6 V	-
HP_DET	142	DI	Headphone plug detect	-	-
HEADMIC_IN_DET	93	DI	headset single-ended input channel and insertion detection	-	-
GPIO interfaces					
GPIO4	69	B	General Purpose Input Output	P3	-
GPIO5	70	B	General Purpose Input Output	P3	-
Matrix keypad interfaces					
USB_BOOT	55	DI	Key 0 of inputting	P3	After the module is started, the key is used for KEYIN0.
KEYIN1	129	DI	Key 1 of inputting	P3	Leave this pin open if unused.
KEYIN2	128	DI	Key 2 of inputting	P3	Leave this pin open if unused.
KEYIN3	127	DI	Key 3 of inputting	P3	Leave this pin open if unused.
KEYIN4	126	DI	Key 4 of inputting	P3	Leave this pin open if unused.
KEYIN5	125	DI	Key 5 of inputting	P3	Leave this pin open if unused.

KEYOUT0	105	DO	Key 0 of outputting	P3	Leave this pin open if unused.
KEYOUT1	106	DO	Key 1 of outputting	P3	Leave this pin open if unused.
KEYOUT2	107	DO	Key 2 of outputting	P3	Leave this pin open if unused.
KEYOUT3	108	DO	Key 3 of outputting	P3	Leave this pin open if unused.
KEYOUT4	104	DO	Key 4 of outputting	P3	Leave this pin open if unused.
KEYOUT5	103	DO	Key 5 of outputting	P3	Leave this pin open if unused.
Antenna interface					
ANT_WLAN_BT	42	AIO	Shared antenna interface of Bluetooth and Wi-Fi scan	-	50 nominal characteristic impedance.
ANT_MAIN	46	AIO	Main antenna interface	-	50 nominal characteristic impedance.
Other interfaces					
USB_BOOT	55	DI	Force the module into emergency download mode	P3	Pulling up this pin to 1.8 V through a 10 resistor can force the module to boot from USB port for firmware upgrade. If unused, Leave this pin open.
AP_READY	50	DO	Sleep status detection for application processor	P3	-
RF_DISABLE	51	DI	Flight mode control	P3	-
AP_26M_OUT*	96	DO	Reserved 26 MHz clock output	-	-
VRTC*	115	PI	Real Time Clock Power supply	V_{nom} = 3 V, V= 2.8 V - 3.2 V	-
PSM_EXT_INT*	116	DI	Interrupt pin for PSM wakeup Setting this pin high externally	VRTC power domain	Active high Leave this pin open if unused.

			can wake up the module from PSM.		
ISENSE	101	AI	Charging current detection	-	-
VDRV	102	AO	Charging control	-	Used to drive the MOS transistor of the external charging circuit, so as to adjust the charging current.
RESERVED	97, 144	-	-	-	Used for function extension or the function not open to users. These RESERVE pins might have different functions. Leave these pins open.

5 Application Interfaces

N715-EA provides power, control, communication, peripherals, audio, video, and RF interfaces to meet the functional requirements of customers in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

5.1 Power Interfaces

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin	I/O	Function description	Remarks
VBAT	36, 37	PI	Power input of the module	3.4 V - 4.2 V, type: 3.6 V
VBAT_SENSE	29	AI	VBAT voltage sampling pin	The pin must be connected to VBAT; otherwise, the module cannot start up.
VDD_1P8	76	PO	1.8 V power output	V_{norm} =1.8 V, I_{max} = 50 mA
GND	18, 30, 35, 38, 41, 43 - 45, 47, 73, 77 - 92			All the GND pins are intended to be connected to ground.

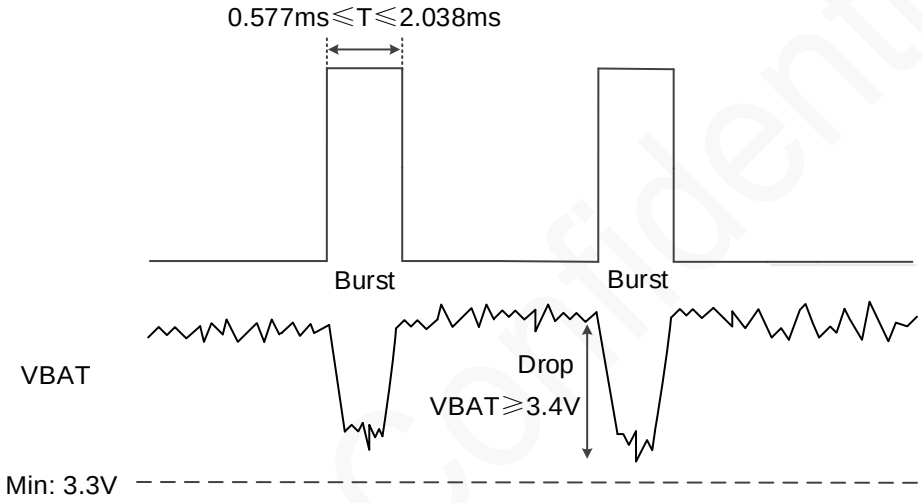
5.1.1 VBAT

The power supply design covers two parts: schematic design and PCB layout.

Schematic Design

In GSM/GPRS mode, RF data is transmitted in burst mode that generates voltage drops on the power supply. Furthermore, this results in a 217 Hz TDD noise through the power and the transient peak current is 2.5 A. Therefore, it is necessary to ensure that the drive capacity of the power supply is sufficient, the power supply trace is wide enough to reduce impedance and there are large-capacity capacitors to improve the freewheeling capability to ensure that the voltage will not drop below the minimum operating voltage of the module when the instantaneous current reaches its peak.

Figure 5-1 Voltage drops of the power supply.



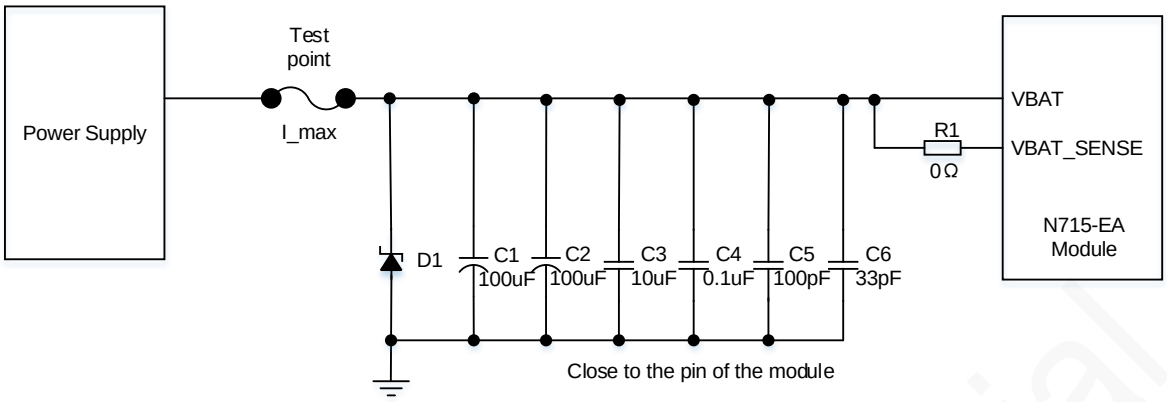
Never use a diode to make the drop voltage between a higher input and the module power supply. The forward voltage drop V_f of the diode has two characteristics: one is that it increases with the increase of forward current; the other is that it increases significantly at a low temperature. If there is an instantaneous high current, the instantaneous increase of forward voltage drop will lead to unstable operating voltage of the module, or even damage the module.

The power supply design of the N715-EA module is determined by the power input voltage. The designs are classified by power input voltage as follows:

- Supports the 3.4 V - 4.2 V power input (typical value: 3.6 V, supplied by a battery)
- Supports the 4.2 V - 5.5 V power input (typical value: 5.0 V, supplied by a computer through its internal rectifier.)
- Supports the 5.5 V - 24 V power input (typical value: 12 V, using a DC-DC power supply solution.)

The recommended 3.4 V to 4.2 V input design is as follows:

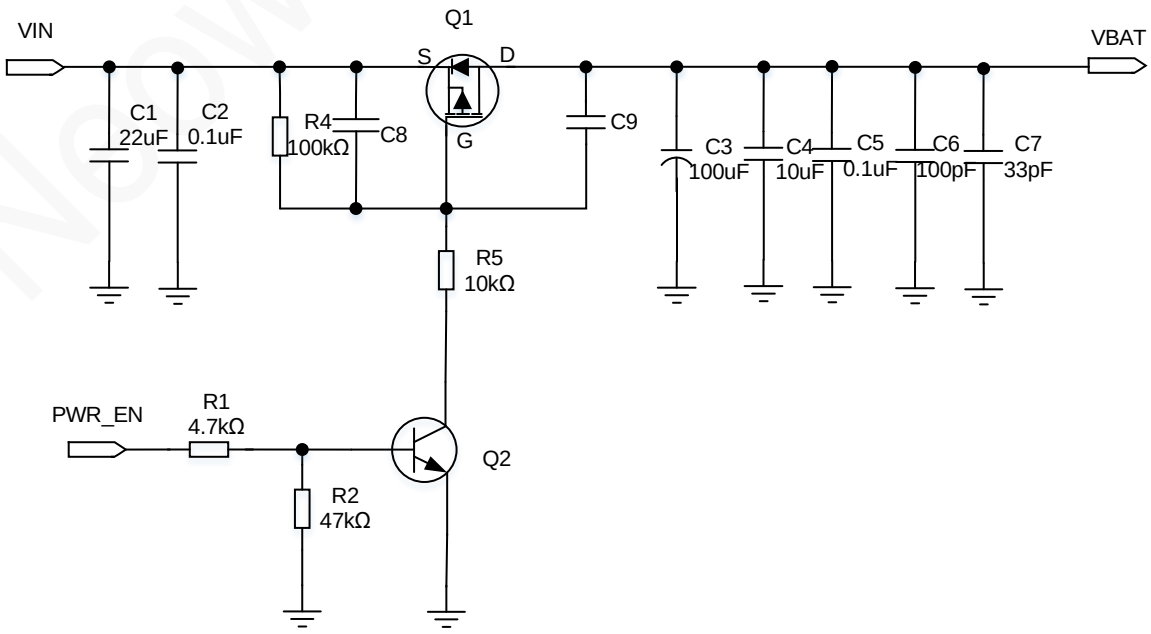
Figure 5-2 Recommended design 1



- The maximum input voltage for the module is 4.2 V and the typical value is 3.6 V.
- The reverse voltage across D1 (a TVS diode) should be 4.5 V (V_{RWM}=4.5V) and the peak power (Ppp) should be 2800 W (tp=8/20uS). Keep the placement of the TVS diode close to the power input interface to suppress the surge voltage before it enters back-end circuits to prevent the back-end component and the module from damaging.
- To decrease voltage drops during bursts, a large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 and C2. Its maximum safe operating voltage should be larger than 2 times the voltage across the power supply.
- To get a stable power source, place a bypass capacitor (C3, C4, C5, and C6) of low-ESR close to the VBTA pins to filter out high-frequency jamming.

The following circuit design is recommended to control the power supply.

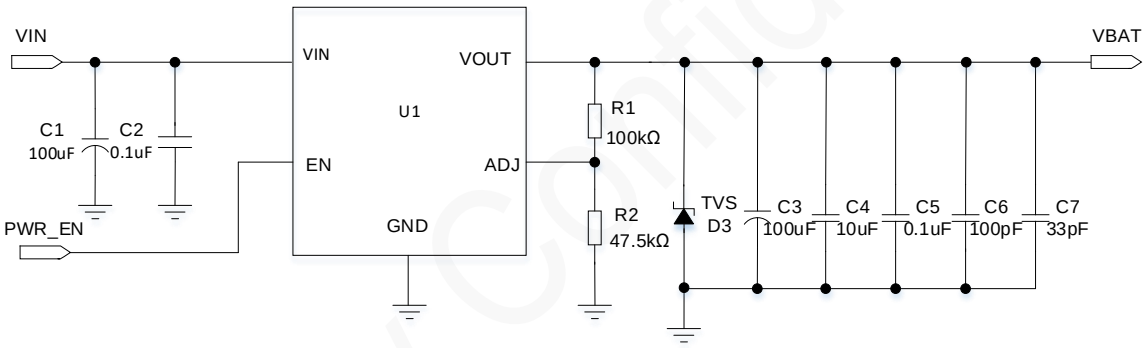
Figure 5-3 Recommended design 2



- Select an enhanced p-MOSFET at Q1, of which the safe operating voltage is at least 12 V (V_{dss}=-12 V) and drain current is at least 3.5 A ($I_{D(MAX)}$=-3.5 A) and Rds is low ($R_{ds(on)}$ =108 mΩ).
- Select a common NPN tripolar transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which operating voltage of the tripolar transistor might increase in low temperature; it is recommended that the value of R2 be at least 10 times that of R1.
- Keep the placement of C3 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C3 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Place the bypass capacitors (C4, C5, C6, C7) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

Recommended 4.2 V to 5.5 V input design:

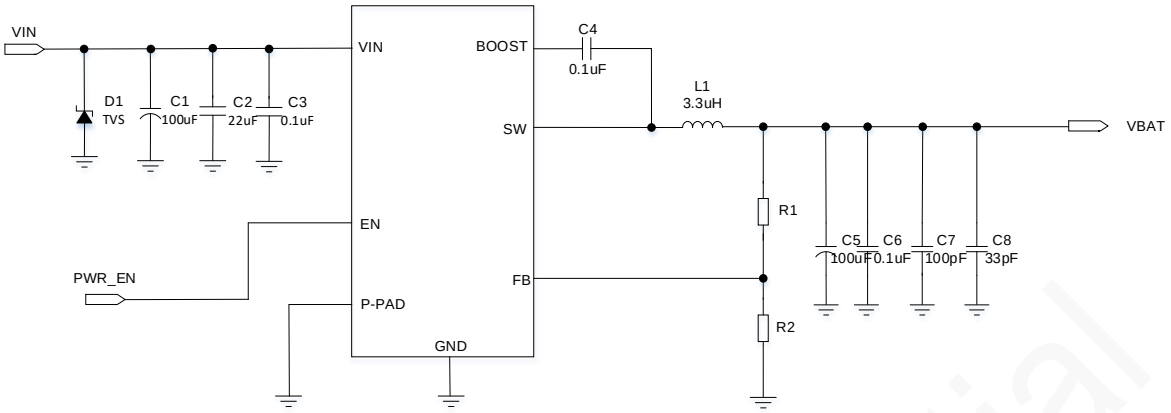
Figure 5-4 Recommended design 3



- Design with LDO is simpler and more efficient when the system power input is close to the permissible voltage across VBAT.
- Select an LDO that can output 3 A current at U1 to ensure the performance of the module.
- In order to protect the back-end components and the module, place the TVS diode close to the power input interface to suppress the surge voltage before it enters back-end circuits
- Keep the placement of C3 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C3 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Keep the placement of the bypass capacitors (C4, C5, C6, C7) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

Recommended 5.5 V to 24 V input design:

Figure 5-5 Recommended design 4



- When there is a big difference between the system power input and VBAT, it is recommended to select the DC-DC step-down chip, and its maximum output current should be at least 3 A.
- In order to protect the back-end components and the module, place the TVS (D1) close to the power input interface to suppress the surge voltage before it enters back-end circuits.
- Keep the placement of C5 close to the module. A large tantalum electrolytic capacitor (220 μF or 100 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) can be selected at C5 to improve the instantaneous large current freewheeling ability of the power supply. Its withstand voltage should be larger than 2 times the voltage of the power supply.
- Keep the bypass capacitors (C6, C7, C8) of low-ESR close to the module to filter out high-frequency jamming from the power supply.

When the module fails to shut down normally due to abnormality, it is recommended to cut off the power first to shut down the module, and then power up again to restart the module.

PCB Layout

An ESR capacitor must be placed at the output end of the power supply to suppress the peak current. In order to protect back-end devices, a TVS diode should be placed at the power input end to suppress voltage spikes. The circuit design is important, and the device layout and routing are equally important. Several key points in power supply design are summarized below:

- The TVS diode can absorb instantaneous high-power pulses and withstand instantaneous pulse current peaks up to tens or even hundreds of amperes. The clamp response time is extremely short. Keep the TVS diode as close as possible to the power input to ensure that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB wires.
- The bypass capacitor must be placed close to the power supply pin of the module to filter out high-frequency noise signals in the power supply.

- For the main power circuit of the module, the PCB routing width must ensure that the 2.5 A current can be passed safely, and there should be no obvious loop voltage drop. Keep the PCB trace width be at least 2.5 mm and ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make the power cable short and thick.
- Noise-sensitive circuits, such as audio circuits and RF circuits, should be kept away from power circuits, especially when the DC-DC power supply is used.
- The voltage frequency of the SW pin of the DC-DC power supply is high, and the loop should be minimized. Keep sensitive components far away from the SW pin of the DC-DC component to prevent noise coupling. Place feedback components as close as possible to the FB pin.
- The GND pin and bottom pad of the chip must be grounded to ensure good heat dissipation and noise isolation.

5.1.2 VDD_1P8

VDD_1P8 power is on normally and cannot be turned off even when the module is in sleep mode. Connecting the module to an external circuit will increase its power consumption in sleep module. It is recommended that VDD_1P8 is used for voltage-level translation only and an ESD protector should be added.

N715-EA provides one VDD_1P8 output. It can provide the 1.8 V voltage and the maximum output current is 50 mA.

5.2 Control Interfaces

Signal	Pin	I/O	Function description	Remarks
PWRKEY_N	74	DI	ON/OFF button	Active low
RESET_N	75	DI	Module reset input	Active low

5.2.1 Power-on

Table 5-1 Module power-on descriptions

Power-on trigger method	Is it supported?	Power-off method	Cautions
Button	Supported	A long press of the power button for over 2s can switch off the module.	When the module is in power-on mode, do not directly disconnect the power supply of the module; otherwise, the flash memory (Flash) inside the module may be damaged.
Pulse	Supported	Forcing a low pulse	

		(controlled by MCU) at the PWRKEY_N pin for not less than 2s can switch off the module.	
Automatic power-on (Ground PWRKEY_N directly)	Supported	Execute the shutdown AT command first and then power down the module.	If you design an automatic power-on circuit by reference to Figure 5-9, you should add a RESET circuit by reference to Figure 5-12, since when the auto power-on solution is used and after the module is powered off it may encounter a startup failure.
Power-on triggered by USB_VBUS	Supported	Unplug the USB, execute a dedicated AT command, and then power down the module.	When using AT commands to switch off the module, if the system is not powered down and the USB is still connected, the module may start again after power-down.

Power-on controlled by PWRKEY_N

The following show two recommended reference designs of power-on controlled:

Figure 5-6 Reference design of power-on controlled by a button

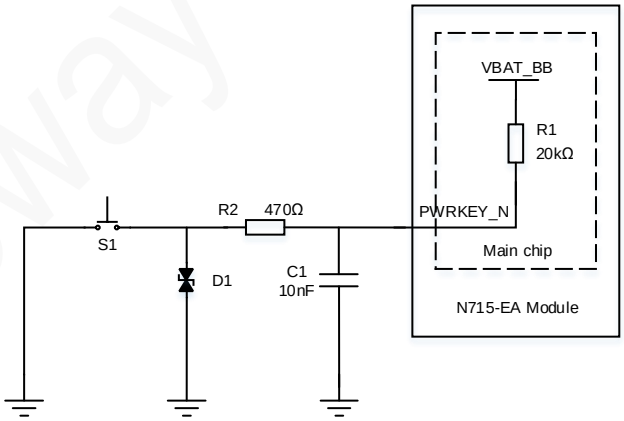
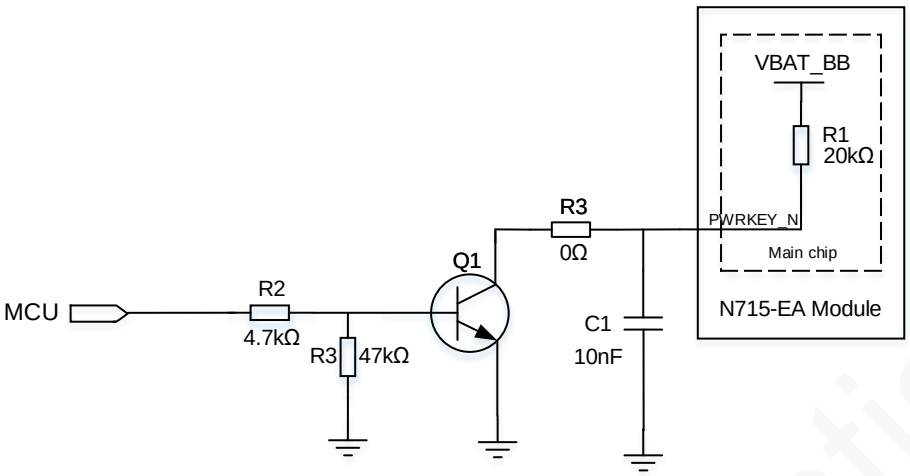


Figure 5-7 Reference design of power-on controlled by an MCU

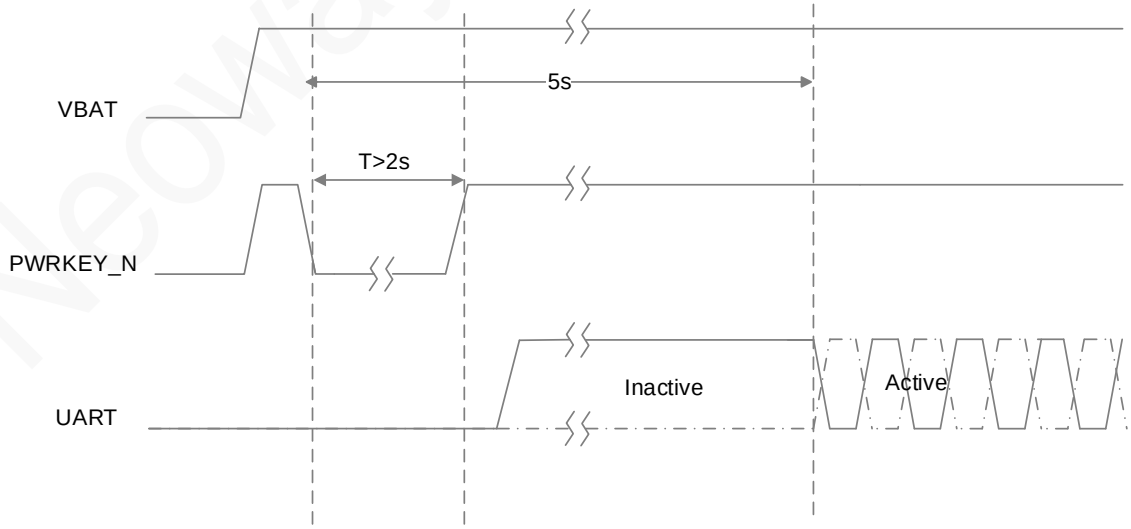


- Power-on process

To switch the module on, you can first apply a voltage at the VBAT module supply input and then force a low pulse for greater than 2s at PWRKEY_N. The AT function is available after 5 seconds. Do NOT connect an external resistor with large resistance in series to the PWRKEY_N pin (a 470 Ω resistor is recommended) since there is already an internal 1 kΩ series resistor. Otherwise, the module cannot be switched on since the PWRKEY_N is at a high level all the time.

After the module is switched on, it needs to perform initialization process untill the pin state is stable, and during the process, do not perform other operations on the module. The following figure shows the power-on process:

Figure 5-8 Power-on process

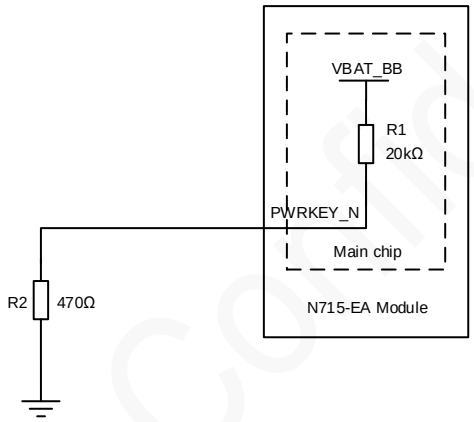


Automatic power-on once powered-up

If you design an automatic power-on circuit but power-off of the module is not required, you can directly pull down PWRKEY_N to ground. The recommended pull-down resistance is 470 Ω.

If you design an automatic power-on circuit and power-off of the module is required, you should add a reset circuit, since when the automatic power-on solution is used and after the module is powered off, the module may encounter a power-on failure. To ensure a proper power-on/off operation, reset the module at least one time after power-on. For the reset circuit, see Figure 5-12.

Figure 5-9 Reference design of automatic power-on once powered-up



5.2.2 Power-off

When the module is power-on mode, do not directly disconnect the power supply of the module; otherwise, the flash memory (Flash) inside the module may be damaged. It is recommended that before disconnecting the power supply, you should switch off the module through PWRKEY_N or a dedicated AT command.

After the module is switched off using the dedicated AT command, ensure that PWRKEY_N is at a high level; otherwise, the module will switch on again after power-off.

Two methods are available to power off the module: hard power-off and soft power-off.

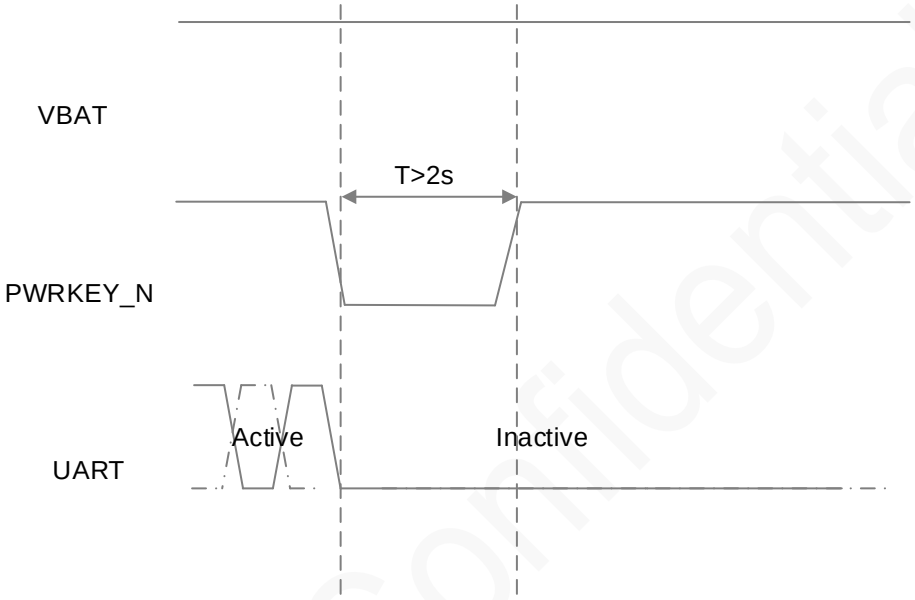
- Hard power-off: power-off controlled by PWRKEY_N
- Soft power-off: power-off by AT command

Power-off controlled by PWRKEY_N

Pulling down the PWRKEY_N input pin, which is normally set high by an internal pull-up, for at least 2s, can switch off the module.

The following figure shows the hardware power-off process:

Figure 5-10 Hard power-off process



Power-off controlled by AT command

When the module is in power-on mode, it can be switched off after a dedicated AT command is executed. For details, see *Neoway_N715-EA_AT_Commands_Manual*.

5.2.3 Reset

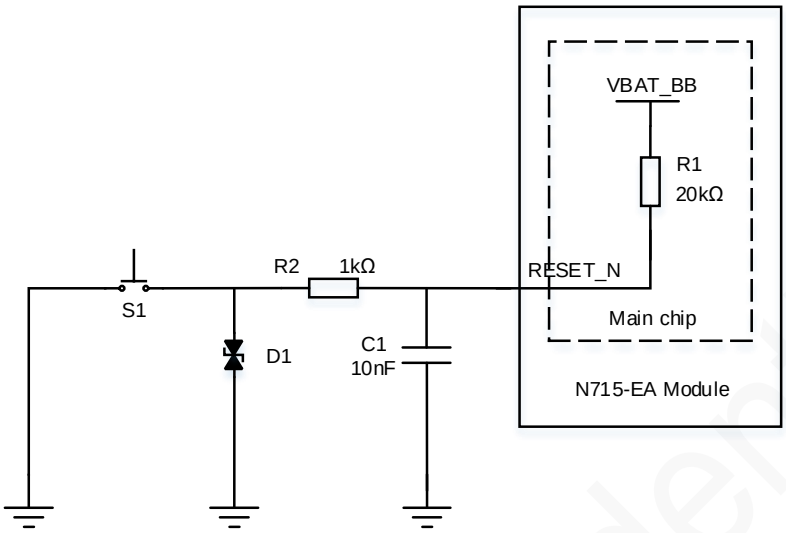
When the module encounters an exception (crash, etc.), you can reset the system through the RESET_N pin to ensure the normal operation of the module. Therefore, it is recommended to add a reset control circuit during circuit design, and the recommended reference circuit is shown in Figure 5-11 and Figure 5-12.

RESET_N is used to reset the module. When the module is in power-on mode, forcing a low pulse at RESET_N for more than 50 ms can reset the module. Figure 5-13 shows the reset process.

The following show two recommended reference reset designs of N715-EA:

- Resetting the module by using a button

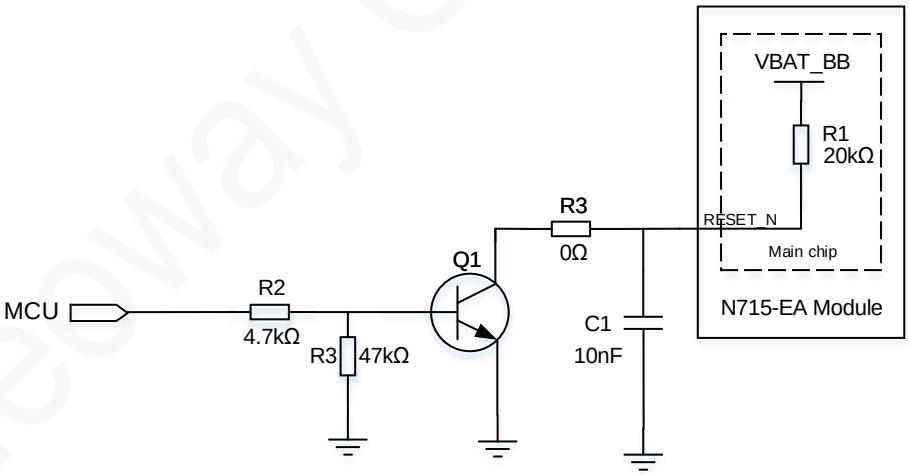
Figure 5-11 Reference design for reset by using a button



- Resetting the module by controlling an MCU

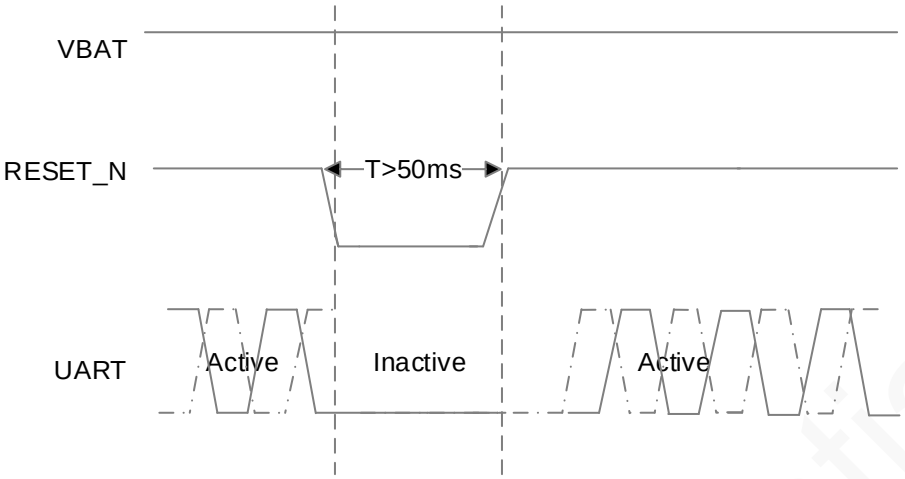
  If you use a 1.8 V/2.8 V/3.0 V MCU system, it is recommended to add a triode to separate it. Refer to the following designs.

Figure 5-12 Reference design for reset controlled by an MCU



The following figure shows the reset process of the N715-EA module:

Figure 5-13 Reset process of the N715-EA module



5.3 Peripheral Interfaces

N715-EA provides various peripheral interfaces.

In all reference designs of this section, the receiving and sending directions included in the pin names of the peripheral interface of the module are based on the module, whereas peripheral pins are named based on the components. For example, UART_TXD indicates the pin used by the module to send data, and MCU_RXD indicates the pin used by the MCU to receive data. These two pins should be connected.

Please note the signal naming of pins on the components in peripheral selection and design.

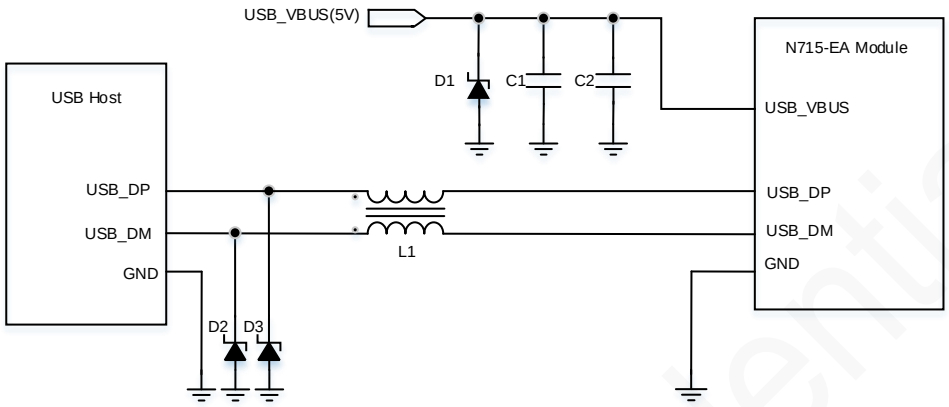
5.3.1 USB

Signal	Pin	I/O	Function description	Remarks
USB_VBUS	28	PI	USB insertion detection pin	4.5 V < USB_VBUS < 5.2 V typical value: 5 V
USB_DM	27	AIO	USB data negative signal	USB 2.0. 90 nominal differential characteristic impedance. This pin is used for software download and data transmission.
USB_DP	26	AIO	USB data positive signal	
USB_ID	139	DI	Reserved	-

N715-EA can implement program download, data communications, and debugging through the USB interface. The USB of N706 only supports slave mode. Figure 5-14 shows the recommended USB interface circuit.

The reverse current may flow from the USB powering device to the VBAT circuit (around 2.5 V) when VBAT is powered down. To prevent the reverse current from affecting the total circuit design, it is recommended that you add a power switch for the USB_VBUS power.

Figure 5-14 Recommended design of the USB interface



Schematic Design Guidelines

- Connect a 1 μF (C1) and a 33 pF (C2) filter capacitor in parallel to the USB_VBUS pin. An ESD component must be added for the power cable.
- The junction capacitance of the ESD components D2 and D3 on the USB_DP and USB_DM cables must be smaller than 0.5 pF.
- To improve EMI interference generated by USB signals, connect a common-mode inductor L1 to the USB_DP and USB_DM cables in series.

PCB Design Guidelines

- Place the filter capacitor on the USB_VBUS as close to the module pins as possible and place the ESD component as close to the USB connector as possible.
- Place the ESD component on the USB_DP and USB_DM cables as close to the USB connector as possible.
- It is important to route the USB signal traces as differential pairs. The impedance of USB differential trace is 90 Ω. The cable from the USB host to the module must be isolated from other signal cables with ground surrounded.

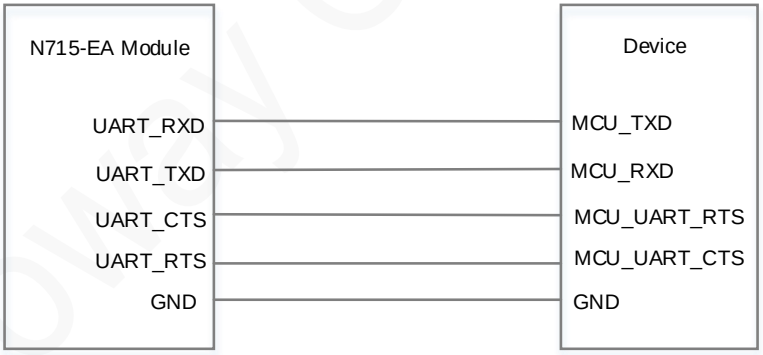
5.3.2 UART

Signal	Pin	I/O	Function description	Remarks
UART1_RXD	31	DO	UART data input	FW in standard version: used for AT
UART1_TXD	32	DI	UART data output	

UART1_RTS	33	DO	UART ready to send	communications FW in open version: used for data transmission.
UART1_CTS	34	DI	UART clear to send	
UART1_DTR	39	DO	UART data terminal ready	
UART1_RI	40	DI	UART ring indicator	
UART1_DCD	48	DI	Carrier detect output	
UART2_RTS	121	DO	UART ready to send	Used for data transmission
UART2_CTS	122	DI	UART clear to send	
UART2_RXD	123	DI	UART data input	
UART2_TXD	124	DO	UART data output	
DEBUG_UART_RXD	72	DI	DEBUG data input	Use for module debugging
DEBUG_UART_TXD	71	DO	DEBUG data output	

N715-EA provides three UART interfaces, two of which support hardware flow control. They support 1.8 V level and baud rates up to 921600 bps. The following figure shows recommended design of UART interface.

Figure 5-15 Reference design of UART interface



Schematic Design Guidelines

- Pay attention to the corresponding relations between the signal direction and the connection.
- It is prohibited to use diodes for voltage-level translation.

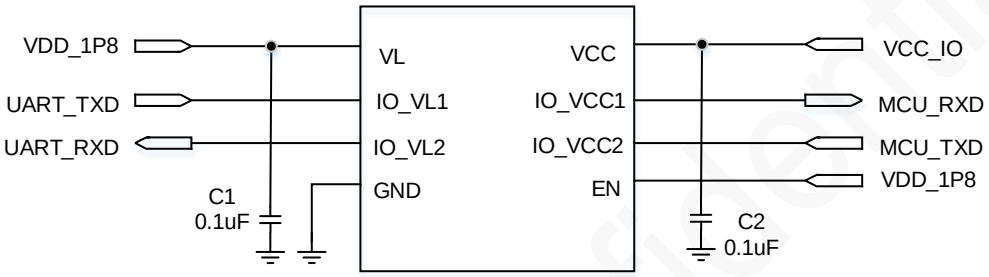
If the UART does not match the logic voltage of the MCU, add a voltage-level translation circuit outside of the module. Three transistor translation circuits are recommended based on the differences in logic levels and rates.

Do Not directly apply the parameter values of the components provided by the circuit to your circuit design; they need to be adjusted according to the actual situations. Note the difference between different voltage-level translation circuits .

- Voltage-Level Translation Circuit (Translator Chip)

  If the UART baud rate is greater than 115200 bps, it is recommended to refer to the recommended voltage-level translation circuit 1. See Figure 5-16.

Figure 5-16 Recommended voltage-level translation circuit1

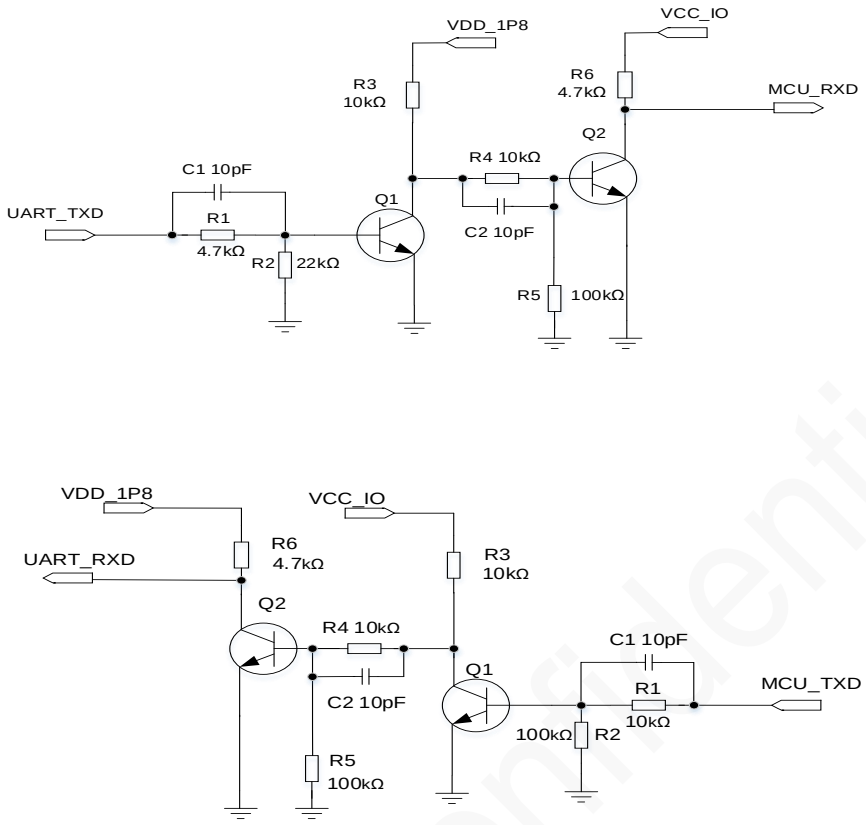


  - VL is the reference voltage of IO_VL1 and IO_VL2, ranging from 1. 5 V to 5.5 V.
  - VCC is the reference voltage of IO_VCC1 and IO_VCC2, ranging from 1. 5 V to 5.5 V.
  - EN is the enable pin, which works at a voltage of greater than VL-0.2 V. In the above circuit, the EN pin is connected to VDD_1P8 and the translator chip is always working.

- Dual-triode Voltage-Level Translator Circuit

  If the serial port baud rate is less than or equal to 115200 bps, design the serial port TXD and RXD by referring to recommended voltage-level translation circuit 2. As shown in Figure 5-17.

Figure 5-17 Recommended voltage-level translation circuit 2



MCU_TXD and MCU_RXD are the data output and input ports of the MCU respectively, and UART_TXD and UART_RXD are the data output and data input ports of the module respectively. VCC_IO is the IO voltage of the MCU. VDD_1P8 is the IO voltage of the module.

The circuit translates the voltage-level through the turn-on and turn-off of the triode, and dual triode can achieve higher pressure difference after voltage-level translation.

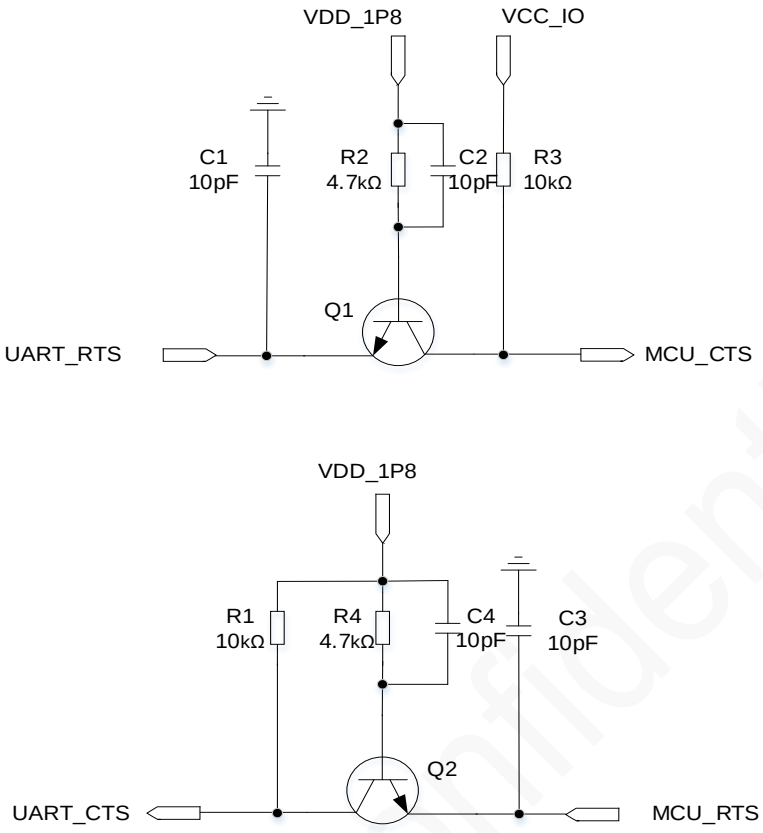
Schematic Design Guidelines

- Ensure that the base voltage of the triode is operating within the temperature range and the transistor can be fully turned on.
- It is recommended to reserve the acceleration capacitor, which can adjust the delay of the level conversion circuit in some cases.

- Single-triode Voltage-Level Translation Circuit

  Design the serial port pins CTS/RTS/DCD/RI by reference to recommended voltage-level translation circuit 3, as shown in Figure 5-18.

Figure 5-18 Recommended voltage-level translation circuit 3



MCU_CTS and MCU_RTS are the MCU-side signals; UART_CTS and UART_RTS are the module-side signals. VCC_IO is the IO voltage of the MCU. VDD_1P8 is the IO voltage of the module.

The circuit translates the voltage-level through the turn-on and turn-off of the triode, and the translation is unidirectional. Pay attention to the signal flow.

Schematic Design Guidelines

- Ensure that the voltage difference between the high-level and low-level sides is not greater than 2 V.
- For the accelerating capacitor, adjust it according to the actual test conditions; it is recommended to reserve the capacitor.
- The base voltage of the transistor is the lower voltage between both sides.

5.3.3 USIM

Signal	Pin	I/O	Function description	Remarks
USIM1_VCC	8	PO	USIM1 power output	1.8 V/3.0 V (self-adaptive)
USIM1_DATA	6	B	USIM1 data input and output	Connecting this pin to USIM1_VCC through a 4.7

				kΩ pull-up resistor is required.
USIM1_CLK	5	DO	USIM1 clock output	-
USIM1_RESET	7	DO	USIM1 reset	-
USIM1_DET	9	DI	USIM1 card plug detection	1.8 V power domain If unused, connect this pin to VDD_1P8 through a 47 kΩ resistor.
USIM2_VCC	136, 148	PO	USIM2 power output	1.8 V/3.0 V (self-adaptive)
USIM2_RESET	145	DO	USIM2 reset	-
USIM2_DATA	146	B	USIM2 data input and output	Connect this pin to USIM2_VCC through a 4.7 kΩ pull-up resistor.
USIM2_CLK	147	DO	USIM2 clock output	-

N715-EA provides 2 USIM card interfaces, self-adaptable to 1.8 V/3.0 V USIM cards, of which the USIM1 interface supports the hot-swap function. USIM1 is the default USIM interface. Figure 5-20 shows the reference design of the USIM card interface.

There are hardware conflicts between USIM2 interface (pins 145# to 147#) and status indication interface (pins 52# to pin 54#). if you use USIM2 interface, please be sure to leave the status indication interface open; if you use the status indication interface, leave the USIM2 interface open.

USIM2 is an optional signal, which is configured in the firmware. Therefore, pay attention to the difference in firmware version. For more information about how to use the USIM2 interface, please contact Neoway FAEs.

Figure 5-19 Reference design of the USIM card interface (normally closed type)

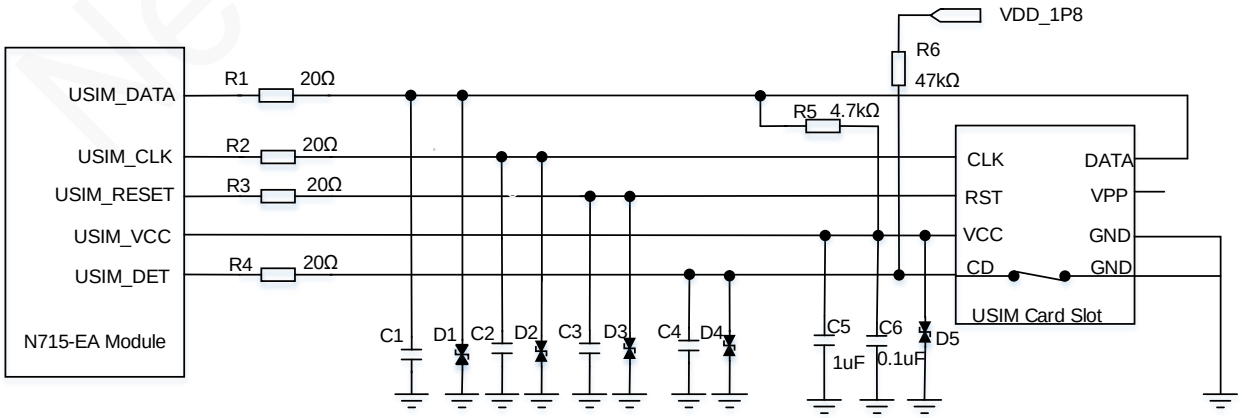
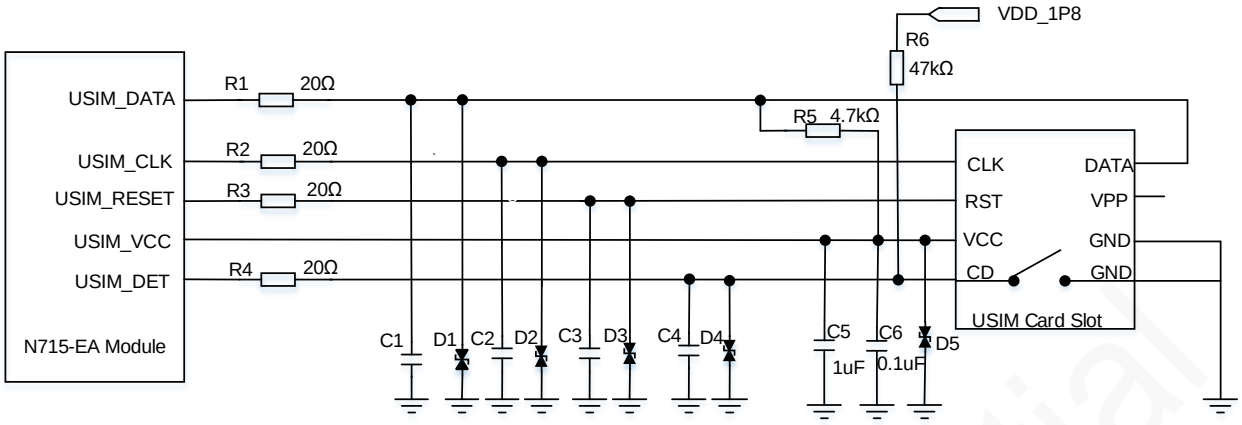


Figure 5-20 Reference design of the USIM card interface (normally open type)

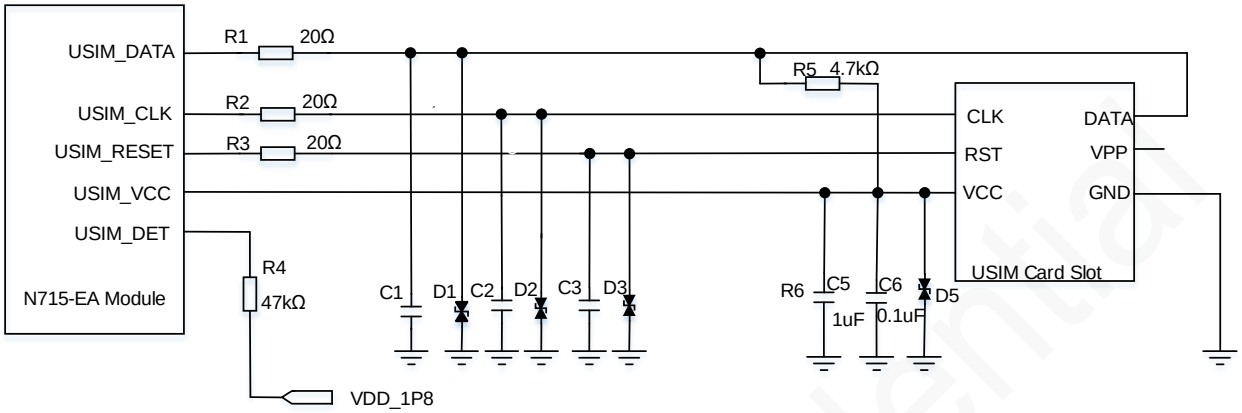


Schematic Design Guidelines

- USIM_VCC is the pin to supply power for USIM card and its maximum load is 50 mA. It is only used as power supply for USIM card (forbidden to supply power to other loads).
- Connect the USIM_DATA pin to USIM_VCC through a 4.7 kΩ resistor since there is no pull-up inside USIM_DATA.
- USIM_CLK is the clock signal pin of the USIM card. In applications with complex electromagnetic environments that have high requirements for ESD protection, it is recommended to add ESD protection diodes (junction capacitance ≤ 7pF) on each signal cable or add an integrated ESD component.
- Connect a resistor (not greater than 20 Ω) respectively to USIM_DATA, USIM_RESET, USIM_CLK, and USIM_DET (close to the card connector) in series to enhance the ESD performance.
- The placements from C1 to C4 are designed to place the high-frequency filter capacitors. The recommended capacitance value is not greater than 10 pF. No capacitors are placed on them by default in design. Please adjust it according to the actual debugging results.
- N715-EA supports USIM detection. USIM_DET is a 1.8 V interrupt pin. The USIM detection circuit works by checking the voltage-level across the USIM_DET pin before and after a USIM card is inserted. In the reference circuit, Figure 5-19, SIM_DET is grounded before a USIM card is inserted and is connected to a 1.8 V voltage after a USIM card is inserted. The high voltage-level means USIM card detected while the low voltage-level means no USIM card detected. In the reference circuit, Figure 5-20, SIM_DET is at a high-level voltage before a USIM card is inserted and is grounded after a USIM card is inserted. The low voltage-level means USIM card detected while the high voltage-level means no USIM card detected.

If the USIM card hot-swapping function is not used, the USIM_DET pin must be pulled up to 1.8 V with a 47 kΩ resistor in series, and the USIM hot-swapping detection function must be disabled in software. Figure 5-21 shows the reference design of USIM card (without hot-swapping function) interface.

Figure 5-21 Reference design of the USIM card (without hot-swap) interface



PCB Design Guidelines

- USIM signals are like to be jammed by RF radiation, resulting in failure to detect the USIM card. Keep USIM cards far away from the area where antennas and RF circuits are located.
- Keep USIM cards close to the module and keep USIM traces as short as possible.
- On the USIM traces, connect the series resistor and ESD protection component close to the USIM card.
- In order to enhance EMC, surround USIM traces with ground.

5.3.4 SDIO

Signal	Pin	I/O	Function description	Remarks
SDIO2_CMD	99	DO	SDIO2 command control	Used for external WLAN chip
SDIO2_CLK	118	DO	SDIO2 clock	
SDIO2_DATA0	98	B	SDIO2 data 0	
SDIO2_DATA1	95	B	SDIO2 data 1	
SDIO2_DATA2	119	B	SDIO2 data 2	
SDIO2_DATA3	100	B	SDIO2 data 3	

The module provides one SDIO2 interface, which can be used to connect the external WLAN chip. With the high-speed nature of the SDIO2 data signals, careful attention must be paid to PCB layout and design to maintain adequate signal integrity.

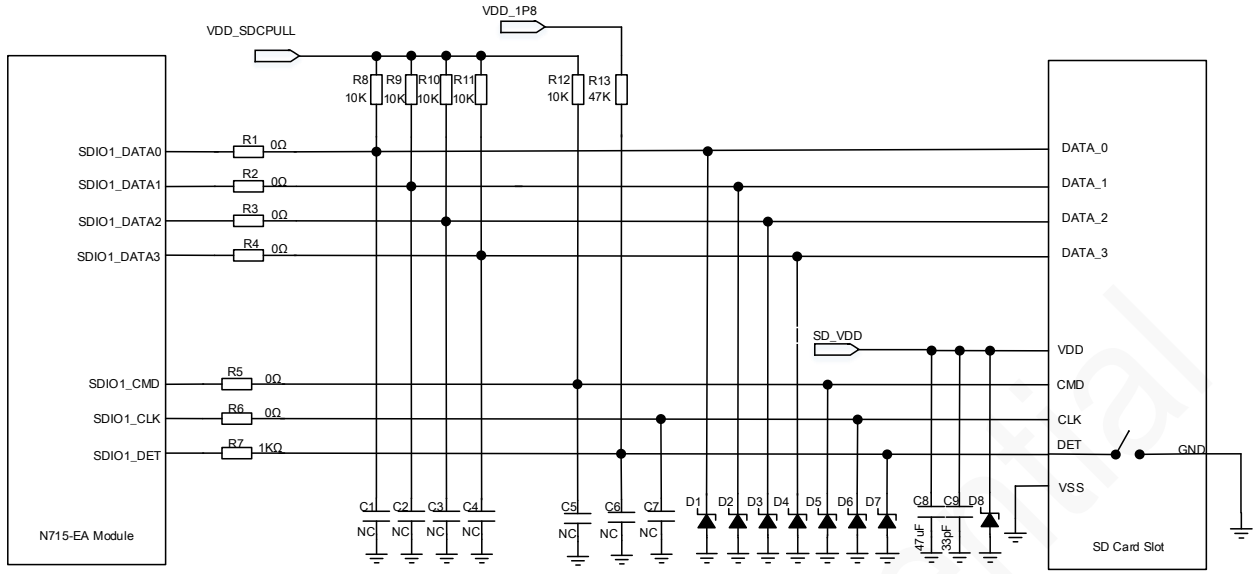
- Traces should be of equal length on each differential pair to minimize EMI and jitter. The DATA traces (DATA [0-3]) should be matched in length to within 0.5 mm, and the CMD, CLK and DATA traces should be matched in length to within 0.5 mm.
- Spacing between DATA traces should be larger than 2 times trace width.
- Control the impedance for each SDIO trace to 50 Ω.
- Keep SDIO traces far away from the RF, analog, clock, and DC-DC signals.

5.3.5 SDCard (Signal Multiplexing)

Signal	Pin	I/O	Signal multiplexing	Remarks
VDD_SDCPULL	133	PO	SD card IO power supply	Pull-up power supply of SDIO It cannot used to furnish power for the SD card. Leave this pin open if unused.
SDIO1_CLK	132	DO	SDIO1 clock	-
UART1_DCD	48	DO	SDIO1_CMD	-
UART1_DTR	39	B	SDIO1_DATA0	-
UART1_RI	40	B	SDIO1_DATA1	-
WAKEUP_IN	49	B	SDIO1_DATA2	-
AP_READY	50	B	SDIO1_DATA3	-
I2C_SDA	56	B	SDIO1_DET	-

SD interface supports 1.8 V/3.0 V dual voltages and a maximum clock frequency of 33.33 MHz. The following shows the reference design of the SDC interface.

Figure 5-22 Reference design of the SD card interface



Schematic Design Guidelines

- VDD_SDCPULL is a 1.8 V/3.0 V dual-voltage power supply; configure it according to the SD card voltage type. It outputs a maximum current of 50 mA and is only used for SD pull-up. Do not use it for any other purpose.
- SD_VDD is used to drive SD card peripherals
- N715-EA supports SD card detection, which is triggered by a 1.8 V interrupt pin. The SD detection circuit works by checking the voltage-level across the USIM_DET pin before and after a SD card is inserted. In the reference circuit, Figure 5-22, SD_DET is at a high-level voltage (with external pull-up to VDD_1P8) before a SD card is inserted and is grounded after a SD card is inserted. The low-level means SD card detected while the high-level means no SD card detected.

PCB Design Guidelines

- Ensure that the power supply trace width is not less than 0.6 mm.
- Control the trace lengths of each SDIO signal. The DATA traces should be matched in length to within 0.5 mm, and the CMD, CLK and DATA traces should be matched in length to within 0.5 mm.
- Spacing between DATA traces should be larger than 2 times trace width.
- Control the impedance for each SDIO trace to 50 Ω.

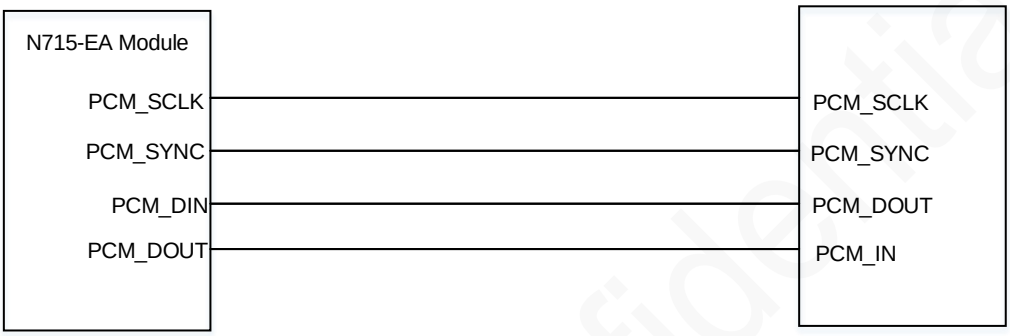
5.3.6 PCM

Signal	Pin	I/O	Function description	Remarks
PCM_SYNC	58	DI	PCM data frame sync	-
PCM_DIN	59	DI	PCM data input	-

PCM_DOUT	60	DO	PCM data output	-
PCM_CLK	61	DO	PCM clock	-

N715-EA provides one 1.8 V PCM interface. The following figure shows the reference design of the PCM interface.

Figure 5-23 PCM reference design



Schematic Design Guidelines

If the levels of N715-EA and Codec do not match, add a voltage-level translation circuit as required by referring to the description of voltage-level translation circuit in section 5.3.2 .

PCB Design Guidelines:

- Reduce the cross routing between the PCM signal cable and other cables. If cross routing cannot be avoided, keep this signal cable perpendicular to other cables to reduce coupling.
- Keep the PCM signal cable away from areas where static electricity may be introduced.
- PCM_SCLK should be ground shielded. It is also recommended that other signal cables be shielded with surrounded ground.

5.3.7 SPI

Signal	Pin	I/O	Function description	Remarks
SPI_CLK	1	DO	Clock signal	Supporting only master mode. Leave this pin open if unused.
SPI_MISO	2	DI	Output of the slave device and input of the master device	
SPI_MOSI	3	DO	Input of the slave device and output of the master device	
SPI_CS_N	4	DO	Chip select signal of the slave device	

The 1.8 V SPI interface supports only master mode and frequencies up to 50 MHz. The following figure shows the reference design of the SPI interface.

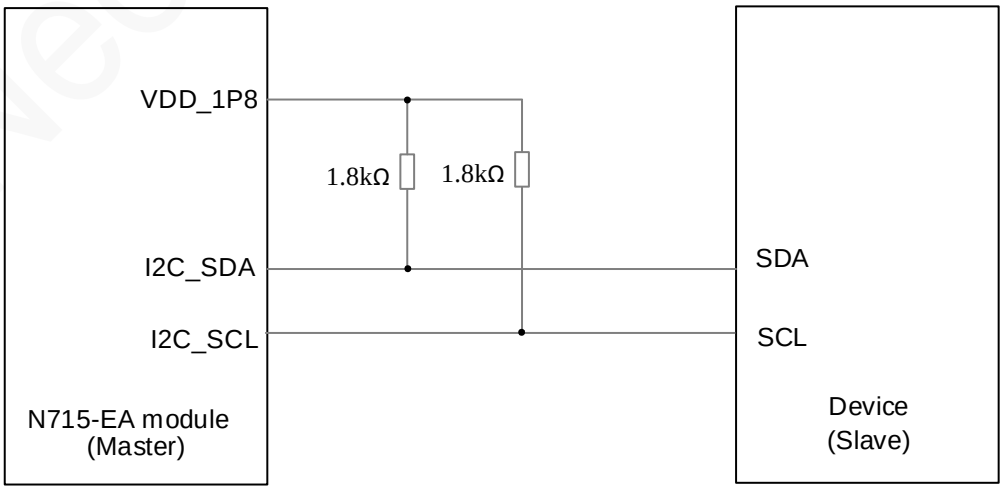
Figure 5-24 SPI reference design

5.3.8 I2C

Signal	Pin	I/O	Function description	Remarks
I2C_SDA	56	B	I2C data	It must be connected to a pull-up resistor (1.8 kΩ is recommended) to VDD_1P8.
I2C_SCL	57	DO	I2C clock	

N715-EA provides one 1.8 V I2C interface, supporting only master mode and speed rates up to 3.4 Mbps. The following shows the reference design of the I2C interface.

Figure 5-25 I2C reference design



5.4 Audio Interfaces

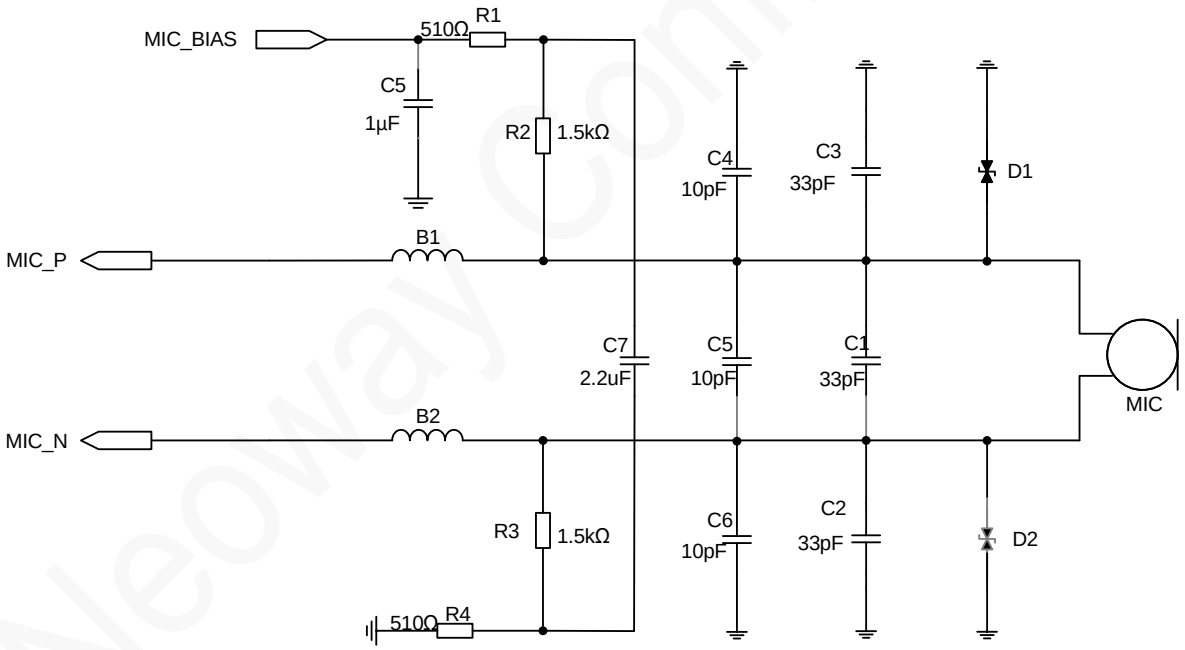
N715-EA provides many audio input/output interfaces to meet your demands for the audio function in different environments.

5.4.1 Analog Audio Input

Signal	Pin	I/O	Function description	Remarks
MIC_N	23	AI	MIC input channel -	-
MIC_P	24	AI	MIC input channel +	-
MIC_BIAS	25	PO	Microphone bias power supply	V_O=2.2 V - 3 V, V_{norm}=2.2 V

N715-EA supports one MIC differential input. The reference design is as follows:

Figure 5-26 Reference design of the MIC differential input



Schematic Design Guidelines

- D1 and D2 are TVS diodes to prevent MIC from introducing ESD and damaging the module.
- C1 to C6 are filter capacitors to filter out undesirable frequencies. Adjust the parameters according to the actual debugging situation.

- B1 and B2 are ferrite beads used to filter out high-frequency noise. It is recommended to use ferrite beads specifically for audio and the ferrite beads should have an impedance of 1800 Ω or higher at 100 MHz and a DC resistance lower than 1.5 Ω. Dedicated audio magnetic beads are recommended.
- It is recommended to adopt an electret MIC that embeds dual capacitors (e.g.10 pF and 33 pF) to filter out RF jamming and reduce TDD coupled noise.

PCB Design Guidelines

- MIC_P and MIC_N traces should comply with the differential rules
- Shield the audio traces with surrounded ground. Keep them 3 times widths away from other signal traces.
- Place RF filter capacitors close to the audio components or pins.
- Keep traces far away from interference sources, such as DC-DC power supply.

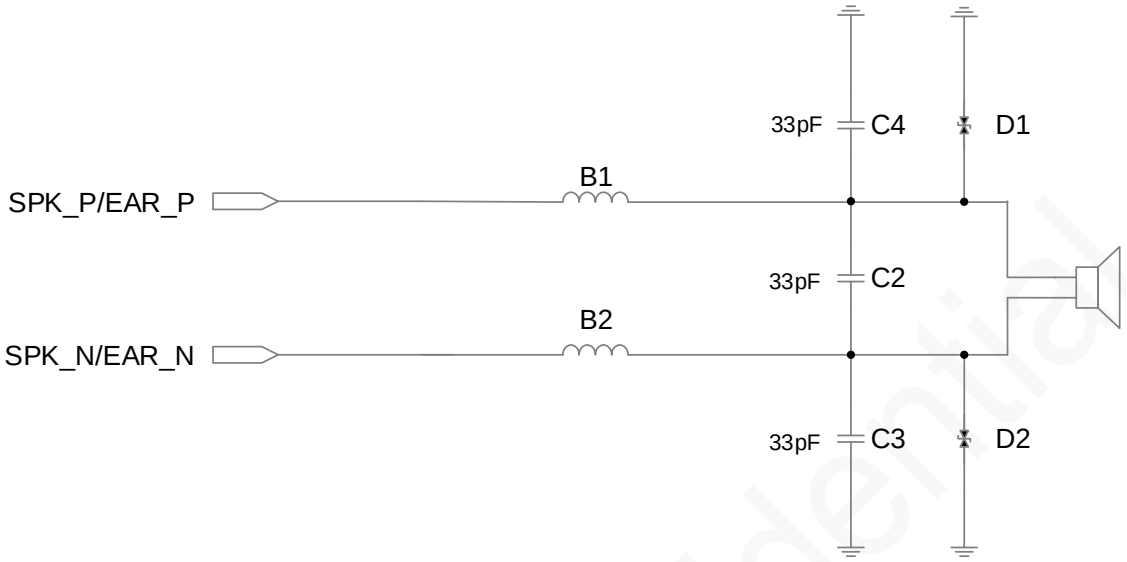
5.4.2 Analog Audio Output

Signal	Pin	I/O	Function description	Remarks
EAR_N	21	AO	Earpiece output -	With a 32 Ω load, the maximum output power is 50 mW. If the output power is not enough, connect this interface to an external power amplifier.
EAR_P	22	AO	Earpiece output +	
SPK_P	109	AO	Speaker output +	Support differential output only, with built-in class-AB or class-D power amplifier. Peak output power: Class AB: 600 mW@4.2V, with a 8 Ω load Class D: 800 mW@4.2V, with a 8 Ω load
SPK_N	110	AO	Speaker output -	

The external power amplifier should be added as required. The following shows the reference design of the audio interface:

Reference Design without External Power Amplifier

Figure 5-27 Reference design of audio interface in EAR/ SPK differential mode



Schematic Design Guidelines

- C2, C3, and C4 are used to place capacitors to filter out jamming frequencies.
- TVS diodes at D1 and D2 are used to prevent ESD from damaging the module.
- B1 and B2 are ferrite beads to filter out high-frequency noise. It is recommended to use ferrite beads specifically for audio.

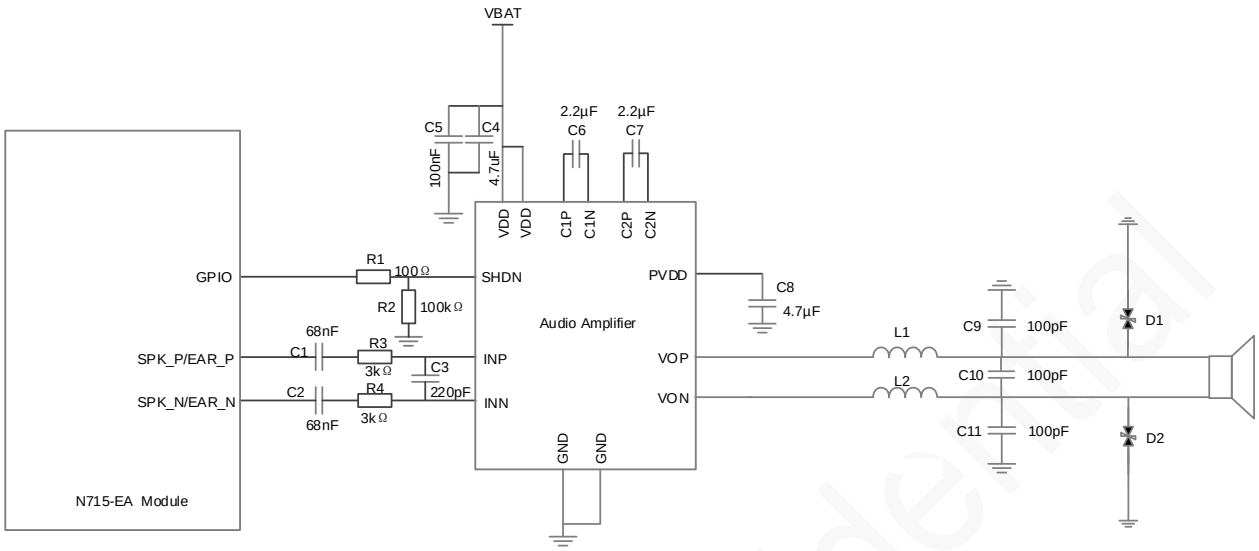
  Note the DC resistance of the ferrite beads because overlarge DC resistance will consume too much audio power while audio output components generally have a small impedance. A ferrite bead with a DC resistance lower than 0.1 Ω is recommended.

PCB Design Guidelines

- The audio signal traces should be wide enough (0.5 mm is recommended) on the PCB to bear large current when audios are outputted at the highest volume. Isolate the traces from high-speed digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough grounding holes and ground protection.
- Keep audio traces far away from antenna to reduce jamming. Avoid parallel layout between power supply traces and audio traces.
- It is important to route the audio signal traces as differential pairs.

Reference Design with External Power Amplifier

Figure 5-28 Reference design of the external power amplifier connection



Schematic Design Guidelines

- Connect the SPK/EAR output of the module to the power amplifier with differential connection and select a power amplifier that can support differential input for the audio connection.
- Note that the over-current capability of L1 and L2 must meet the current demand at the maximum power. DCR is recommended to be less than 100 mΩ.

PCB Design Guidelines

- Ensure that the width of audio input/output traces be no less than 0.5 mm.
- The analog audio traces should be surrounded with ground and comply with the differential routing rules. Isolate the traces from digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough grounding holes and ground protection.

5.4.3 Headset Interface

N715-EA headset interface pinouts:

Table 5-2 Headset audio pin description

Signal	Pin	I/O	Function description	Remarks
AMP_VCOMP	94	-	Headset-dedicated ground	Route traces between the left and right sound channels of the headset, connect to the GND of the

				headset connector, and then the main ground.
HP_L	111	AO	Headset left channel	-
HP_P	112	AO	Headset right channel	-
HEADMIC_P	140	AI	Module-side differential input +	-
HEADMIC_N	141	AI	Module-side differential input -	-
HEADMIC_BIAS	143	PO	MIC bias power supply	-
HP_DET	142	DI	Headset plug detect	-
HEADMIC_IN_DET	93	DI	headset single-ended input channel and insertion detection	-

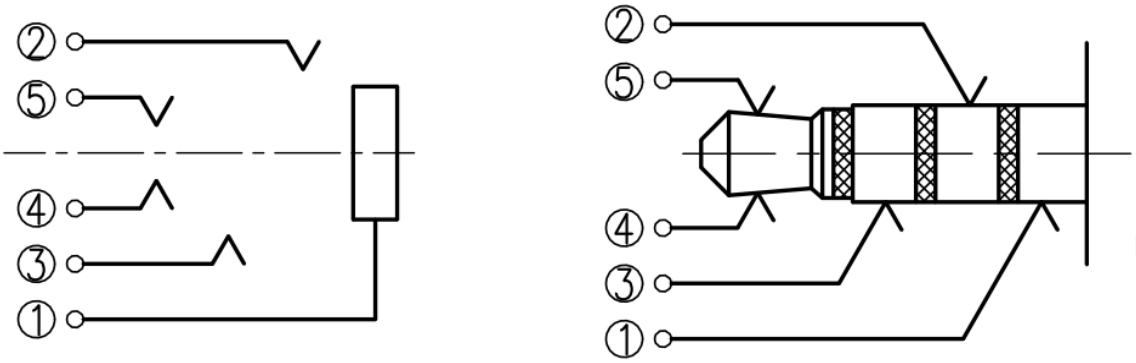
The following figure shows the reference design of the headset interface.

Figure 5-29 Reference design of the headset interface

TBD

There are two commonly used headphone jack (3.5 mm) pin definitions

Figure 5-30 Headphone interface diagram



Pin definition A:

1—MIC

2—GND

3—R

4—L

5—HPH_DET

Pin definition B:

1—GND

2—MIC

3—R

4—L

5—HPH_DET

Please note if the headphone you select is A-type or B-type. The connections of ① and ② are reversed for the two type of headphones. The HPH_DET pin (⑤ in the above figure) is not connected (pulled up internally) if the headphone is not plugged. After the headphone is plugged, this pin is connected to GND through the left channel (8/16/32 Ω) loudspeaker of the headphone.

PCB Design Guidelines

- The audio signal traces should be wide enough on the PCB to bear large current when audios are outputted at the highest volume. Isolate the traces from high-speed digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough grounding holes and ground protection.
- Keep audio traces far away from antenna to reduce jamming. Avoid parallel layout between power supply traces and audio traces.
- It is important to route the audio signal traces as differential pairs.

5.5 Video Interfaces

5.5.1 LCD

N715-EA provides an LCD-dedicated SPI interface, supporting frame rates up to QVGA@30fps. The following shows the LCD interface description. The following shows the LCD interface pin description.

Table 5-3 LCD interface pin description

Signal	Pin	I/O	Function description	Remarks
LCD_TE	62	DI	LCD frame synchronization	-
LCD_SPI_RS	63	DO	LCD register selection	-
LCD_RESET	64	DO	LCD reset	-
LCD_SPI_CS	65	DO	LCD chip select	-
LCD_SPI_DOUT	66	B	LCD data	-
LCD_SPI_CLK	67	DO	LCD clock	-
LCD_ISINK	135	PI	sink current input pin, used to adjust backlight brightness.	I_{max} = 200 mA, the current value is configurable.
LCD_SEL	137	DO	Reserved	-
LCD_DVDD	134	PO	LCD digital power	V_{nom} = 1.8 V
LCD_AVDD	138	PO	LCD analog power	V_{nom} = 3.0 V

5.5.2 Camera

N715-EA provides a camera-dedicated SPI interface, supporting frame rates up to VGA@30fps. The following shows the camera interface description.

Signal	Pin	I/O	Function description	Remarks
CAM_MCLK	10	DO	Camera main clock	-
CAM_I2C_SCL	11	DO	Camera I2C clock	Connect this pin to a pull-up resistor externally when used. Leave this pin open if unused.
CAM_I2C_SDA	12	B	Camera I2C data	
CAM_SPI_CLK	13	DO	Camera SPI clock	-
CAM_SPI_DATA0	14	B	Camera SPI data 0	-
CAM_SPI_DATA1	15	B	Camera SPI data 1	-
CAM_PWDN	16	DO	Camera power down	-
CAM_RESET	120	DO	Camera reset	-
CAM_AVDD	17	PO	Camera analog power	Disabled by default, after enabled, it outputs 2.8 V voltage.
CAM_DVDD	68	PO	Camera digital power supply	Disabled by default, after enabled, it outputs 1.8 V voltage.

5.6 Radio Frequency

Signal	Pin	I/O	Function description	Remarks
ANT_WLAN_BT	42	AIO	Shared antenna interface of Bluetooth and Wi-Fi scan	50 Ω impedance characteristics
ANT_MAIN	46	AIO	Main antenna pin	

5.6.1 ANT_MAINAntenna Interfaces

The antenna interface of the N715-EA requires the 50 Ω impedance feature. The impedance of the cable from the module interface to the antenna needs to be kept at 50 Ω impedance to ensure RF performance. A matching network needs to be added in the middle. The matching network is generally

divided into three types: L type, T type, and π type. As shown in the figure below, it is recommended to reserve a π-type matching circuit for better RF performance.

Figure 5-31 L-type network

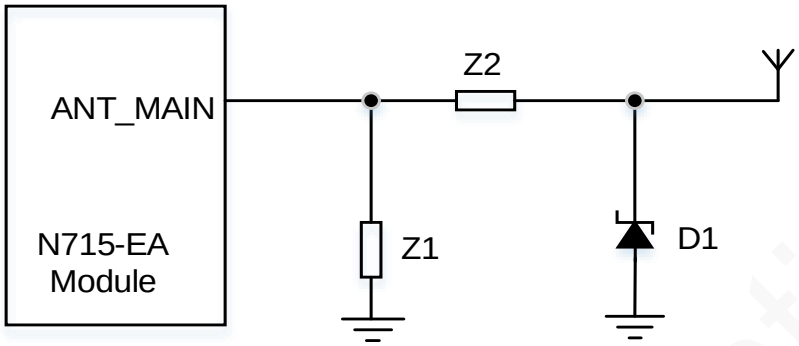


Figure 5-32 T-type network

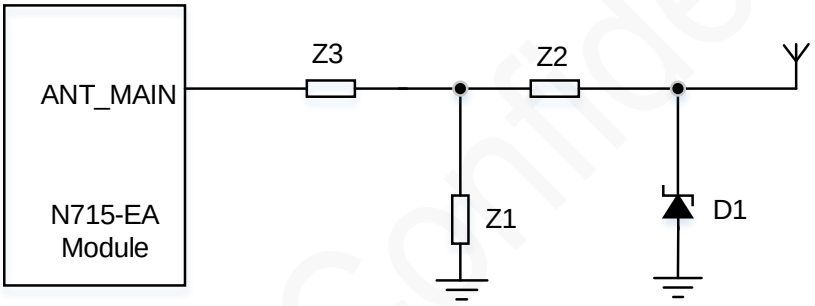
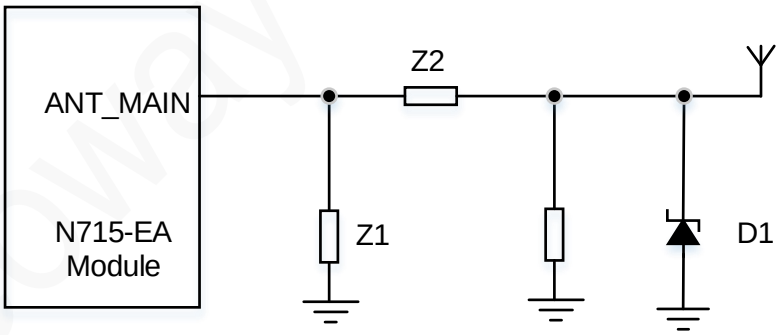


Figure 5-33 π-type network



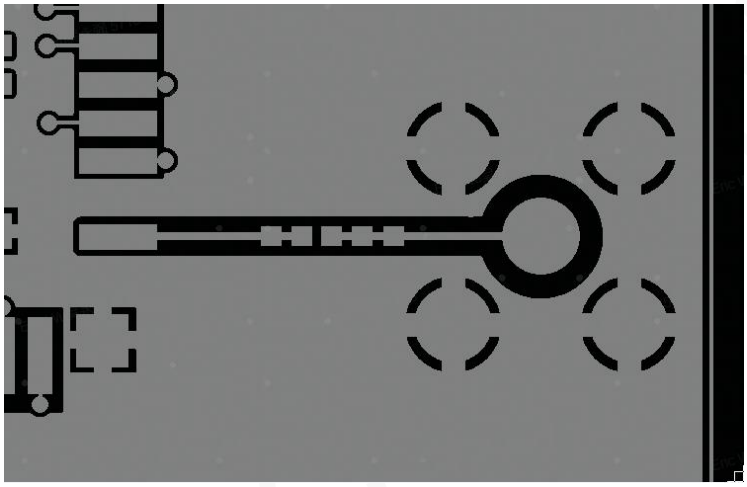
Schematic Design Guidelines

- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- Add an ESD protector if the antenna might generate static electricity. The protector can be a ESD diode with a junction capacitance of less than 0.5 pF. Ensure that the reverse breakdown voltage of the ESD greater than 10 V (above 15 V is recommended).

PCB Design Guidelines

- Lay copper foil around the RF connector. Dig as many ground holes as possible on the copper and the characteristic impedance of all RF traces should be controlled to 50 Ω.
- Traces between the RF pin and the antenna connector should be as short as possible. Control the trace impedance to 50 Ω.
- If you adopt an SMA connector, a big RF solder pad might result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and fourth layers or all layers of a multiple-layer PCB under the RF solder pad.

Figure 5-34 Recommended RF PCB design



- A reasonable distance should be kept between ANT_MAIN and ANT_WLAN_BT to avoid mutual interference that may affect reception performance.
- On the PCB, keep the RF signals and components far away from high-speed circuits, power supplies, transformers, great inductors, the clock signal, etc.

5.6.2 ANT_WLAN_BT

The 42 pin of the N715-EA module is shared by the WLAN and Bluetooth antennas. It has a characteristic impedance of 50 Ω.

For the schematic design and the PCB design of the WLAN antenna and Bluetooth antenna interface, see the requirements in section 5.6.1 “ANT_MAIN”.

5.6.3 Antenna Assembling

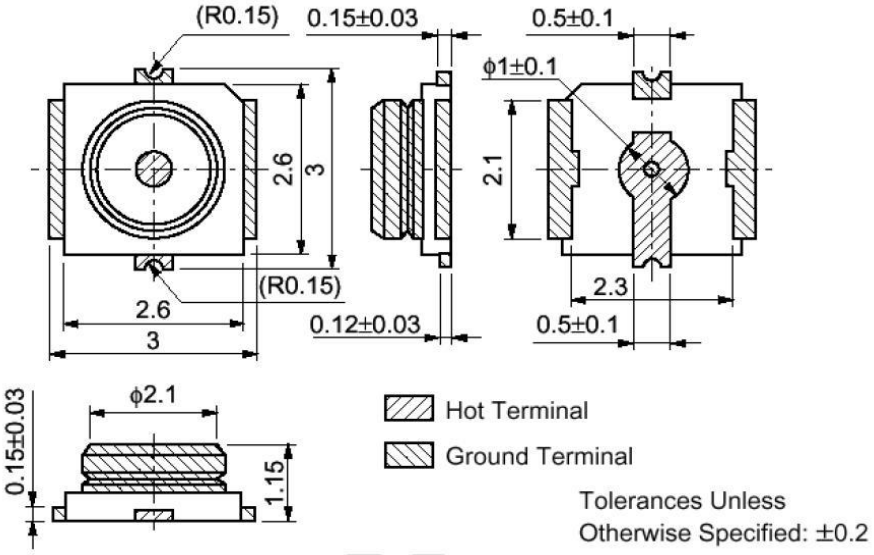
The antenna used by the module must comply with the mobile device standard. The standing wave ratio should be between 1.1 and 1.5, and the input impedance should be 50 Ω. Requirements for antenna gain vary according to the application environment. You can choose a suitable antenna according to specific application scenarios and environments.

Antenna interfaces can be connected to a rubber ducky antenna, magnet antenna, or embedded Planar Inverted F Antenna (PIFA). Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.

The following methods are commonly used to assemble antenna:

- GSC RF connector
  MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

Figure 5-35 Murata RF connector encapsulation specifications



- The RF cable is connected to the module by means of soldering. However, this method has the stability, consistency, and RF performance degradation issues, and therefore is not recommended.

The following figure shows the effect of the connection methods.

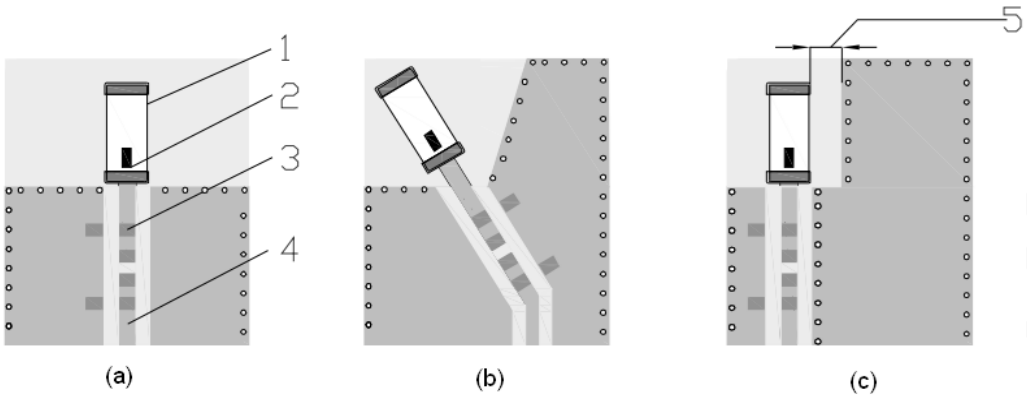
Figure 5-36 RF cable connections

- PCB Printing or SMT

  The module works in a wide frequency range, but it is difficult for PCB antennas or ceramic antennas to cover a wide frequency. Therefore, this connection method is recommended only for 2.4 GHz Wi-Fi or BT/ BLE antennas.

The following figure shows the layout of the 2.4 GHz ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

Figure 5-37 Antenna layout

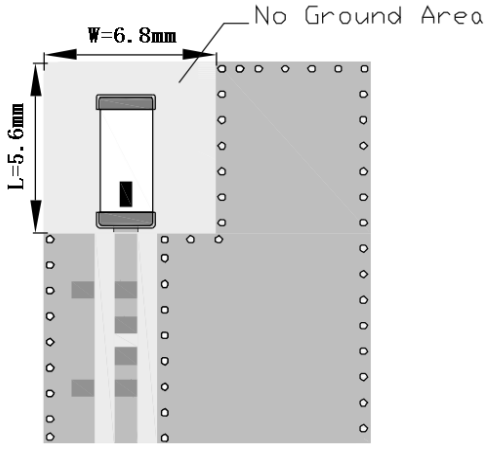


If your PCB is large enough, you can adopt the layout shown in Figure 5-37 (a).

- 1 Chip antenna
- 2 Feeding mark
- 3 Layout pad of the matching circuit
- 4 50 Ω characteristic impedance RF traces

Figure 5-38 shows the layout for the area between the antenna and ground that is marked as "5" in Figure 5-37.

Figure 5-38 Layout around the antenna



For more details, refer to the antenna manuals and other documents.

5.7 GPIO Interfaces

Signal	Pin	I/O	Function description	Remarks
GPIO4	69	B	General Purpose Input Output	-
GPIO5	70	B	General Purpose Input Output	-

N715-EA provides 2 GPIO interfaces, all of which have the interrupt function.

5.8 Multi-Function Interfaces

Table 5-4 Pin definition description

Function (default)	Pin	GPIO	Function (multiplexed)	Pin State	Remarks
UART1_DCD	48	GPIO24	SDIO1_CMD	H	-
UART1_DTR	39	GPIO25	SDIO1_DATA0	H	-
UART1_RI	40	GPIO26	SDIO1_DATA1	H	-
WAKEUP_IN	49	GPIO27	SDIO1_DATA2	H	-
AP_READY	50	GPIO28	SDIO1_DATA3	H	-
I2C_SDA	56	GPIO15	SDIO1_DET	L	-
NET_MODE	52	GPIO31	USIM2_RESET	L	If the USIM2 interface is not used, pins #52 to #54 are available. Otherwise, leave the pins open. If a status indication signal is required, it should be multiplexed by a dedicated pin that is not used; for more information, contact Neoway.
SLEEP_IND	53	GPIO30	USIM2_DATA	L	
NET_LIGHT	54	GPIO29	USIM2_CLK	L	
PCM_SYNC	58	GPIO_1	SPI_FLASH1_CS	L	-
PCM_DIN	59	GPIO_2	SPI_FLASH1_SIO_0	L	-
PCM_DOUT	60	GPIO_3	SPI_FLASH1_SIO_1	L	-
PCM_CLK	61	GPIO_0	SPI_FLASH1_CLK	L	-
GPIO_4	69	GPIO_4	SPI_FLASH1_SIO_2	L	-
GPIO_5	70	GPIO_5	SPI_FLASH1_SIO_3	L	-

USIM2_RESET	145	-	NET_MODE	L	Using the USIM2 interface and the pins #52 to #54 simultaneously are not allowed, that is, when the USIM2 interface is connected, you should leave these pins open.
USIM2_DATA	146	-	SLEEP_IND	L	
USIM2_CLK	147	-	NET_LIGHT	L	

N715-EA provides 18 pins with multiplexing function. For more details, see section 4.2

If the signal multiplexing table is required, contact Neoway.

5.9 Other Interfaces

5.9.1 ADC

The module provides four ADC channels and their input voltage ranges from 0 V to VBAT. The ADC interfacea support the highest precision of 12bit and it can be used for temperature detection and other checks. For details, see *Neoway_N715-EA_AT_Commands_Manual*.

Signal	Pin	I/O	Function description	Remarks
ADC0	19	AI	Universal ADC interface	-
ADC1	20	AI	Universal ADC interface	
ADC2	113	AI	Universal ADC interface	
ADC3	114	AI	Universal ADC interface	

5.9.2 WAKEUP_IN

Signal	Pin	I/O	Function description	Remarks
WAKEUP_IN	49	DI	Module wakeup	-

WAKEUP_IN the control pin of sleep mode, it needs to be used together with the AT commands. For details, see *Neoway_N715-EA_AT_Commands_Manual*. In sleep mode, the module can also respond to incoming call, SMS, and data service in time.

The following shows the process of entering sleep mode:

Figure 5-39 Process of entering into sleep mode

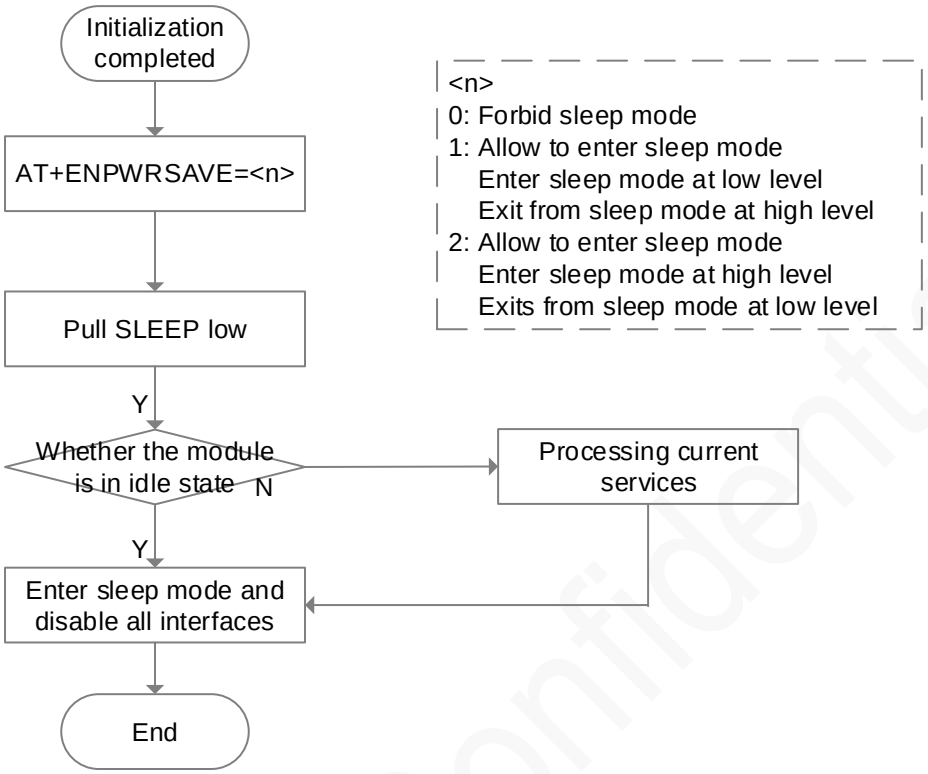


Figure 5-40 Incoming call service process

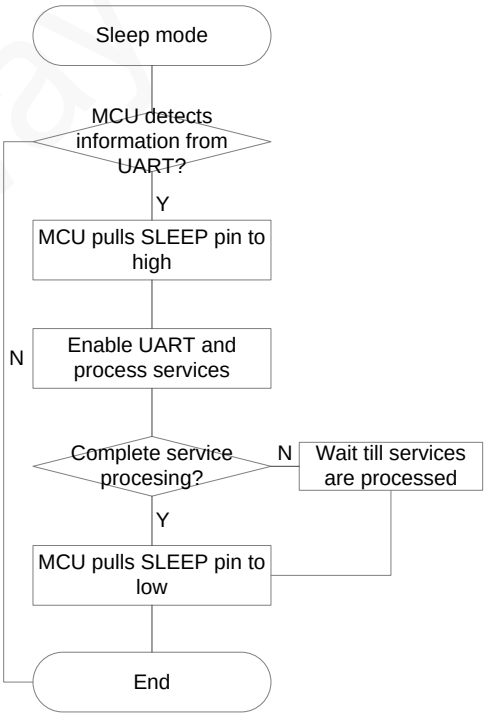
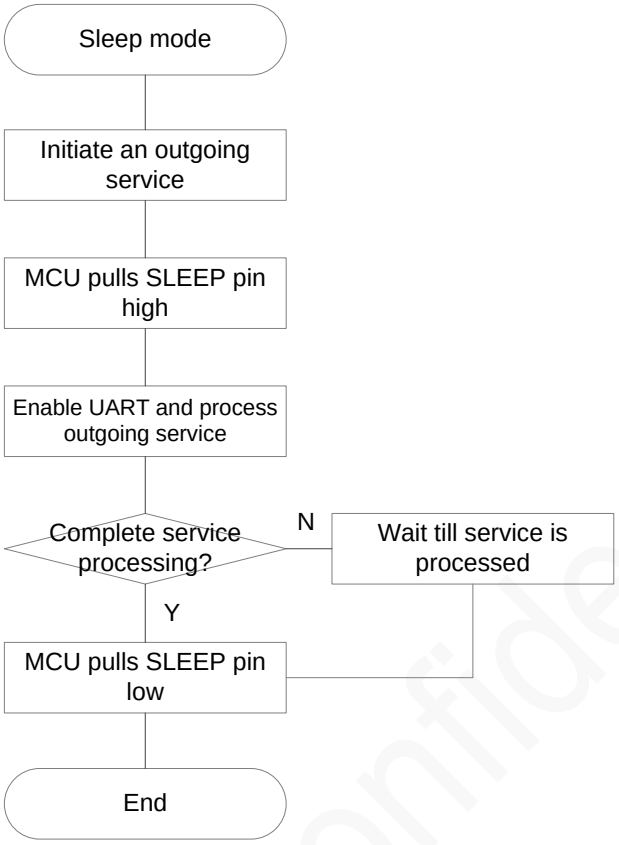
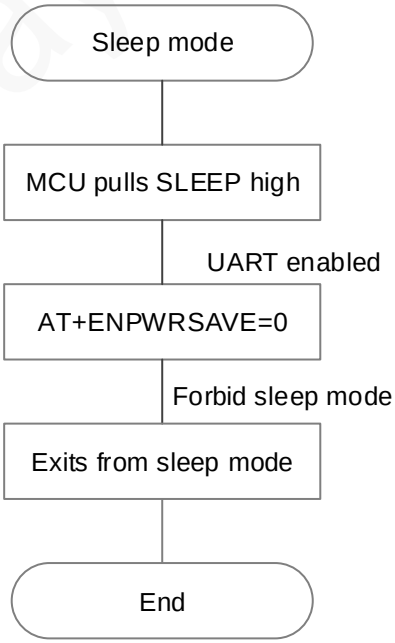


Figure 5-41 Outgoing call service process



The following shows the process of exiting from sleep mode:

Figure 5-42 Process of existing from sleep mode



5.9.3 Status Indication

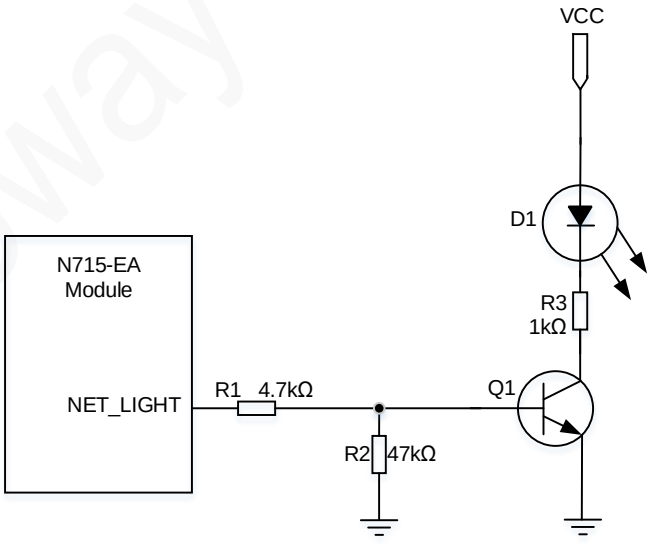
Signal	Pin	I/O	Function description	Remarks
NET_MODE	52	DO	Registered network mode indication	Note: If the USIM2 interface is not used, pins #52 to #54 are available; otherwise, leave these pins open. If status indication is required, it should be multiplexed from the other not pin that is not used; for more details, contact Neoway.
SLEEP_IND	53	DO	Sleep mode indication	
NET_LIGHT	54	DO	Network status indication	

Note: If the USIM2 interface is not used, pins #52 to #54 are available; otherwise, leave these pins open. If status indication is required, it should be multiplexed from the other not pin that is not used; for more details, contact Neoway

NET_MODE, SLEEP_IND, and NET_LIGHT are respectively the registered network mode indication, sleep mode indication, and network status indication pins. They output PMW waves of duty cycle varying with the status of the module and drives an LED indicator to blink at different frequencies. You can use the AT+SIGNAL command to enable the LED indicator to blink in different states. For detailed usage, see *Neoway_N715-EA_AT_Commands_Manual*.

Do not use the indication pin to drive the LED indicator directly since the pin outputs a high level of 1.8 V. It is recommended to drive the LED indicator by controlling a triode.

Figure 5-43 Driving LED indicator with a triode



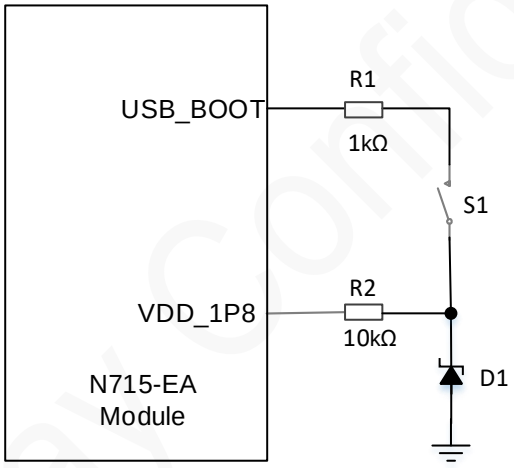
5.9.4 USB_BOOT

Signal	Pin	I/O	Function description	Remarks
USB_BOOT	55	DI	Forcible download/upgrade control pin	-

N715-EA provides a USB_BOOT pin. During development, USB_BOOT can force the module to boot from USB port for firmware upgrade.

To force the module into emergency download mode, you can connect USB_BOOT of the module to VDD_1P8 through a pull-up resistor in a short time during the module's power-on process. This is the last method to handle issues that result in startup or running failures. It is recommended to reserve this pin to facilitate software upgrades and debugging. The following figure shows the reference design of this pin. Adding an ESD component to protect USB_BOOT in the circuit is required.

Figure 5-44 Reference design of USB emergency download mode



5.9.5 Keypad

N715-EA supports a 6x6 matrix keypad. The following shows the pin descriptions.

Signal	Pin	I/O	Function description	Remarks
USB_BOOT	55	DI	Key 0 of inputting	After the module is started, the key is used for KEYIN0.
KEYIN1	129	DI	Key 1 of inputting	Leave this pin open if unused.
KEYIN2	128	DI	Key 2 of inputting	Leave this pin open if unused.
KEYIN3	127	DI	Key 3 of inputting	Leave this pin open if unused.
KEYIN4	126	DI	Key 4 of inputting	Leave this pin open if unused.
KEYIN5	125	DI	Key 5 of inputting	Leave this pin open if unused.

KEYOUT0	105	DO	Key 0 of outputting	Leave this pin open if unused.
KEYOUT1	106	DO	Key 1 of outputting	Leave this pin open if unused.
KEYOUT2	107	DO	Key 2 of outputting	Leave this pin open if unused.
KEYOUT3	108	DO	Key 3 of outputting	Leave this pin open if unused.
KEYOUT4	104	DO	Key 4 of outputting	Leave this pin open if unused.
KEYOUT5	103	DO	Key 5 of outputting	Leave this pin open if unused.

Do Not set the KEYIN1 and USB_BOOT pins to high before power-on; otherwise, the module will enter download mode and cannot start up properly.

5.9.6 PSM Interface

Signal	Pin	I/O	Function description	Remarks
PSM_EXT_INT*	116	DI	Interrupt pin for PSM wakeup Setting this pin high externally can wake up the module from PSM.	-

6 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the N715-EA module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

6.1 Electrical Characteristics

- If the voltage is lower than threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it outputs at least 2.5 A current. The 2.5 A current occurs when the module is working at the maximum power level of the GSM mode. The peak current during burst transmission has a short duration. Placing a large capacitor on the VBAT pin of the module can effectively enhance the flyback capability of the power supply and avoid excessive voltage drops that may cause exceptions, such as module shutdown.

Table 6-1 N715-EA electrical characteristics

Parameter		Minimum value	Typical value	Maximum value
VBAT	V_{in}	3.4 V	3.6 V	4.2 V
	I_{in}	N/A	N/A	2.5 A

Table 6-2 N715-EA current consumption (Typical)

Status / Network standard and band	Sleep (mA)	Idle (mA)	Active power (mA)@max
FDD-LTE: B1, B3, B5, B7, B8, B20, B28	< 3 mA	< 15 mA	< 610 mA
TDD-LTE: B38, B40, B41	< 3 mA	< 15 mA	< 340 mA
GSM 900	< 3 mA	< 15 mA	< 245 mA
DCS 1800	< 3 mA	< 15 mA	< 175 mA

6.2 Temperature Characteristics

Table 6-3 N715-EA temperature characteristics

Parameter	Minimum value	Typical value	Maximum value
Operating	-30℃	25℃	75℃
Extended	-40℃	25℃	85℃
Storage	-40℃	25℃	90℃

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse but it can still work properly.

6.3 ESD Protection

Electronic products generally need to undergo strict ESD testing. The following is the ESD protection capability of the main pins of the module. When designing related products, customers need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25℃

Table 6-4 N715-EA ESD protection characteristics

Testing point	Contact discharge	Air discharge
GND	±8 kV	±15 kV
ANT interface	±8 kV	±15 kV
Cover	±8 kV	±15 kV

Test data in the above table is obtained from tests performed using a N715-EA EVB.

7 RF Characteristics

N715-EA supports GSM, FDD-LTE (Cat.1), TDD-LTE (Cat.1) network modes and the Wi-Fi, RX, and BT wireless connection function.

7.1 Operating Band

Table 7-1 N715-EA operating bands

Operating band	Uplink	Downlink
FDD-LTE B1	1920~1980 MHz	2110~2170 MHz
FDD-LTE B3	1710~1785 MHz	1805~1880 MHz
FDD-LTE B5	824~849 MHz	869~894 MHz
FDD-LTE B7	2500~2570 MHz	2620~2690 MHz
FDD-LTE B8	880~915 MHz	925~960 MHz
FDD-LTE B20	832~862 MHz	791~821 MHz
FDD-LTE B28	703~748 MHz	758~803 MHz
TDD-LTE B38	2570~2620 MHz	2570~2620 MHz
TDD-LTE B40	2300~2400 MHz	2300~2400 MHz
TDD-LTE B41	2535~2655 MHz	2535~2655 MHz
EGSM900	880~915 MHz	925~960 MHz
DCS1800	1710~1785 MHz	1805~1880 MHz

7.2 TX Power and RX Sensitivity

Table 7-2 N715-EA RF transmit power

Band	Max Power	Min. Power
FDD-LTE B1	23 dBm±2 dB	<-40 dBm
FDD-LTE B3	23 dBm±2 dB	<-40 dBm

FDD-LTE B5	23 dBm±2 dB	<-40 dBm
FDD-LTE B7	23 dBm±2 dB	<-40 dBm
FDD-LTE B8	23 dBm±2 dB	<-40 dBm
FDD-LTE B20	23 dBm±2 dB	<-40 dBm
FDD-LTE B28	23 dBm±2 dB	<-40 dBm
TDD-LTE B38	23 dBm±2 dB	<-40 dBm
TDD-LTE B40	23 dBm±2 dB	<-40 dBm
TDD-LTE B41	23 dBm±2 dB	<-40 dBm
EGSM900	33 dBm±2 dB	5 dBm±5 dB
DCS1800	30 dBm±2 dB	0 dBm±5 dB

Table 7-3 RF RX sensitivity of N715-EA

Band	Receiving sensitivity
FDD-LTE B1	≤ -97 dBm
FDD-LTE B3	< -97 dBm
FDD-LTE B5	≤ -97 dBm
FDD-LTE B7	≤ -96 dBm
FDD-LTE B8	≤ -97 dBm
FDD-LTE B20	< -97 dBm
FDD-LTE B28	≤ -97 dBm
TDD-LTE B38	≤ -97 dBm
TDD-LTE B40	≤ -97 dBm
TDD-LTE B41	≤ -97 dBm
EGSM900	≤ -108 dBm
DCS1800	≤ -107 dBm

The preceding indicators are tested in a shielded environment in the laboratory. The LTE band indicators are the test results when the bandwidth is 10 MHz, the modulation mode is QPST and RB is set according to the protocol. On no-shielded environments, deviations may exist in the receiver sensitivity of some individual bands due to the interference.

7.3 WLAN/BT Characteristics

Table 7-4 WLAN/BT TX power and RX sensitivity

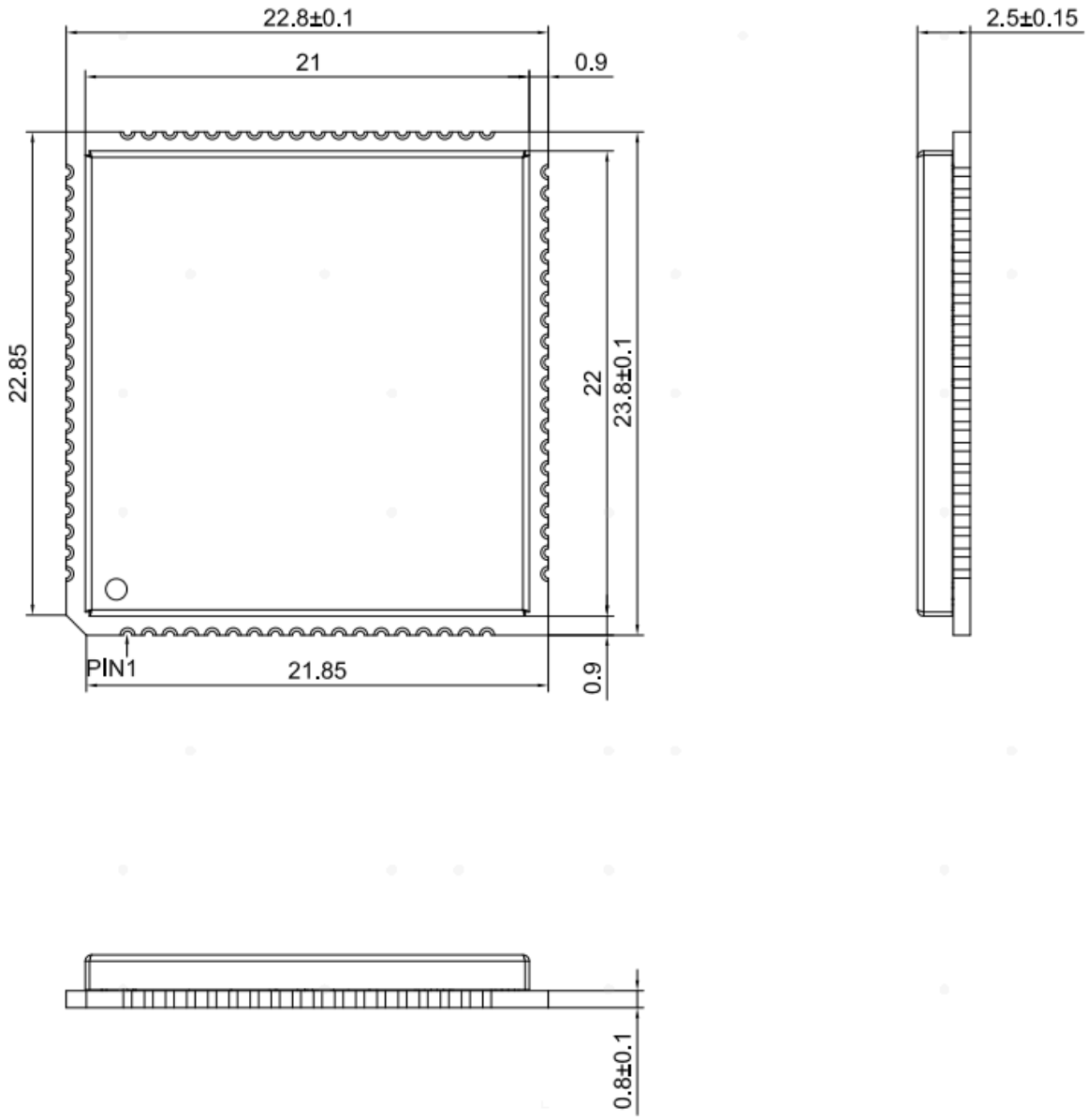
Operating band	Rate	Transmit power	Receiving sensitivity
802.11b (2.4G)	1/2/5.5/11 Mbps	N/A	≤ -88 dBm
Bluetooth	DH5	3.2 dBm	≤ -88 dBm
	2HD5	1 dBm	≤ -88 dBm
	3DH5	1 dBm	≤ -80 dBm
	BLE/1 Mbps	TBD	≤ -94 dBm

8 Mechanical Characteristics

This chapter describes mechanical characteristics of the N715-EA module.

8.1 Dimensions

Figure 8-1 N715-EA top and side view dimensions (unit: mm)



8.2 Label

The N715-EA label is laser etched, and can withstand a high temperature of 260°C. The following shows the label format of N715-EA.

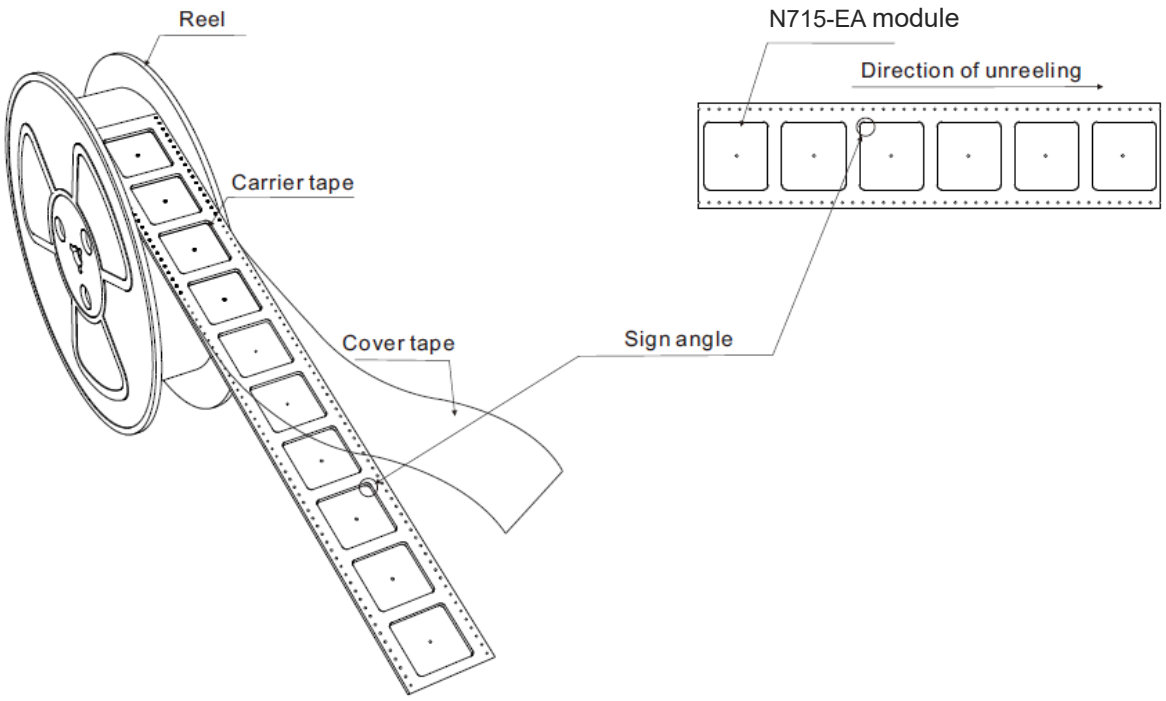
The picture above is only for reference.

8.3 Packaging

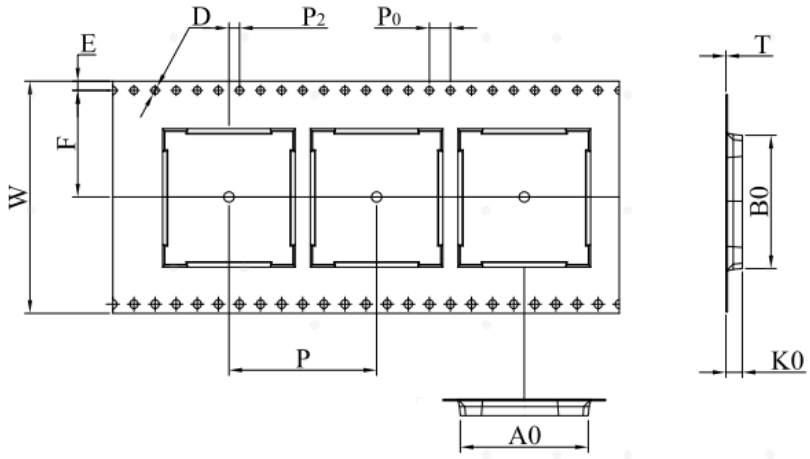
N715-EA adopts the SMT method for oven soldering. To enable efficient production, production lot set-up and tear-down, the modules are delivered as hermetically sealed reeled tapes for moisture-proof packaging and use the aluminum foil bag, desiccant, humidity indicator card, vacuum and other processing methods to ensure the dryness of the product and extend its service life.

8.3.1 Reels

N715-EA in mass production is delivered in the following packaging.



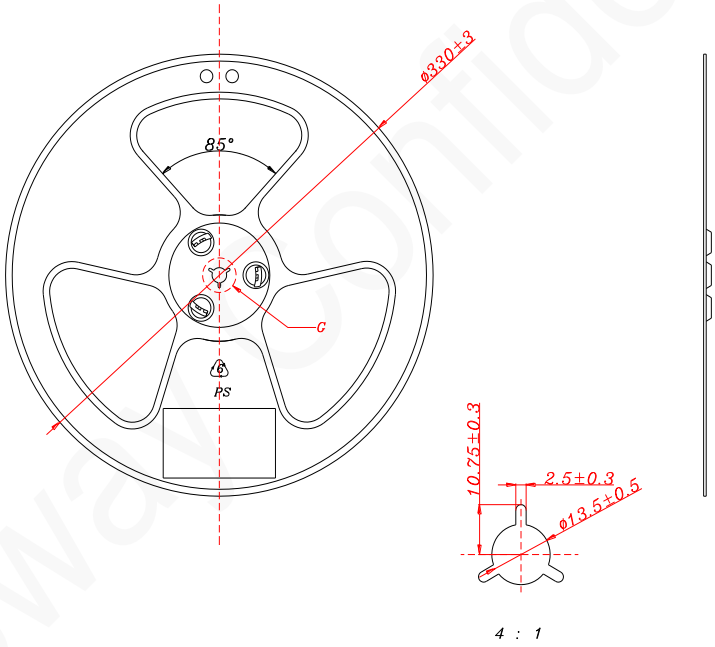
Tape Dimensions



EIA DIMENSIONS	
W	$44.0^{+0.30}_{-0.30}$
E	$1.75^{+0.10}_{-0.10}$
F	$20.2^{+0.15}_{-0.15}$
P	$28.0^{+0.10}_{-0.10}$
P_0	$4.00^{+0.10}_{-0.10}$
P_2	$2.00^{+0.15}_{-0.15}$
D	$1.50^{+0.10}_{-0.10}$
T	$0.30^{+0.05}_{-0.05}$
A_0	$23.2^{+0.10}_{-0.10}$
B_0	$24.2^{+0.10}_{-0.10}$
K_0	$3.10^{+0.10}_{-0.10}$

1. 10 sprocket hole pitch cumulative tolerace ±0.20mm.
2. Carrier camber not to exceed 1mm in 100mm.
3. A_0 and B_0 measured on a plane 0.3mm above the bottom of the pocket.
4. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. All dimensions meet EIA-481-C requirements.
6. Material:Black Anti-Statice Polystyrene.
7. Packing lenght per 13"reel : 17.64 Meters.
8. Component load per 13"reel :630pcs.
9. This Product Must Comply With HSF Standard

Reel Dimensions



8.3.2 Moisture Sensitivity Level

N715-EA modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification..

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. The MSL standard is available in IPC/JEDEC J-STD-020.

- Sealed storage period: 12 months under the condition of temperature below 40°C and humidity less than 90%.
- Production environment condition: 30°C/60%

The module should be pre-baked under the following circumstances:

- The vacuum-sealed packaging is removed for more than 48 hours.
- The relative humidity is greater than 10% (you can see the humidity card that comes with the package).

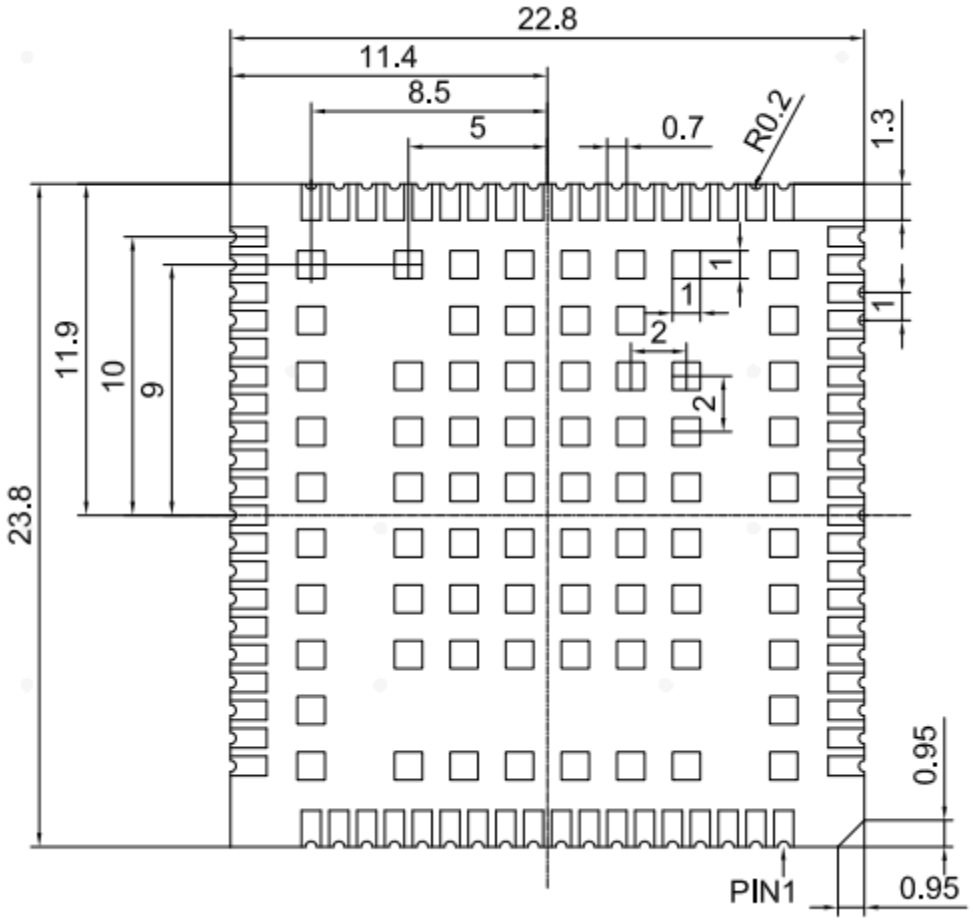
After the module is unpacked, if it is exposed to air for a long time, the module will get damped, and may be damaged during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at temperatures higher than 120 degrees for more than 12 hour

9 Mounting

This chapter describes the module PCB package and application PCB package of N715-EA, as well as the key points of SMT related technology.

9.1 PCB Package

Figure 9-1 Bottom view of N715-EA PCB package (unit: mm)

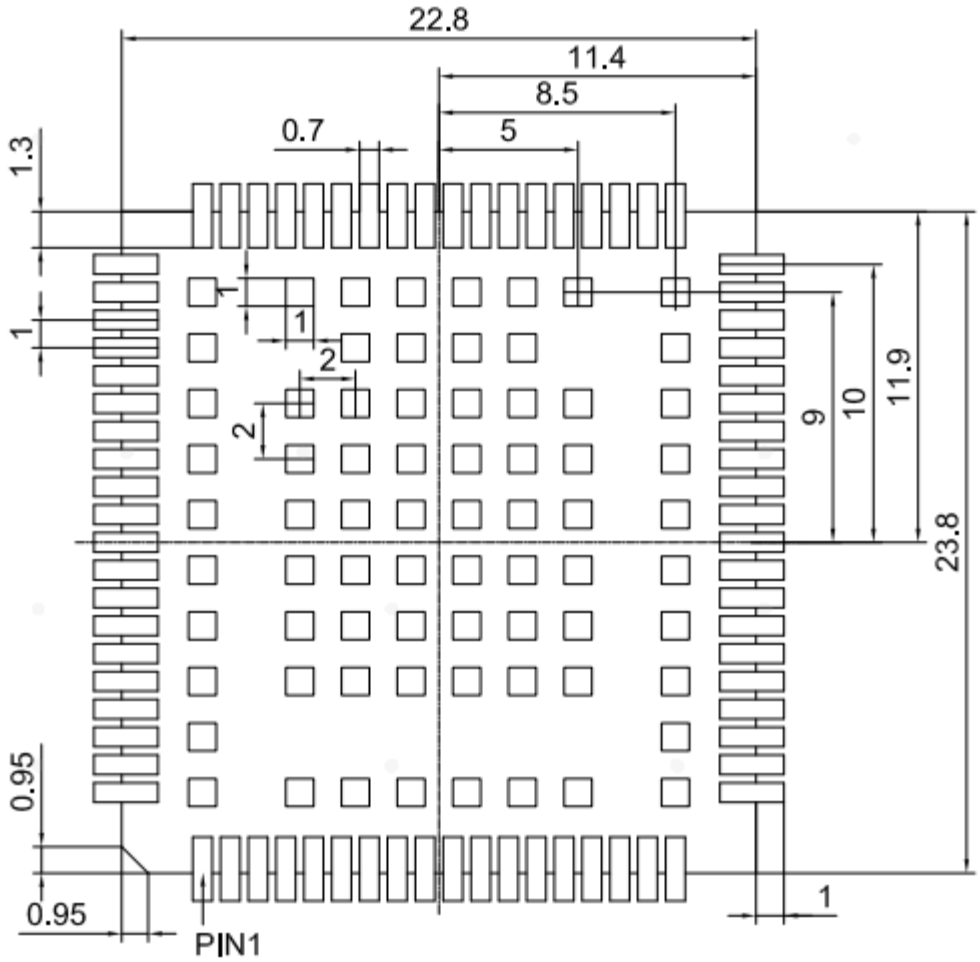


9.2 Application PCB Package

N715-EA adopts the 76-pin LCC + 72-pin LGA form package. The recommended application PCB package is as follows:

To achieve higher yield during module production, it is recommended that the distance between other components on the PCB board and the module pads be at least 3 mm to avoid the risk of tin connection when using stepped stencil.

Figure 9-2 N715-EA application PCB package (top view, unit: mm)



9.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

9.4 Solder Paste

The thickness of the solder paste and the flatness of the PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

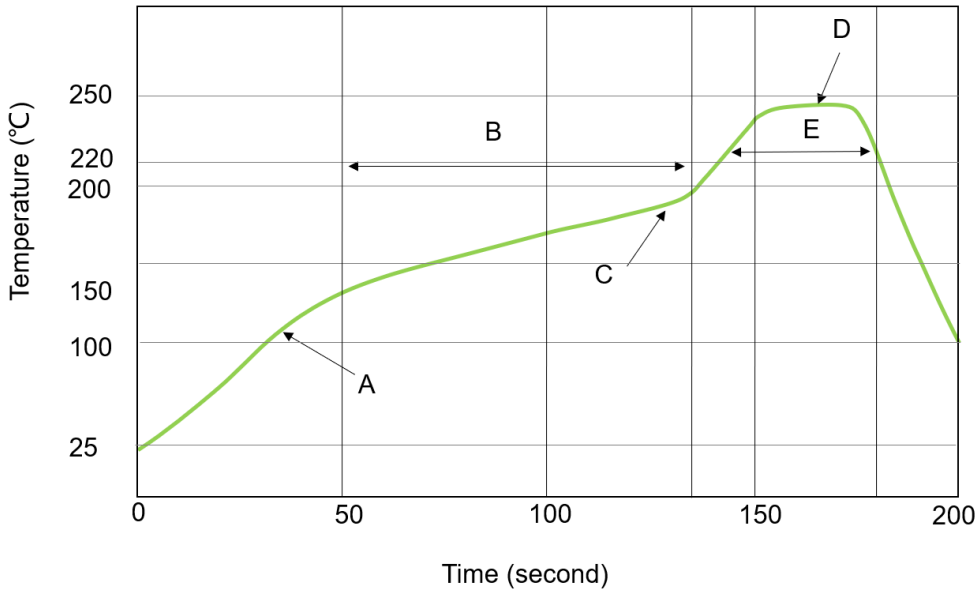
- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process parameters is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LCC/LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220°C for more than 45 seconds and the peak temperature reaches 240°C.

9.5 SMT Oven Temperature Profile

Neoway will not provide warranties for heat-responsive element abnormalities caused by improper temperature control.

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 9-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4°C/sec
- Ramp down rate: -3 to -1°C/sec
- Soak zone: 150 - 180°C, Time: 60 - 100s
- Reflow zone: >220°C, Time: 40 - 90s
- Peak temperature: 235 - 245°C

For information about cautions in storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 245°C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module at high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

A Abbreviations

Abbreviation	Full name
AI	Analog Input
AO	Analog Output
AIO	Analog Input /Output
ARM	Advanced RISC Machine
bps	Bits per Second
CCC	China Compulsory Certification
CTS	Clear to Send
DC	Direct Current
DI	Digital Input
B	Digital Input/Output
DL	Downlink
DO	Digital Output
DRX	Discontinuous Reception
DTR	Data Terminal Ready
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance
EVK	Evaluation Kit
FDD	Frequency Division Duplexing
FTP	File Transfer Protocol
FTPS	FTP Secure
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
EGSM	Enhanced GSM
3GPP	3rd Generation Partnership Project
IO	Input/Output
ISP	Image Signal Processor
LCC	Leadless Chip Carriers

LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
PCB	Printed Circuit Board
PCS	Personal Communications Service
PWM	Pulse Width Modulation
QVGA	Quarter Video Graphics Array
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
RTC	Real Time Clock
SPK	Speaker
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage

