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N58 Mini PCIe (Audio)

Hardware User Guide

Issue 1.1 Date 2021-05-17

Notice

This document provides a guide for users to use N58 Mini PCIe (Audio).

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to N58 Mini PCIe.

It defines the feature, indicators, and test standards of the N58 mini PCIe and provides a reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2020-05	Initial draft	Wu Wentao
1.1	2021-05	Deleted the SIM2 connector related content	Wu Yongqiang

Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

Related Documents

Neoway_N58 Mini PCIe (Audio)_ Product_Specifications

Neoway_N58_AT_Commands_Mannual

1 Introduction

N58 is an industrial 4G module that is developed on UNISOC chipset. Its dimensions are 30.0 mm x 28.0 mm x 2.6 mm. This high-performance cellular module supports GSM, LTE-FDD, LTE-TDD (Cat 1) network modes and provides various hardware interfaces. It facilitates the application development for customers and applies to various IoT communication devices such as AMR, POC, POS, etc.

N58 Mini PCIe is implemented on N58 and complies with PCI Express Mini Card 1.2 standard. It provides multiples functional interfaces to simplify customers' development. N58 Mini PCIe applies to various kinds of IoT communication devices such as video surveillance, laptops, in-vehicle devices, and wireless routers.

1.1 Overview

N58 Mini PCIe provides different hardware variants with the optional functions such as AUDIO and GNSS. You can choose one based on your demands. Table 1-1 lists the bands that each variant supports.

Table 1-1 Variant and frequency bands

Variant	Category	Band	GNSS[1]	CODEC
N58-CA	Cat1	FDD-LTE: B1, B3, B5, B8, TDD-LTE: B34, B39, B40, B41 GSM/GPRS: 900/1800 MHz	Optional	Supported
N58-EA	Cat1	FDD-LTE: B1, B3, B5, B7, B8, B20, B28 TDD-LTE: B38, B40, B41 GSM/GPRS: 900/1800 MHz	Optional	Supported
N58-LA	Cat1	FDD-LTE: B1, B2, B3, B4, B5, B7, B8, B28, B66 TDD-LTE: B38, B40, B41 GSM/GPRS: 850/900/1800/1900 MHz	Optional	Supported

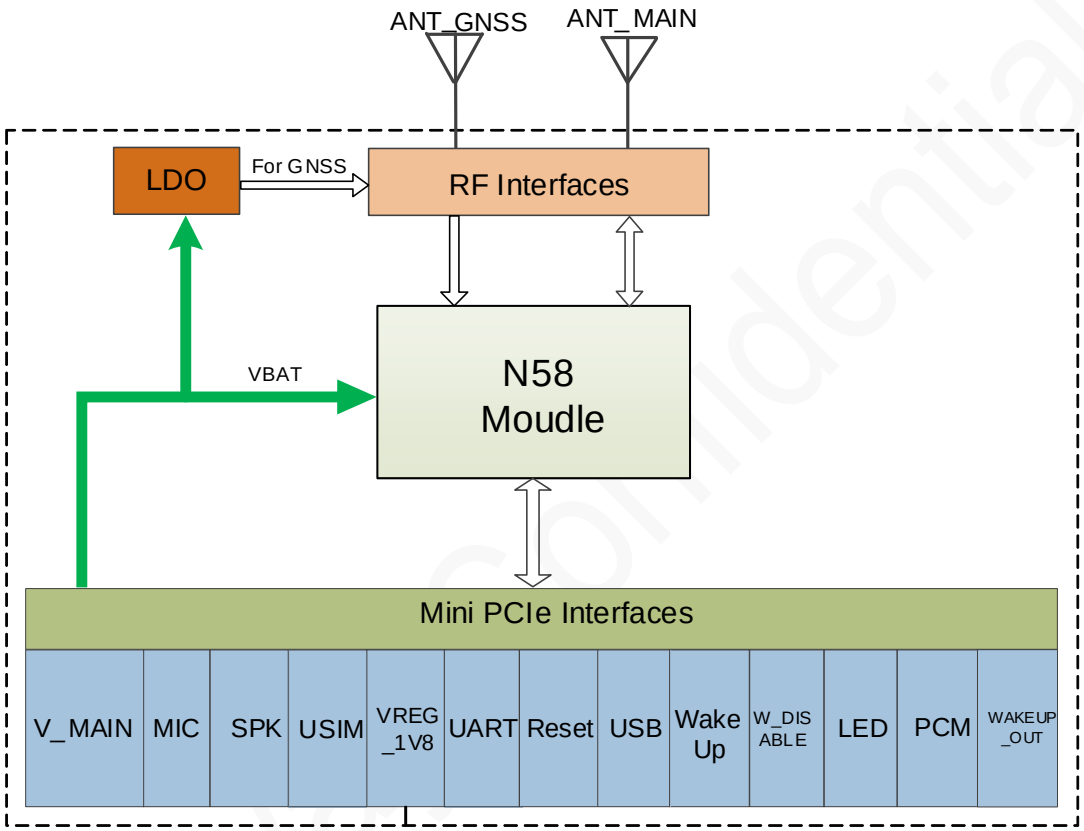
1.2 Block Diagram

N58 Mini PCIe consists of the following functionality modules:

[1]GNSS is optional for all above variants.

- N58 module
- Power management unit
- RF section
- Digital interfaces (USIM, PCM*, UART, USB, VREG_1V8, Wake up*, etc)
- Analog interfaces (MIC, SPK)

Figure 1-1 Block Diagram



* indicates functions that will be developed in the future.

LDO supplies 3.3V for external active GNSS antenna.

1.3 Basic Features

Parameter	Description
Dimensions	51.0 mm x 30.2 mm x 5.3 mm

Temperature ranges	Operating: -30°C to +75°C Extended: -35°C to +85°C Storage: -40°C to +90°C
Operating voltage	V_MAIN: 3.4 V to 4.2 V input, Typ. 3.8 V
	VREG_1V8: 1.8 V output, 50 mA at most
Operating current[2]	Sleep[3]<TBD
	Idle<TBD
	Operating mode (LTE networks) Current in data service: TBD Current in max. RX power: TBD
Processor	ARM Cortex-A5 processor, 500 MHz main frequency, 32KB L1 cache
Memory	RAM: 128 Mb ROM: 64 Mb
Band	See Table 1-1.
Wireless rate	GPRS: Max 85.6Kbps(DL) / Max 85.6Kbps(UL) FDD-LTE: Cat1, Max 10Mbps(DL)/Max 5Mbps(UL) TDD-LTE: Cat1, Max 8.96Mbps(DL)/Max2Mbps(UL)
Transmit power	GSM85c0:+33dBm (Power Class 4) EGSM900:+33dBm (Power Class 4) DCS1800:+30dBm (Power Class 1) PCS1900:+30dBm (Power Class 1) LTE:+23dBm (Power Class 3)
Application interfaces	2G/4G antenna, GNSS antenna 50 Ω impedance
	One UART interface, 2 Mbps
	One USIM interface, 1.8 V/3.0 V
	One USB2.0 high-speed interface
	One PCM interface*
	One WAKEUP_IN interface, used to control sleep mode of the module.
	One W_DISABLE interface, used to disable RF communication of the module.
	One WAKEUP_OUT interface, used to indicate whether the module is in sleep mode.
	One PON_RESET interface, used to reset the module.

[2] The table above only lists the operating currents of LTE band1 and band41, for the operating currents of the other network modes in different states, see the N58 Mini PCIe Current Test Report.

[3] Sleep mode needs to supported by software and hardware simultaneously.

	One network indicator control interface, used to control the network indicator.
	One MIC differential analog audio interface
	One SPK differential analog audio interface
AT Command	• 3GPP Release 13 • Neoway extended commands
Data	PPP, RNDIS, ECM
Protocol	TCP*, UDP*, MQTT, FTP/FTPS, HTTP/HTTP(S), SSL, TLS
Certification approval	CCC, SRRC, RoHS, CE

* indicates functions that will be supported in the future.

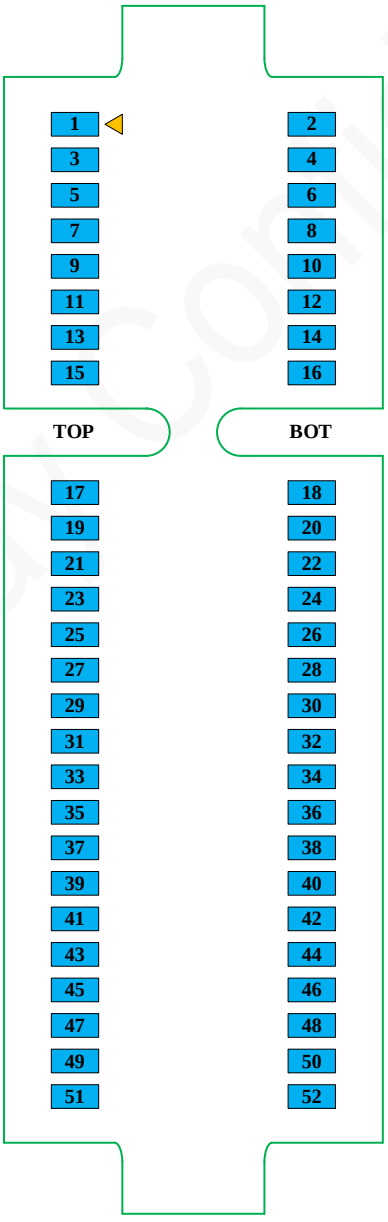
2 Module Pins

2.1 Pin Layout

N58 Mini PCIe provides 52 pins and their definitions meet the standard of Mini PCI Express. Figure 2-1 shows the pin definitions.

Figure 2-1 N58 Mini PCIe pin definition

Signal	Pin
MIC_P	1
MIC_N	3
SPK_P	5
SPK_N	7
GND	9
VREG_1V8	11
NC	13
GND	15
NC	17
WAKEUP_IN	19
GND	21
UART_RX	23
UART_RTS	25
GND	27
GND	29
UART_TX	31
PON_RESET	33
GND	35
GND	37
V_MAIN	39
V_MAIN	41
GND	43
PCM_CLK	45
PCM_DIN	47
PCM_DOUT	49
PCM_SYNC	51



Pin	Signal
2	V_MAIN
4	GND
6	NC
8	V_USIM
10	USIM_DATA
12	USIM_CLK
14	USIM_RST
16	NC
18	GND
20	W_DISABLE
22	PON_RESET
24	V_MAIN
26	GND
28	UART_CTS
30	NC
32	WAKEUP_OUT
34	GND
36	USB_D-
38	USB_D+
40	GND
42	LED_WWAN
44	USIM_DETECT
46	NC
48	NC
50	GND
52	V_MAIN

2.2 Pin Description

Table 2-1 lists the definition of IO types.

Table 2-1 IO definition

IO Type			
B	Digital input/output, COMS logic level		
DO	Digital output, COMS logic level		
DI	Digital input, COMS logic level		
OC	Open collector		
PO	Power output		
PI	Power supply input		
AO	Analog output		
AI	Analog input		
AIO	Analog input/output		
Level Feature			
P1	1.8V/3V	1.8V level feature: V_{IH}=1.26V~2.1V V_{IL}=-0.3V~0.36V V_{OH}=1.44V~1.8V V_{OL}=0V~0.4V	3.0V level feature VIH=2V~3.15V VIL=-0.3V~0.57V VOH=2.59V~2.96V
P3	1.8V digital IO	V_{IHmin}=1.2V V_{ILmax}= 0.3V V_{OHmin}=1.35V V_{OLmax}=0.45V	
P6	Voltage type of USB2.0 data interfaces	V_{min}=2.97V, V_{max}=3.5V, V_{typ}=3.08V	

Figure 2-2 Pin description

Signal	Pin	I/O	Function	Level Feature	Remarks
Power interface					
V_MAIN	2, 24, 39, 41, 52	PI	Main power supply input	V_{min}=3.4V V_{typ}=3.8V V_{max}=4.2V	Supply more than 3A current
VREG_1V8	11	PO	1.8V power output	V_{norm}=1.8V I_{max}=50mA	Used only for level shifting and IO power supply.

					Leave this pin floating if it is not used.
GND	4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50				Ensure that all GND pins are connected to the ground.
Control Interfaces					
PON_RESET	22, 33	DI	Module reset input		Triggered by a low level to reset the module.
WAKEUP_IN	19	DI	Sleep control input	P3	This pin function needs to be used together with AT commands.
UART interfaces					
UART_TX	31	DO	Data transmitting	P3	Max speed: 2 Mbps
UART_RX	23	DI	Data receiving	P3	Max speed: 2 Mbps
UART_CTS	28	DI	The customer enables the module to send data.	P3	Leave this pin floating if it is not used.
UART_RTS	25	DO	The module requests the customer to send data.	P3	Leave this pin floating if it is not used.
USIM interface					
V_USIM	8	PO	USIM power output	P1	1.8V/3.0V SIM cards are supported.
USIM_DATA	10	B	USIM data IO	P1	It should be connected to V_USIM through a 10 kΩ pull-up resistor.
USIM_CLK	12	DO	USIM clock output	P1	
USIM_RST	14	DO	USIM reset	P1	
USIM_DETECT	44	DI	USIM detect	P1	
USB interface					
USB_D-	36	AIO	USB data minus	P6	Route DM and DP signals in differential mode, and control impedance of 90Ω Leave this pin floating if it is not used.
USB_D+	38	AIO	USB data plus	P6	

Audio SPK interface					
SPK_P	5	AO	SPK signal positive		
SPK_N	7	AO	SPK signal negative		
Audio MIC interface					
MIC_P	1	AI	MIC signal positive		
MIC_N	3	AI	MIC signal negative		
PCM interface					
PCM_CLK	45	B	PCM clock signal	P3	In development
PCM_DIN	47	DI	PCM data input	P3	
PCM_DOUT	49	DO	PCM data output	P3	
PCM_SYNC	51	B	PCM frame synchronization signal	P3	
Other interfaces					
W_DISABLE	20	DI	Disable RF communication	P3	In development
WAKEUP_OUT	32	DO	Indicates whether the module is in sleep mode	P3	In development
LED_WWAN	42	OC	Network indicator control	P3	Leave this pin floating if it is not used.
Unused interface					
NC	6, 13, 16, 17, 30, 46, 48				Leave these pins floating.

3 Application Interfaces

N58 Mini PCIe provides power supply, control, communications, peripheral, audio, LCD, RF, and other interfaces to meet customers' requirements in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

3.1 Power Interface

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin	I/O	Function	Remarks
V_MAIN	2,24,39,41,52	PI	Main power supply input	3.4V to 4.2V (Typ. 3.8V)
VREG_1V8	11	PO	1.8V power output	V_{norm}=1.8V I_{max}=50 mA
GND	4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50			Ensure that all GND pins are connected to ground.

3.1.1 V_MAIN

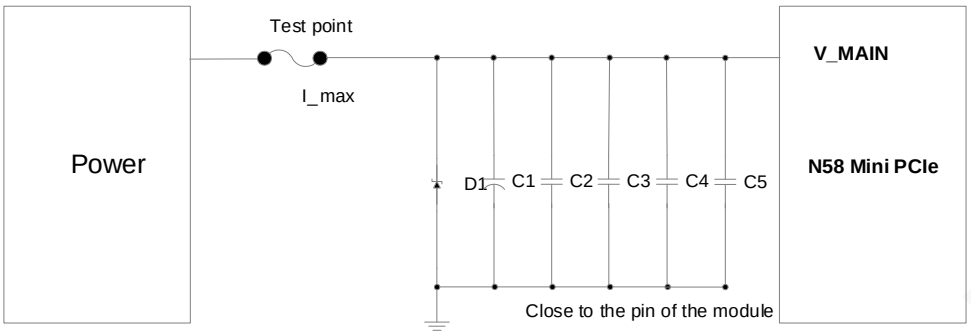
The power supply design covers two parts: schematic design and PCB layout.

Schematic Design

N58 Mini PCIe supports a power supply of 3.4 V to 4.2 V (3.8 V typically)

Figure 3-1 shows the schematic design recommended.

Figure 3-1 Recommended design 1



- The maximum input voltage for the module is 4.2 V and the typical value is 3.8 V. The recommended VBAT trace is wider than 3 mm on the PCB.
- TVS D1 with surge protection, VRWM=4.5 V, Ppp=2800 W. Place TVS close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- A large bypass aluminum capacitor (470 μF or 220 μF) or tantalum capacitor (220 μF or 100 μF) is expected at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be greater than 1.5 times the voltage across the power supply.
- Place a bypass capacitor of low-ESR close to the module to filter out high-frequency jamming from the power supply.

In GSM/GPRS mode, RF data is transmitted in burst mode that generates voltage drops on the power supply. Furthermore, this results in a 216 Hz TDD noise through the power and the transient peak current is larger than 3.0 A. Ensure low resistance of power supply trace in design to avoid voltage drop.

Never use a diode to make the drop voltage between a higher input and module power. Otherwise, Neoway will not provide a warranty for product issues caused by this. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, due to the forward voltage of the diode will vary greatly in different temperature and current. The module might not work properly with a diode power supply.)

3.1.2 VREG_1V8

N58 Mini PCIe provides one VREG_1V8 pin that outputs 1.8V@50mA.

VREG_1V8 is enabled automatically when the module is awake or in a running state.

It is recommended that VREG_1V8 is used for level shift only and an ESD protector should be reserved.

3.2 Control Interfaces

Signal	Pin	I/O	Function	Remarks
PON_RESET	22, 33	DI	Module reset input	Trigger by a low level
WAKEUP_IN	19	DI	Sleep mode input	Leave this pin floating if it is not used.

3.2.1 PON_RESET

PON_RESET is used to reset the module. When the module is working, inputting a negative pulse for more than 50 ms to RESET_N can trigger the reset process of the module. RESET_N is pulled up internally. Its typical high-level voltage is 3.3V. Leave this pin floating if not used.

If you use a 1.8V/2.8V/3.0V IO system, it is recommended to add a triode to separate it. Refer to the following designs. To reset the module through a high level, refer to Figure 3-3.

Figure 3-2 Reset control by button

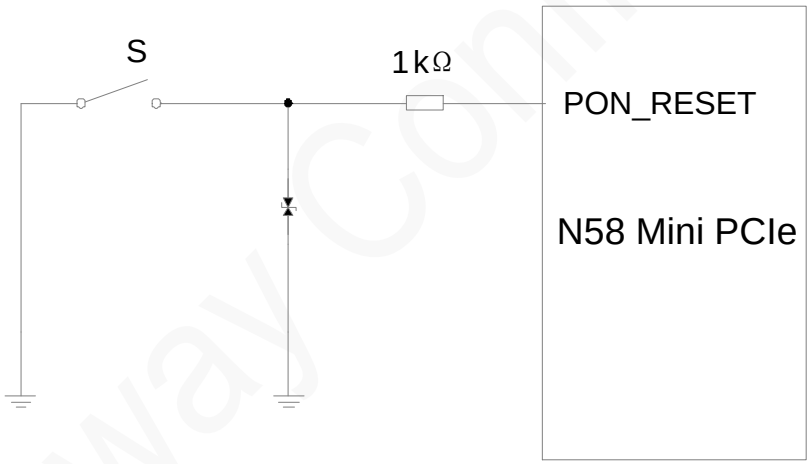
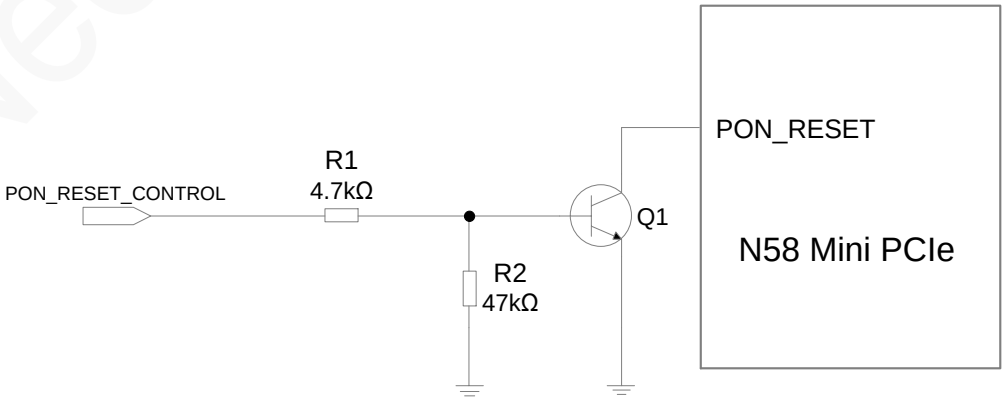
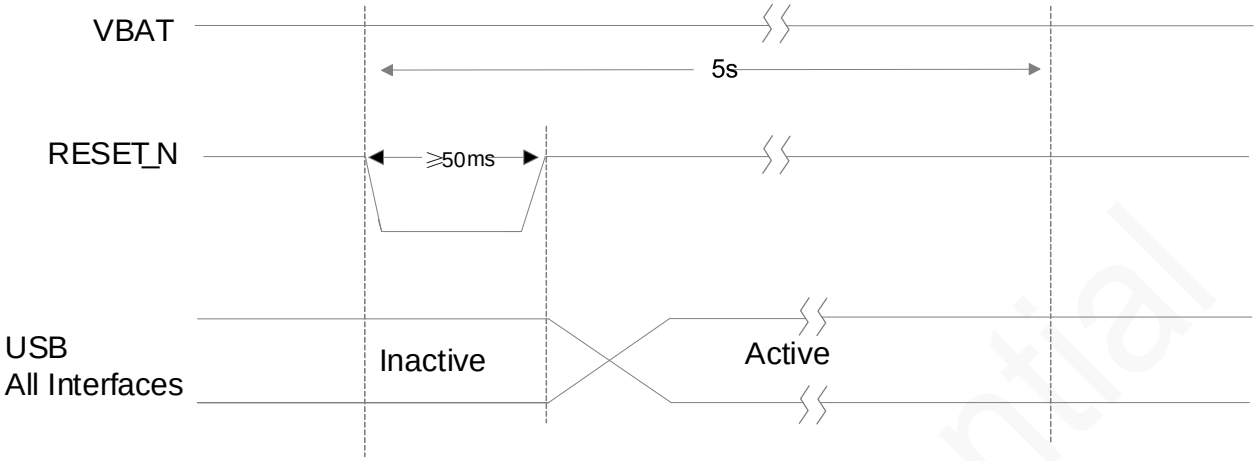


Figure 3-3 Reset circuit with triode separating



The following figure shows the reset process of N58 Mini PCIe.

Figure 3-4 N58 Mini PCIe reset process



3.2.2 WAKEUP_IN

The WAKEUP_IN pin is used to control sleep mode together with AT command.

Common sleep and wakeup functions are supported. You can set the function in software as required.

3.3 Peripheral Interfaces

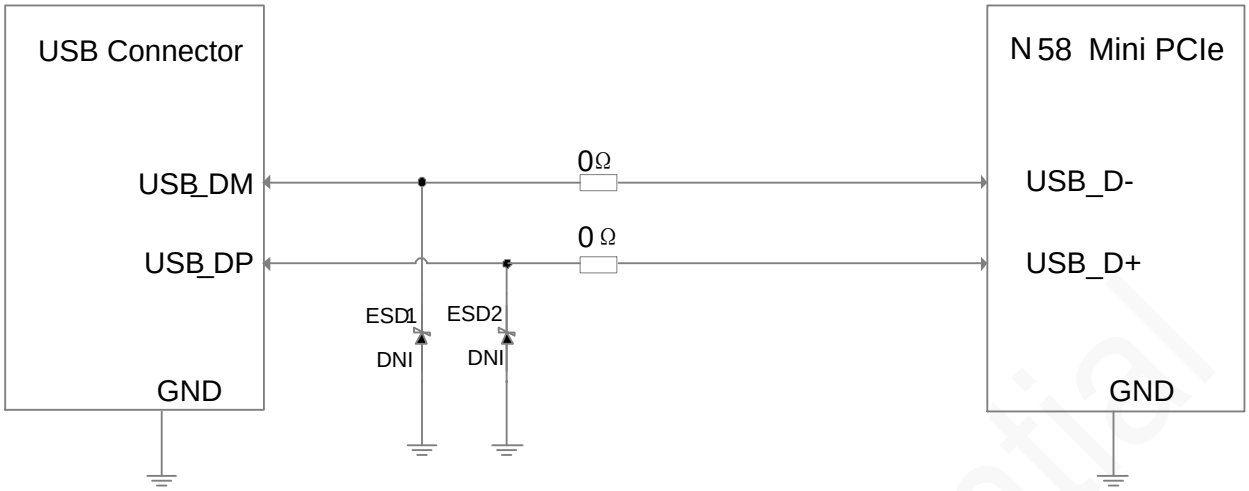
N58 Mini PCIe provides various peripheral interfaces.

3.3.1 USB

Signal	Pin	I/O	Function	Remarks
USB_D-	36	AIO	USB data minus	USB2.0, used for firmware download and data transmission. 90Ω impedance for differential traces.
USB_D+	38	AIO	USB data plus	

USB can be used to download firmware for N58 Mini PCIe and establish data communication for commissioning. The recommended USB circuit is shown in Figure 3-5.

Figure 3-5 USB connection



Schematic Design Guidelines

- Reserve positions on USB_D+ and USB_D for ESD protection diodes in design. You can determine whether to mount the dioxides according to your actual demands.

  The junction capacitance of the ESD protection diodes for USB_D+ and USB_D- should be lower than 0.5 pF.

- Reserve a resistor lower than 10Ω for USB_DP and USB_DM to improve the ESD performance.

PCB Design Guidelines

- Place the ESD diodes on USB_D+ and USB_D- lines as close to the USB connector as possible.
- USB data lines adopt differential trace design, in which the differential impedance should be limited to 90Ω. Isolate the USB traces from other signal traces by surrounding them with ground.

3.3.2 UART

In all the reference designs of this section, the signals of pins on the module are named in perspective of the module while peripheral pins are named from the view of the components. For example, UART_TXD indicates the pin that the module sends data while MCU_RXD indicates the pin that MCU receives data. These two pins should be connected.

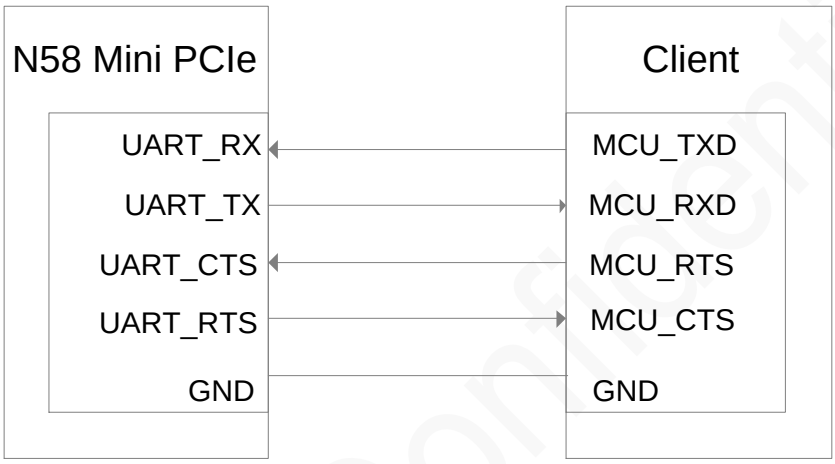
Please note the signal naming of pins on the components in peripheral selection and design.

Signal	Pin	I/O	Function	Remarks
UART_TX	31	DO	Data transmitting	1.8V power domain

UART_RX	23	DI	Data receiving	Leave these pins floating if they are not used.
UART_CTS	28	DI	Clear to send	
UART_RTS	25	DO	Request to send	

N58 Mini PCIe provides one UART interface that supports hardware flow control. This interface supports a speed of 2 Mbit/s at most and it operates at 1.8 V level.

Figure 3-6 UART connection

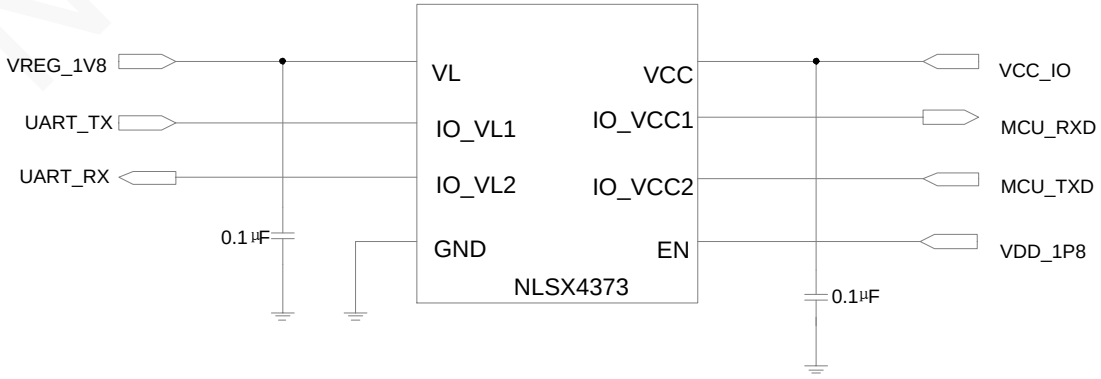


Schematic Design Guidelines

- Note the flow direction and match of signals.
- Leave the UART_CTS and UART_RTS pin floating if the hardware flow control is not used.

Level shift chip is recommended if the level of UART is higher than 1.8V. Figure 3-7 shows the reference design (if the hardware flow control is used, UART_CTS and UART_RTS are also needed to connect a level shift chip).

Figure 3-7 Recommended level shifting circuit 1



- NLSX4373 is a dual-supply level shifter, the rate of which can be up to 20 Mb/s.
- VL is the reference voltage of IO_VL1 and IO_VL2, ranging from 1.5V to 5.5V.
- VCC is the reference voltage of IO_VCC1 and IO_VCC2, ranging from 1.5V to 5.5V.
- For other details, see the specifications of NLSX4373.

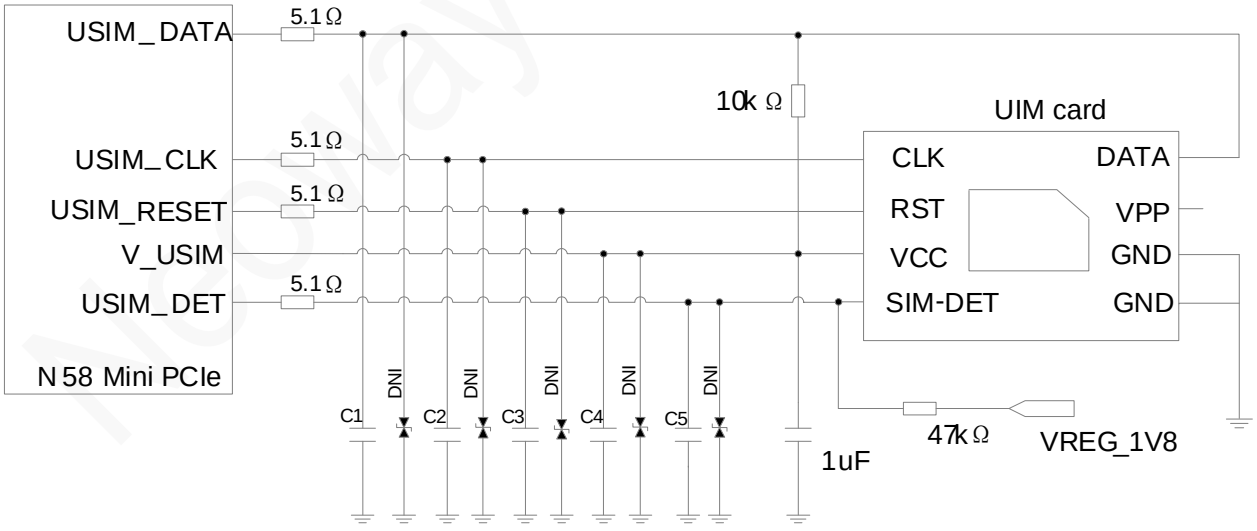
3.3.3 USIM

Signal	Pin	I/O	Function	Remarks
V_USIM	8	PO	USIM power output	Compatible with 1.8 V/3.0 V level
USIM_DATA	10	B	USIM data IO	It should be connected to V_USIM through a 10 kΩ pull-up resistor.
USIM_CLK	12	DO	USIM clock output	
USIM_RST	14	DO	USIM reset	
USIM_DETECT	44	DI	USIM detect	

N58 Mini PCIe supports 1.8 V/3.0 V USIM card. The circuit internally connects the other USIM interface of the N58 Mini PCIe.

N58 Mini PCIe supports dual SIM single standby. The USIM interface with slot is preferential by default. Figure 3-8 shows the reference design of the USIM card interface.

Figure 3-8 Reference design of USIM card interface



Schematic Design Guidelines

- V_USIM is the pin to supply power for the USIM card and its maximum load is 50 mA. Do NOT use it for any other purpose.
- Add a pull-up resistor externally in design since the USIM_DATA pin is not pulled up internally.
- Reserve a position for the ESD protection diode (junction capacitance lower than 10 pF) in every signal line. Although the USIM embeds ESD components internally, ESD standards might vary with products.
- Reserve a capacitor in each signal line to filter high-frequency noise. The capacitors are 33 pF by default.
- Connect a 10 Ω resistor respectively to USIM_DATA, USIM_RESET, USIM_CLK, and USIM_DET in series to enhance the ESD performance.
- N58 Mini PCIe supports USIM card detection. USIM_DET is a 1.8V interrupt pin. The USIM detection circuit works by checking the levels across the USIM_DET pin before and after a USIM card is inserted. In the reference circuit, SIM-DET is not connected before a USIM card is inserted and is grounded after a USIM card is inserted. Low level means USIM card detected while high level means no USIM card detected.

PCB Design Guidelines

- USIM signals are like to be jammed by RF radiation, resulting in failure to detect the SIM card. Place USIM far away from RF circuits.
- Place the USIM card closed to the module and USIM traces should be as short as possible.
- Place ESD protection resistors and components close to the USIM card.
- Surround USIM traces with ground to enhance EMC.

3.4 Audio Interface

N58 Mini PCIe provides different audio input/output interfaces to meet your demands for the audio function.

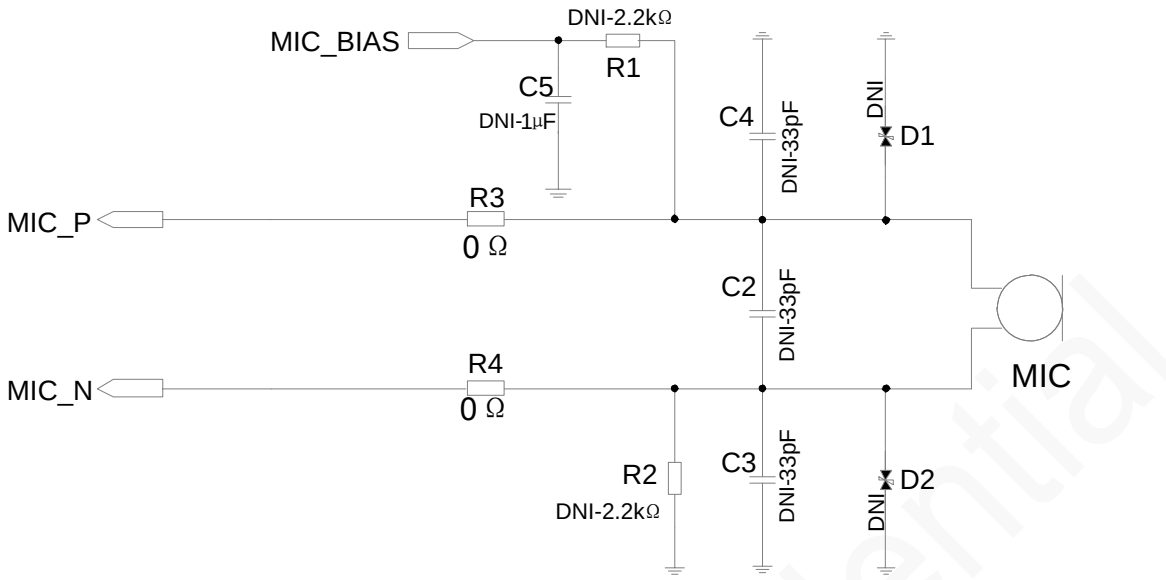
3.4.1 Analog Audio Input Interfaces

Signal	Pin	I/O	Function	Remarks
MIC1_P	1	AI	MIC input positive	Embeds bias internally
MIC1_N	3	AI	MIC input negative	

N58 Mini PCIe supports one diffrerential MIC input. It embeds a MIC_BIAS internally and you do not have to add one. You can reserve a bias and filter network in your design.

Figure 3-9 shows the recommended MIC circuit.

Figure 3-9 Reference design of differential MIC input



Schematic Design Guidelines

- Reserve D1 and D2 for ESD components that prevent the MIC from introducing static electricity and damaging the module.
- Reserve C2, C3, C4, and C5 for four capacitors that are mainly used to filter out interference signals. You can determine whether to mount the capacitors according to the debugging results.
- Reserve R1 and C5 for the bias components.
- Reserve 0Ω resistors at R2 and R4 to deal with noise interference and ESD problems in the circuit. Adjust them according to the debugging results.
- Reserve the positions that are marked with DNI and do not mount any components.
- For the selection of the bias voltage of MIC_BIAS, refer to the MIC data manual.
- It is recommended to select an electret MIC that embeds dual capacitors (e.g. 10 pF and 33 pF) to reduce TDD noise.

  If you select other MIC components, confirm with Neoway FAE.

PCB Design Guidelines

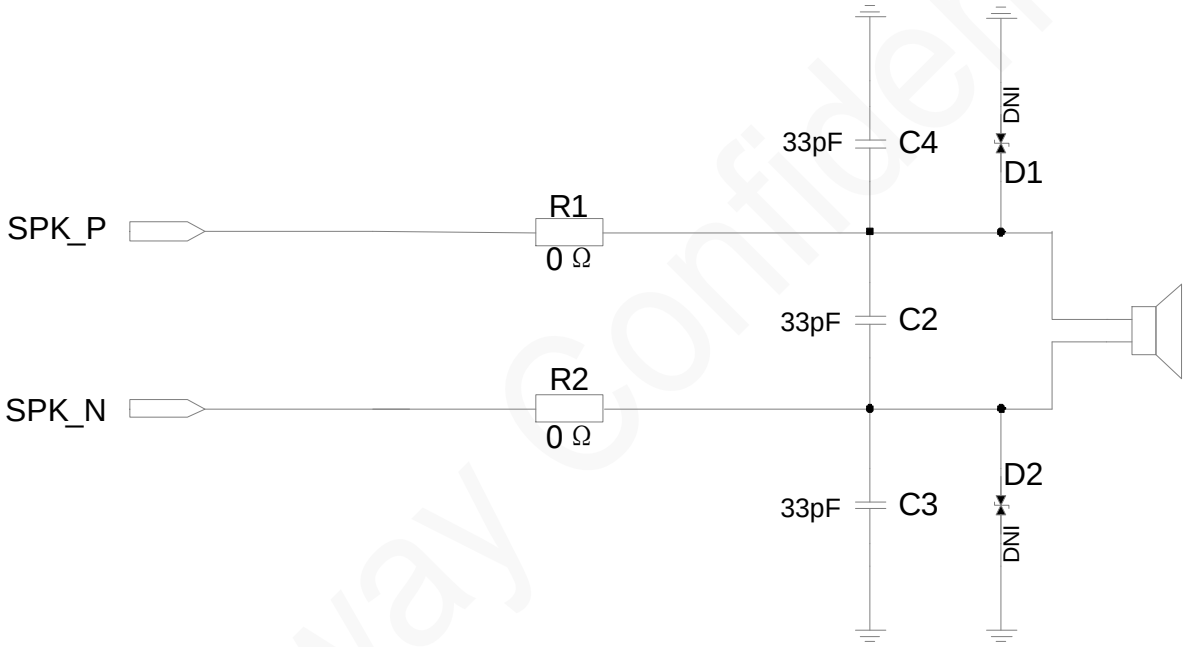
- MIC_P and MIC_N traces should be routed in differential mode.
- Surround the traces with ground plane. Keep them 3 times trace width away from other signal traces.
- Place the ESD devices as close as possible to the MIC component or interface.
- Keep the MIC_P and MIC_N traces far away from interference sources such as the DC-DC power supply.

3.4.2 Analog Audio Output Interfaces

Signal	Pin	I/O	Function
SPK_P	5	AO	Speaker output positive
SPK_N	7	AO	Speaker output negative

The speaker interface is a differential output. When the VBAT is supplied 4.2V, the embedded Class D amplifier delivers 800 mW into 8Ω and the Class AB amplifier delivers 600 mW into 8Ω. It supports over burst protection and noise suppression.

Figure 3-10 Schematic of differential SPK output



Schematic Design Guidelines

- C2, C3, and C4 are used to filter the RF interference.
- Reserve D1 and D2 for the ESD components that prevent the APK from introducing static electricity and damaging the module.
- Reserve 0 Ω resistors at R1 and R2 to deal with noise interference and ESD problems in the circuit. Adjust them according to the debugging results.

PCB Design Guidelines

- The audio signal traces should be wide enough on the PCB to bear large current when audios are output at the highest volume. Isolate the traces from digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough grounding holes and ground protection.

- Keep audio traces far away from the antenna to reduce jamming.

  Avoid parallel layout between power traces and audio traces.

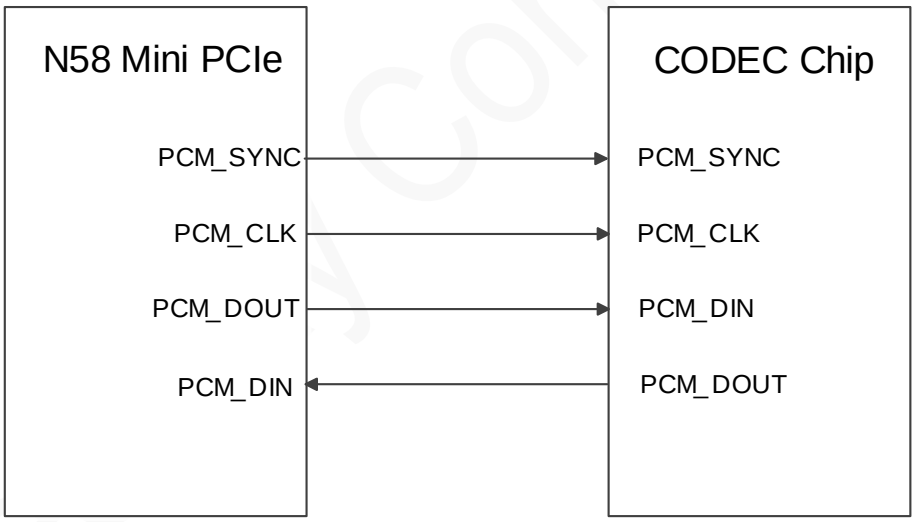
- Comply with differential rules.

3.5 PCM Interface

N58 Mini PCIe provides one PCM interface. This function is in development. The reference high level of the interface is 1.8V.

Signal	Pin	I/O	Function	Remarks
PCM_CLK	45	IO	PCM clock signal	The PCM function is in development.
PCM_DIN	47	DI	PCM data input	
PCM_DOUT	49	DO	PCM data output	
PCM_SYNC	51	IO	PCM frame synchronization signal.	

Figure 3-11 PCM connection



3.6 Other Functional Interfaces

Signal	Pin	I/O	Function	Remarks
W_DISABLE	20	DI	Disable RF communication	In development
WAKEUP_OUT	32	DO	Used to indicate the sleep status of the module	In development
LED_WWAN	42	OC	Network status indicator	

control

3.6.1 W_DISABLE

The W_DISABLE pin supports 1.8 V. It is used to control the RF communication function (flight mode). This function is in development.

When W_DISABLE detects a low level, the module enters flight mode. When it detects a high level, the module exits from the fight mode.

3.6.2 WAKEUP_OUT

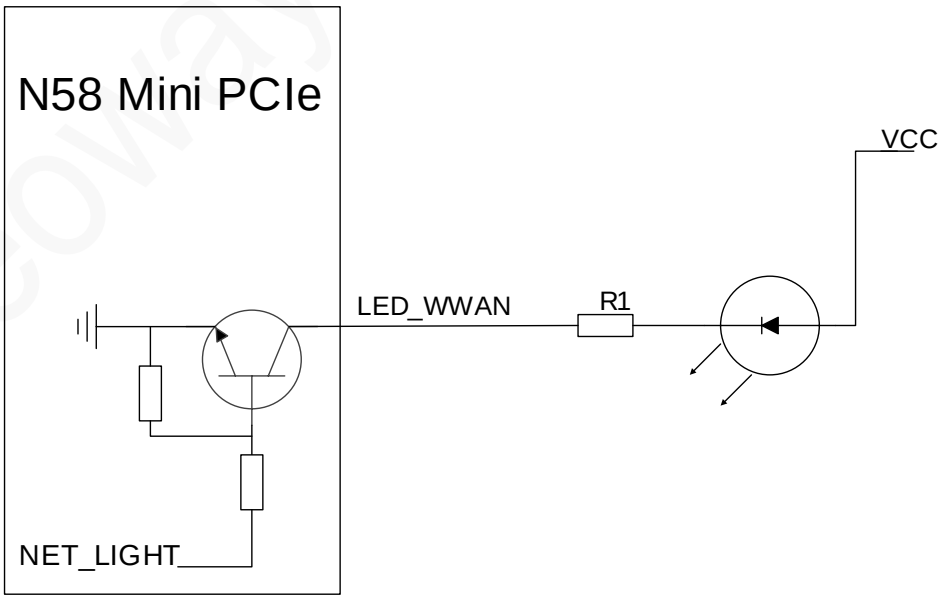
The WAKEUP_OUT pin supports 1.8V. It is used to indicate whether the module is in sleep mode. This function is in development.

When WAKEUP_OUT outputs a high level, the module is awake. When it outputs a low level, the module is in sleep mode.

3.6.3 LED_WWAN

The LED_WWAN pin is used to control the network status indicator. It is designed as an open-collector gate (OC). When it connects an LED indicator, a current limiting resistor need to be connected in series with the indicator. Adjust the resistance of R1 according to LED brightness. When LED_WWAN outputs a low level, the LED indicator lights on. Figure 3-12 shows the reference design of LED_WWAN.

Figure 3-12 LED_WWAN reference design



3.7 Antenna Interface

N58 Mini PCIe provides two antenna interfaces. They are 2G/3G/4G main antenna and GNSS antenna. Figure 3-13 shows their positions on the PCIe module.

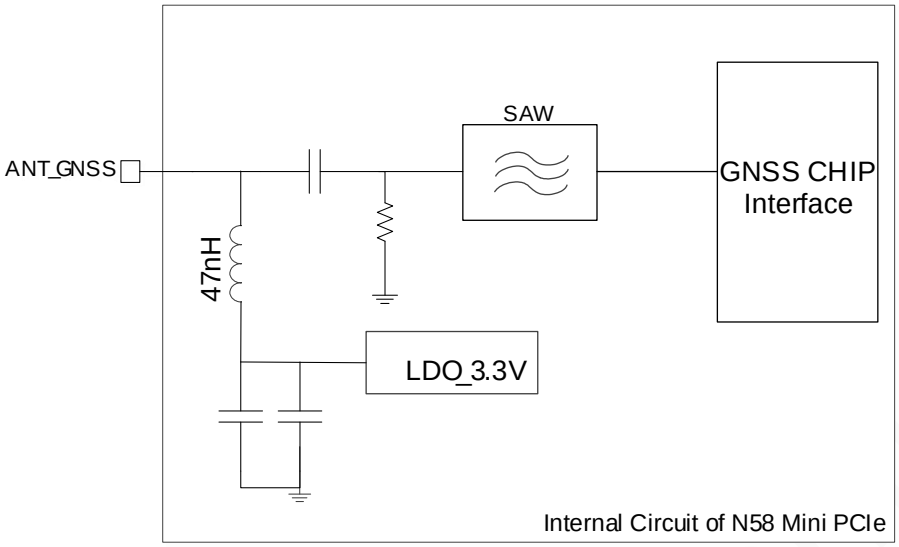
Figure 3-13 N58 Mini PCIe antenna interface

Antennas connecting to the module must comply with mobile device standards. The VSWR ranges from 1.1 to 1.5 and the input 50 Ω. The antennas should be well matched to achieve the best performance in different application scenarios.

Antenna interfaces can be connected to a rubber ducky antenna, magnet antenna, or embedded Planar Inverted F Antenna (PIFA). Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.GNSS Antenna

Figure 3-14 shows the circuit of GNSS RF inside the N58 Mini PCIe module.

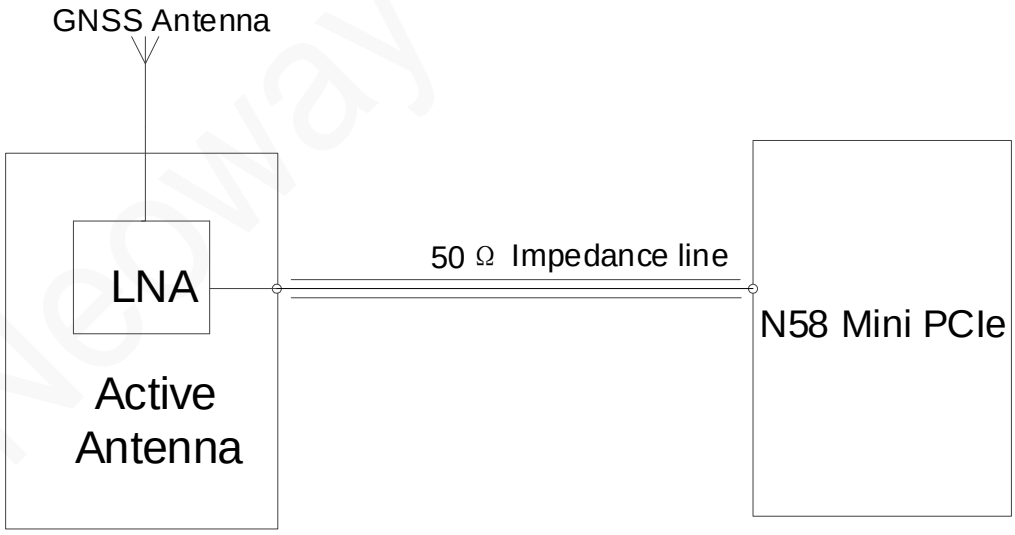
Figure 3-14 Internal GNSS RF circuit



If the GNSS signal is poor, the electric signal converted will be very poor and easy to be interfered. Therefore, an active antenna is a must. The active GNSS antenna amplifies the signal it receives through its internal LNA and then transmit the signal to the internal IC through the feeder.

The N58 Mini PCIe module supplies 3.3 V for the active antenna internally and connects to it through a 47 nH inductor. The GNSS antenna can be an active ceramic antenna.

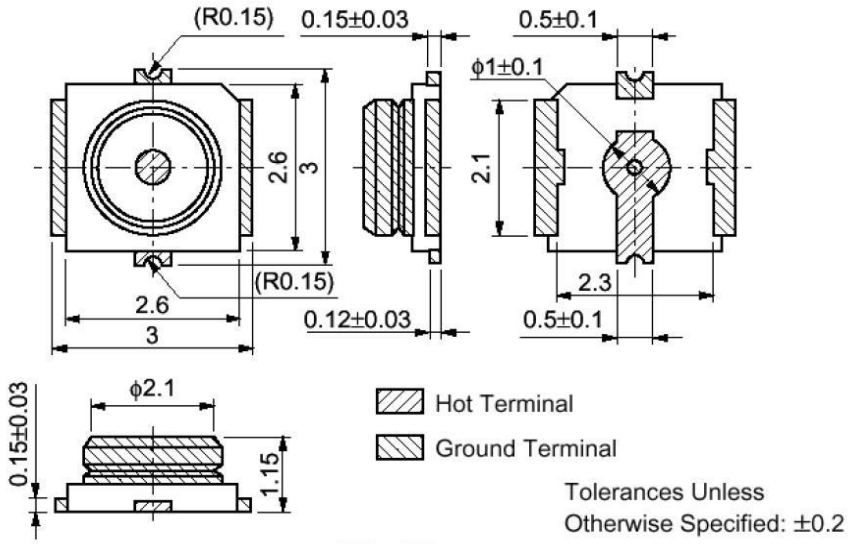
Figure 3-15 Active antenna connection



3.8 RF Connector

To adopt RF antenna connections, the GSC RF connector MM9329-2700RA1 from Murata is recommended. Figure 3-16 shows the encapsulation specifications.

Figure 3-16 Encapsulation specifications of Murata RF connector



4 Electric Feature and Reliability

This chapter describes the electric features and reliability of N58, including the current and voltage of each power pin, operating and storage temperature ranges, and ESD protection features.

4.1 Electric Features

Table 4-1 Operating conditions of N58 Mini PCIe

Pin	Parameter	Minimum Value	Typical Value	Maximum Value
V_MAIN	V_{in}	3.4 V	3.8 V	4.2 V
	I_{in}	/	/	3.0 A

If the voltage is lower than the threshold, the module might fail to start. If the voltage is higher than the threshold or there is a voltage burst during the startup, the module might be damaged permanently.

If you use LDO or DC-DC to supply power for the module, ensure that it outputs at least 3.0 A current.

Table 4-2 Current consumption of N58 Mini PCIe (Typical)

State / Frequency band	PSM/Sleep (mA)	Idle (DRX/eDRX) (mA)	Active power (mA)@max
FDD-LTE: B1, B2, B3, B4, B5, B7, B8, B20, B28, B66	TBD	TBD	TBD
TDD-LTE: B34, B38, B39, B40, B41	TBD	TBD	TBD
GSM 900/850	TBD	TBD	TBD
GSM1800/1900	TBD	TBD	TBD

4.2 Temperature Features

Table 4-3 Temperature feature of N58 Mini PCIe

Status	Minimum Value	Typical Value	Maximum Value
Operating	-30°C	25°C	75°C
Extended	-35°C	25°C	85°C
Storage	-40°C	25°C	90°C

If the module works in an environment of -30°C to -35°C or 75°C to 85°C, RF performance might be beyond the requirements of 3GPP. This does not affect the running of the module. The RF performance will meet the 3GPP standard after the temperature reaches the operating range.

4.3 ESD Protection

Electronics need to pass ESD tests. The following table shows the ESD capability of key pins of this module. It is recommended to add ESD protection based on the application scenarios to ensure product quality when designing a product.

Humidity 45% Temperature 25°C

Table 4-4 N58 Mini PCIe ESD protection

Testing Point	Contact Discharge	Air Discharge
V_MAIN	±8 kV	±15 kV
GND	±8 kV	±15 kV
ANT	±8 kV	±15 kV
Cover	±8 kV	±15 kV
Others	±2 kV	±4 kV

5 RF Features

N58 supports network modes including GSM, FDD-LTE, TDD-LTE(Cat 1), and optionally supports GNSS. This chapter describes the RF features of N58.

5.1 Operating Bands

Table 5-1 Operating bands of N58 Mini PCIe

Operating band	Uplink	Downlink
GSM850	824~849 MHz	869~894 MHz
EGSM900	880~915 MHz	925~960 MHz
DCS1800	1710~1785 MHz	1805~1880 MHz
PCS1900	1850~1910 MHz	1930~1990 MHz
FDD-LTEB1	1920~1980 MHz	2110~2170 MHz
FDD-LTEB2	1850~1910 MHz	1930~1990 MHz
FDD-LTEB3	1710~1785 MHz	1805~1880 MHz
FDD-LTEB4	1710~1755 MHz	2110~2155 MHz
FDD-LTEB5	824~849 MHz	869~894 MHz
FDD-LTEB7	2500~2570 MHz	2620~2690 MHz
FDD-LTEB8	880~915 MHz	925~960 MHz
FDD-LTEB20	832~862 MHz	791~821 MHz
FDD-LTEB28	703~748 MHz	758~803 MHz
FDD-LTEB66	1710~1780 MHz	2110~2200 MHz
TDD-LTEB34	2010-2025 MHz	2010-2025 MHz
TDD-LTEB38	2570~2620 MHz	2570~2620 MHz
TDD-LTEB39	1880~1920 MHz	1880~1920 MHz
TDD-LTEB40	2300~2400 MHz	2300~2400 MHz
TDD-LTEB41	2555~2655 MHz	2555~2655 MHz

5.2 TX Power and RX Sensitivity

Table 5-2 RF TX power of N58 Mini PCIe

Band	Max Power	Min. Power
GSM850	33 dBm+2/-2 dB	5 dBm+2/-2 dB
EGSM900	33 dBm+2/-2 dB	5 dBm+2/-2 dB
DCS1800	30 dBm+2/-2 dB	0 dBm+2/-2 dB
PCS1900	30 dBm+2/-2 dB	0 dBm+2/-2 dB
FDD-LTEB1	23 dBm+2/-2 dB	<-40 dBm
FDD-LTEB2	23 dBm+2/-2 dB	<-40 dBm
FDD-LTEB3	23 dBm+2/-2 dB	<-40 dBm
FDD-LTEB4	23 dBm+2/-2 dB	<-40 dBm
FDD-LTEB5	23 dBm+2/-2 dB	<-40 dBm
FDD-LTE B7	23 dBm+2/-2 dB	<-40 dBm
FDD-LTEB8	23 dBm+2/-2 dB	<-40 dBm
FDD-LTE B20	23 dBm+2/-2 dB	<-40 dBm
FDD-LTE B28	23 dBm+2/-2 dB	<-40 dBm
FDD-LTEB66	23 dBm+2/-2 dB	<-40 dBm
TDD-LTEB34	23 dBm+2/-2 dB	<-40 dBm
TDD-LTEB38	23 dBm+2/-2 dB	<-40 dBm
TDD-LTE B39	23 dBm+2/-2 dB	<-40 dBm
TDD-LTE B40	23 dBm+2/-2 dB	<-40 dBm
TDD-LTE B41	23 dBm+2/-2 dB	<-40 dBm

Table 5-3 N58 Mini PCIe GSM RX sensitivity

Band	Sensitivity
GSM850	≤-108 dBm
EGSM900	≤-108 dBm
DCS1800	≤-108 dBm
PCS1800	≤-108 dBm

Table 5-4 N58 Mini PCIe LTE RX sensitivity

Band	Sensitivity
LTE-FDD B1	≤-96 dBm
LTE-FDD B2	≤-96 dBm
LTE-FDD B3	≤-96 dBm
LTE-FDD B4	≤-96 dBm
LTE-FDD B5	≤-96 dBm
LTE-FDD B7	≤-95 dBm
LTE-FDD B8	≤-96 dBm
LTE-FDD B20	≤-96 dBm
LTE-FDD B28	≤-96 dBm
LTE-FDD B66	≤-96 dBm
LTE-TDD B34	≤-96 dBm
LTE-TDD B38	≤-96 dBm
LTE-TDD B39	≤-96 dBm
LTE-TDD B40	≤-96 dBm
LTE-TDD B41	≤-96 dBm

All values above were obtained in the lab. In actual applications, there might be a difference because of network environments.

5.3 GNSS Features

Table 5-5 GNSS Feature

Parameter	Value
GPS L1 operating frequency	1575.42±1.023 MHz
GLONASS operating frequency	1597.5~1605.9 MHz
BDS operating frequency	1559.1~1563.1 MHz
Tracking sensitivity	-161 dBm
Acquisition sensitivity	-147 dBm
Positioning precision (in air)	< 3m (CEP50)

Hot start (in air)	<2.0s
Cold start (in air)	<35s
Update frequency	<10 Hz
CNRin/CNRout	3 dB
Max. positioning altitude	TBD
Max. positioning speed	TBD
Max. positioning acceleration	TBD
GNSS data type	NMEA-0183
GNSS antenna type	aActive antenna

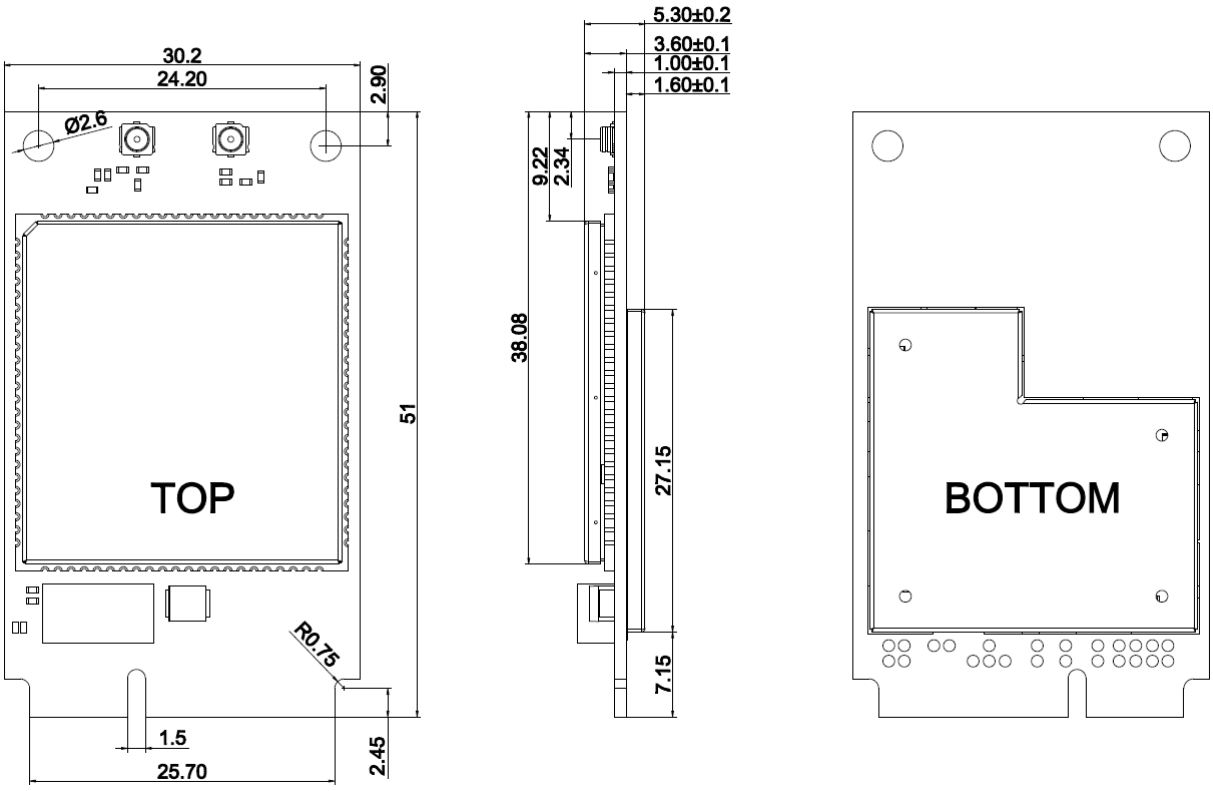
6 Mechanical Features

This chapter describes the mechanical features of N58.

6.1 Dimensions

Specifications	N58 Mini PCIe
Dimensions	51.0 ± 0.1 mm x 30.2 ± 0.1 mm 5.3 ± 0.15 mm (H*W*D)
Weight	TBD
Packaging	52-Pin Mini PCIe

Figure 6-1 N58 Mini PCIe dimensions (Unit: mm)



6.2 Label

The label information is laser carvevd on the cover of the N58 module. The following figure shows the label of N58.

Figure 6-2 N58 label

- The picture above is only for reference.
- The silk-screen printing must be clear. No blur is allowed.
- The material and surface finishing must comply with RoHS directives.

6.3 Packing

N58 Mini PCIe modules are packed in sealed bags on delivery to guarantee a long shelf life. Follow the same package of the modules again in case of opened for any reason.

Figure 6-3 Packaging process

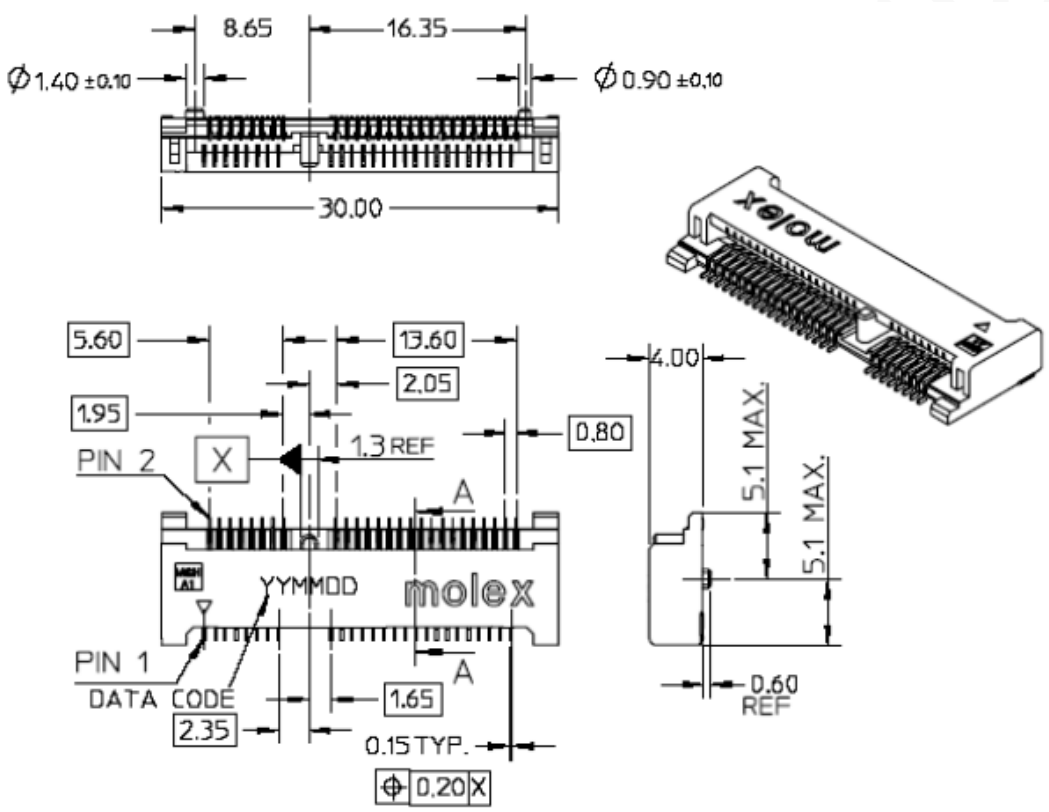
6.4 Storage

- Temperature: 20°C to +26°C
- Humility: 40% to 60%
- Period: 120 days

7 Mounting

N58 Mini PCIe adopts the standard PCI Express Mini Card 1.2 interfaces and can be mounted to a Mini PCIe connector. It is recommended to use 679100002 from Molex. The following figure shows its dimensions.

Figure 7-1 Mini PCIe connector



8 Safety Recommendations

Ensure that this product is used compliant with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or workplace:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, etc.
- Do not use this product in environments such as hospitals or airplanes where it might interfere with other electronic equipment.

Please follow the requirements below in application design:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Please design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Please connect the product to a stable power supply and route traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not remove the USIM card in idle mode if the module does not support hot-plugging.

A Abbreviation

Abbreviation	English Full Name
ADC	Analog-Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AI	Analog Input
AMR	Acknowledged multirate (speech coder)
AO	Analog Output
AP	Access Point
ARM	Advanced RISC Machine
BDS	The BeiDou Navigation Satellite System
BOM	Bill of Material
BT	Bluetooth
CCC	China Compulsory Certification
CEP	Circular Error Probable
CNR	Carrier to Noise Rate
CPU	Central Processing Unit
CS	Chip Select
CTS	Clear to Send
DC	Direct Current
DCS	Digital Cellular System
DI	Digital Input
DIO	Digital Input/Output
DL	Downlink
DO	Digital Output
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DRX	Discontinuous Reception
DTR	Data Terminal Ready

ECM	Ethernet Control Model
eDRX	Extended DRX
EGSM	Enhanced GSM
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance
EVK	Evaluation Kit
FCC	Federal Communications Commission
FDD	Frequency Division Duplexing
FPC	Flexible Printed Circuit
FTP	File Transfer Protocol
FTPS	FTP Secure
GFSK	Gauss frequency Shift Keying
GLONASS	GLOBAL NAVIGATION SATELLITE SYSTEM
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
3GPP	3rd Generation Partnership Project
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
IO	Input/Output
ISP	Image Signal Processor
LCC	Leadless Chip Carriers
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCLK	Main Clock
MCU	Microcontroller Unit
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PCS	Personal Communications Service
PWM	Pulse Width Modulation

QVGA	Quarter Video Graphics Array
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDD	Time Division Duplex
UART	Universal asynchronous receiver-transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Networks