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N58

Hardware User Guide

LTE Cat.1 Module
Issue 2.8
Date 2023-03-16

Notice

This document provides a guide for users to use N58.

This document is intended for system engineers (SEs), development engineers, and test engineers.

THIS GUIDE PROVIDES INSTRUCTIONS FOR CUSTOMERS TO DESIGN THEIR APPLICATIONS. PLEASE FOLLOW THE RULES AND PARAMETERS IN THIS GUIDE TO DESIGN AND COMMISSION. NEOWAY WILL NOT TAKE ANY RESPONSIBILITY OF BODILY HURT OR ASSET LOSS CAUSED BY IMPROPER OPERATIONS.

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Sales@neoway.com

Support@neoway.com

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Contents

Figures

Tables

About This Document

Scope

This document is applicable to the N58 series. It describes N58 information and functional interface characteristics, and provides a reference design for each functional interface.

The reference design in this document is for reference only, and user applications must be designed according to actual scenarios and conditions. If you have any questions, please contact Neoway FAEs.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Author
1.0	2019-11	Initial release.	Zhang Gang
2.0	2020-05	• Changed the definitions of pins 13, 78, 80, and 83. • Updated the GNSS characteristics and added the support for BDS. • Updated the frequency bands of EA and LA variants. • Added the 1PPS pin description of the N58 module with the GNSS function. • Updated the MIC-related design description.	Zhang Gang
2.1	2020-07	Updated the figure of N58 dimensions and adjusted the direction of the PCB package figure.	Liu Pengbin
2.2	2020-08	• Updated the ADC voltage detection range. • Updated the DC characteristics description P3 and the 1.8V digital IO voltage type. • Added the description of VBAT Vmin and Vnorm. • Updated the DC characteristics description of RESET_N and PWRKEY_N pins. • Updated the function of the UART1 interface. This interface is disabled after the BT function is enabled. • Updated the DC characteristics description of	Walter Wu

		USIM1_DET and USIM2_DET pins. • Updated the SDIO reference design. • Updated the resistance value of the pull-up resistor of the 12C bus. • Deleted the UART level shifting circuit. • Updated the power supply range of VRTC_GPS. • Updated the anode power supply range of LED_K. • Changed the PWRKEY_N startup time to be greater than 1.8s and less than 3s. • Updated the description and function definitions of PSM_WAKEUP. • Updated the voltage domain of the LCD and SDIO interfaces.	
2.3	2020-11	• Updated the RING pin description and figures. • Updated the UART1 interface description. • Updated the PSM_WAKEUP description and deleted the DTR description.	Walter Wu
2.4	2021-06	• Updated the USB pin name in Figure 4-1 (that is, "HS" is removed). • Updated the recommended circuit of a USIM card to explain the handling method of the USIM_DET pin when a user uses hot plug or does not use hot plug. • Deleted the description of "adaptive" because an SD card does not support adaptive 1.8 V and 3.0 V (configured based on the software version). • Updated the dimensions figure and added the "PIN1" identifier. • Changed the maximum drive current of the RGB LED to 50 mA.	Wu Yongqiang
2.5	2021-09	• Updated the variants, frequency bands, and regions of N58 modules in Table 2-1. • Updated the block diagram in Figure 2-1. • Updated the description of the application interfaces in the table of basic features. • Updated the power consumption data in sleep mode, idle mode, and operating mode. • Added chapter 3 "Refference Standards" to describe the reference standards of the N58 module design. • Added the VCC_GNSS_BIAS pin description of the N58 module with the GNSS function. • Updated the N58 module startup, shutdown, and reset flowcharts. • Added the reference design of the module sleep and wake-up control circuit.	Wu Yongqiang

		• Added the software (standard/open) version UART instructions. • Updated the reference design of the UART level shifting circuit. • Updated the reference design of the USIM interface circuit. • Added the reference design of the I2C interface circuit. • Added the 1PPS output waveform diagram. • Updated the description of GNSS technical parameters. • Added the reference design of the passive GNSS antenna circuit. • Updated the label diagram. • Updated the table of abbreviations. • Optimized the document to improve its quality.	
2.6	2021-11	• Added the circuit usage instructions for automatic startup upon module power-on. • Deleted section 5.6.10 "VCC_GNSS_BIAS."	Wu Yongqiang
2.7	2022-12	• Updated schematic design guidelines for the reference design of the USIM card interface. • Added application PCB design note in Section 9.2 . • Updated information including storage time and baking time in section 8.3 “Packaging”. • Updated Figure 5-42 "Recommended RF PCB design”. • Updated the data in Table 4-1	Wu Yongqiang
2.8	2023-02	• Modified description for the voltage-level translation circuit and updated the reference design circuits Figure 5-20,Figure 5-21, and Figure 5-22 in section 5.3.2 . • Updated the reference design of the USIM interface in section 5.3.3 “USIM”.	Wu Yongqiang

Conventions

Symbol	Description
	Indicates danger or warning. This information must be followed. Otherwise, a catastrophic module or user device failure or bodily injury may occur.

	Indicates caution. This symbol alerts the user to important points about using the module. If these points are not followed, the module or user device may fail.
	Indicates instructions or tips. This symbol provides advices or suggestions that may be useful when using the module.

Related Documents

Neoway_N58_Datasheet

Neoway_N58_Product_Specifications

Neoway_N58_AT_Commands_Mannual

Neoway_N58_EVK_User_Guide

1 Safety Recommendations

Please carefully read and strictly abide by the following safety requirements to ensure that the product application meets the national laws and environmental regulations, avoid risks to personal safety, and protect the product and application scenario from possible damage:

- Do not use the module in places where fire and explosion may occur.

  If the module is used in places filled with flammable gases and dust such as propane gas, gasoline and combustible spray, it will lead to explosion or fire.
- In places where wireless communication is prohibited, please disable the wireless communication function.

  In medical facilities or aircraft, the electromagnetic waves emitted by the module may interfere with the operation of surrounding equipment.

During the product application design and use of this module, the following requirements should be met:

- Do not disassemble the product of this module without permission. Otherwise, after-sales warranty service will not be available for the product.
- Design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not insert or remove (U)SIM card or mobile device memory card if the product is not in power-off mode.

2 About N58

N58 is a 4G industrial-grade module developed based on UNISOC UIS8910DM platform, with external dimensions of (30.00± 0.10) mm × (28.00± 0.10) mm × (2.50± 0.15) mm. The module provides connectivity on GSM, FDD-LTE (Cat 1) and TDD-LTE (Cat 1) networks. It provides various hardware interfaces, supporting audio, video, Wi-Fi positioning, BT/BLE, and GNSS (optional), suitable for developing IoT communications devices such as wireless meter reading terminal, in-vehicle device, potable POS device and industrial router.

N58 has the following features:

- ARM Cortex-A5 processor, 500 MHz CPU clock speed, 32 KB L1 cache
- Supported network modes: GSM/GPRS&LTE Cat 1
- Supports USB2.0/USIM/ADC/UART/SDIO/SPI/I2C/GNSS (optional)

2.1 Product Overview

The N58 series comprises multiple-band modules with four variants suitable for application in various regions.

Table 2-1 Models and frequency bands

Model	Region	Category	Frequency band	GNSS[1]	Codec
CA	Chinese mainland	Cat. 1	FDD-LTE: B1, B3, B5, B8 TDD-LTE: B34, B39, B40, B41 GSM/GPRS: 900/1800 MHz	Supported	Supported
EA	Europe/Middle East/Africa	Cat.1	FDD-LTE: B1, B3, B5, B7, B8, B20, B28 TDD-LTE: B38, B40, B41 GSM/GPRS: 900/1800 MHz	Supported	Supported
LA	Latin America	Cat.1	FDD-LTE: B1, B2, B3, B4, B5, B7, B8, B28, B66 TDD-LTE: B38, B40, B41 GSM/GPRS: 850/900/1800/1900 MHz	Supported	Supported

GNSS[1] optional configuration.

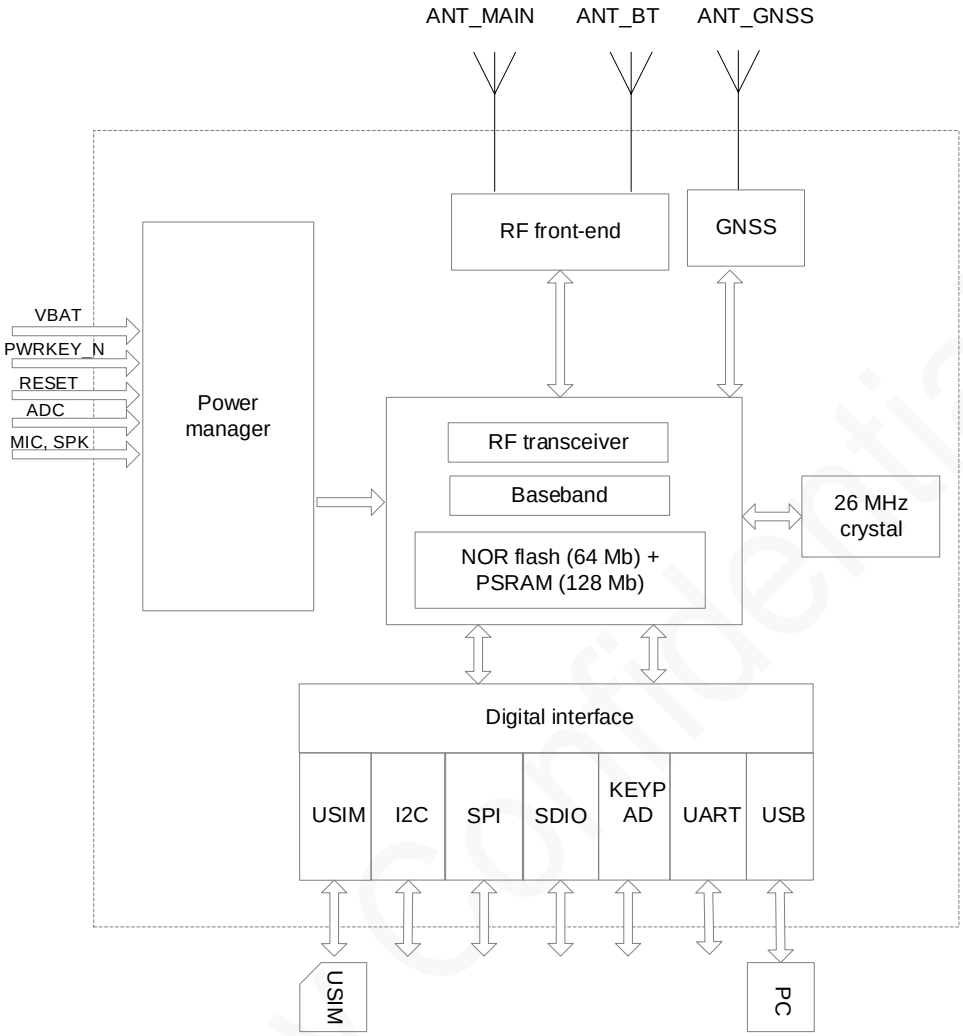
CA-F1	India	Cat 1	FDD-LTE: B1, B3, B5, B8 TDD-LTE: B40, B41 GSM/GPRS: 900/1800 MHz	Supported	Supported

2.2 Block Diagram

N58 series modules include the following functional units:

- Baseband chip
- 26 MHz crystal
- Power management
- RF functional
- Digital interfaces (USIM, I2C, SPI, KEYPAD, UART, USB, SDIO)
- Analog interfaces (ADC, MIC, SPK)

Figure 2-1 Block diagram



2.3 Basic Features

Features	Description
Physical features	• Dimensions: (30.00 ± 0.10) mm × (28.00 ± 0.10) mm × (2.50 ± 0.15) mm • Package: LGA+LCC • Weight: 4.63 g
Temperature ranges	Operating: -30°C to +75°C Extended: -40°C to +85°C Storage: -40°C to +90°C
Operating voltage (DC)	VBAT: 3.4 V to 4.2 V, typical value: 3.8 V

Operating current (DC)	Sleep mode[2]:< 3 mA Idle mode[3]：<16 mA Normal operation mode[4] (LTE system):< 600 mA
Application processor	ARM Cortex-A5 processor, 500 MHz CPU clock speed, 32 KB L1 cache
Memory	RAM: 128 Mb ROM: 64 Mb
Frequency band	See Table 2-1.
Wireless rate	GPRS: Max 85.6 kbps (DL)/Max 85.6 kbps (UL) FDD-LTE: Cat 1, Max 10 Mbps (DL)/Max 5 Mbps (UL) TDD-LTE: Cat 1, Max 8 Mbps (DL)/Max 2 Mbps (UL)
Transmit power	GSM850: +33 dBm (Power Class 4) EGSM900: +33 dBm (Power Class 4) DCS1800: +30 dBm (Power Class 1) PCS1900: +30 dBm (Power Class 1) LTE: +23 dBm (Power Class 3)
Application Interfaces	2G/4G antenna, GNSS antenna, BT antenna. The characteristic impedance of each antenna is 50 Ω.
	Three UART interfaces with baud rates up to 921600 bps.
	Two USIM interfaces, supporting 1.8 V/3 V USIM cards.
	One USB 2.0 interface, for slave mode only.
	Three SPI interfaces. One standard SPI interface, for master mode only; one LCD-dedicated SPI interface; one camera-dedicated SPI interface.
	3x4 matrix keyboard interface.
	One 12-bit ADC interface, voltage detection range: 0.1 V - VBAT.
	One SDIO interface, for SD card.
	One 1PPS interface.
	One MIC interface with built-in bias voltage range of 2.2 V - 3 V.
	One SPK interface, with built-in Class AB/D power amplifier, and output power up to 800 mW @ 4.2 V / 8 Ω.

Operating current in sleep mode[2]: means the current drawn by the module in sleep mode, a low power consumption state, in which its RF function is functioning properly but its peripheral interfaces are disabled. If there is an incoming call or SMS, the module will exit from the sleep mode, and after the incoming call or voice instant messaging has ended, the module will re-enter the sleep mode.

Operating current in idle mode[3]: means the current drawn by the module in a normal operating mode, but no data service is being processed.

Operating current in normal operation mode [4]: means the current drawn by the module when there are on-going data services. In this mode, only the current value in LTE system is exemplified. For other current values in other network modes, please refer to the current test report.

	One I2C interface, for master mode only.
AT command	3GPP Release 13 Neoway extended AT commands
SMS	PDU, TXT
Data	PPP, RNDIS, ECM
Protocol	TCP, UDP, MQTT, FTP, HTTP/HTTPS, SSL, TLS
Certification approval	CCC, SRRC, RoHS, CE, CTA

3 Refference Standards

- 3GPP TS 36.521-1 V13.0.0 User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance Testing
- 3GPP TS 21.111 V13.0.0 USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0 Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V13.0.0 Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V13.0.0 Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V13.0.0 AT command set for User Equipment (UE)
- 3GPP TS 27.005 V13.0.0 Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

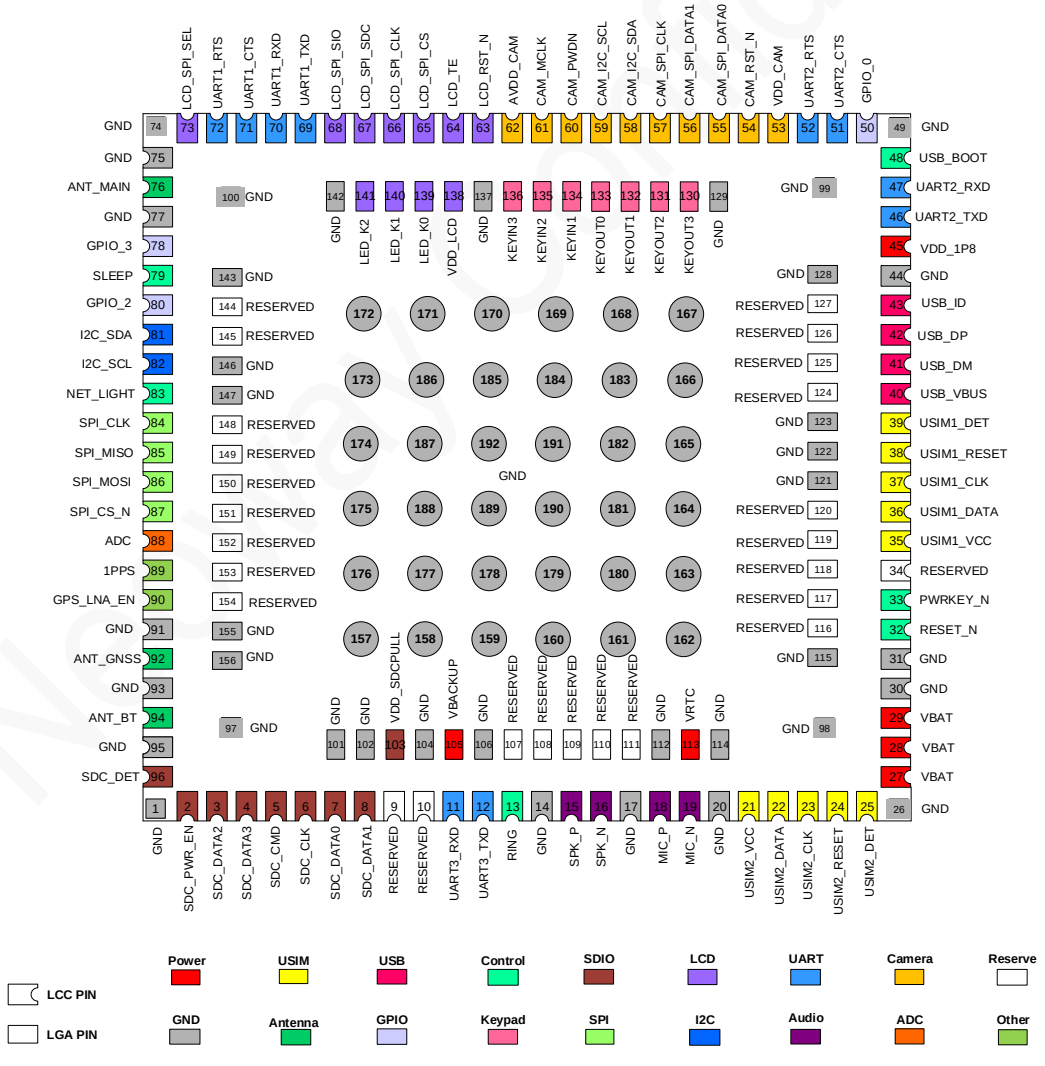
4 Pin Definitions

N58 series modules are equipped with 192 pads, which are introduced in LGA (100 pins) + LCC (92 pins) package. Available functional interfaces include: Power supply, USB, USIM, UART, ADC, I2C, SDIO, etc.

4.1 Pad Layout

Figure 4-1 shows the pad layout of N58.

Figure 4-1 Pad layout of N58 (top view)



4.2 Pin Description

The following table lists the IO types and DC characteristics.

Table 4-1 IO types and DC characteristics

IO type			
B	Digital input and output, CMOS logic level		
DO	Digital output, CMOS logic level		
DI	Digital input, CMOS logic level		
PO	Power output		
PI	Power input		
AO	Analog output		
AI	Analog input		
AIO	Analog input and output		
DC characteristics			
Interface type	Power domain	Logic level characteristics	
USIM	P1: Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented V_{DD_P1}: 1.62 V - 1.98 V (typical value: 1.8 V) /2.9 V - 3.3 V (typical value: 3 V)	1.8 V DC characteristics V_{IH}=0.7V_{DD_P1} - V_{DD_P1} V_{IL}=0V - 0.3V_{DD_P1} V_{OH}=0.9V_{DD_P1} - V_{DD_P1} V_{OL}=0V - 0.1V_{DD_P1}	3.0 V DC characteristics V_{IH}=0.7V_{DD_P1} - V_{DD_P1} V_{IL}=0V - 0.15V_{DD_P1} V_{OH}=0.9V_{DD_P1} - V_{DD_P1} V_{OL}=0V - 0.1V_{DD_P1}
GPIO	P3: 1.8 V V_{DD_P3}: 1.7 V - 1.9 V (typical value: 1.8 V)	V_{IH}=0.7V_{DD_P3} - V_{DD_P3} V_{IL}=0V - 0.3V_{DD_P3} V_{OH}=0.8V_{DD_P3} - V_{DD_P3} V_{OL}=0V - 0.2V_{DD_P3}	

Table 4-2 Pin description

Signal	Pin SN	I/O type	Function description	DC characteristics	Remarks
Power interface					
VBAT	27, 28, 29	PI	Main power supply input	V_{min}=3.4 V V_{norm}=3.8 V V_{max}=4.2 V	The external power supply must ensure at least 2.5 A current for VBAT.
VDD_1P8	45	PO	1.8 V power output	V_{norm}=1.8 V I_{max}=50 mA	Only used for voltage-level translation. Leave this pin open if unused.
GND	1, 14, 17, 20, 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97 - 102, 104, 106, 112, 114, 115, 121 - 123, 128, 129, 137, 142, 143, 146, 147, 155 - 192				Make sure all GND pins are grounded.
Control interfaces					
RESET_N	32	DI	Module reset input	-	Active low This pin is pulled up to VBAT via a 20 kΩ resistor inside the main chip of the module.
PWRKEY_N	33	DI	Module on/off control	-	A low pulse for a valid time period can trigger on/off of the module (see section 5.2.2). This pin is pulled up to VBAT via a 20 kΩ resistor inside the main chip of the module.
SLEEP	79	DI	Sleep mode control	P3	See section 5.2.3 for details.
UART1 interface					
UART1_TXD	69	DO	UART data output	P3	Software version (Standard): For data transmission. Software version (Open): For data transmission. Note: UART1_CTS (pin #71) can be used to capture CP log.
UART1_RXD	70	DI	UART data input	P3	
UART1_CTS	71	DI	UART clear to send	P3	
UART1_RTS	72	DO	UART ready to send	P3	

UART2 interface					
UART2_TXD	46	DO	UART data output	P3	Software version (Standard): For communication based on AT commands. Software version (Open): For data transmission.
UART2_RXD	47	DI	UART data input	P3	
UART2_CTS	51	DI	UART clear to send	P3	
UART2_RTS	52	DO	UART ready to send	P3	
UART3 interface					
UART3_RXD	11	DI	UART data input	P3	For module debugging only.
UART3_TXD	12	DO	UART data output	P3	
USIM1 interface					
USIM1_VCC	35	PO	USIM1 power output	P1	-
USIM1_DATA	36	B	USIM1 data input and output	P1	This pin is pulled up to USIM1_VCC via a 4.7 kΩ resistor.
USIM1_CLK	37	DO	USIM1 clock output	P1	-
USIM1_RESET	38	DO	USIM1 reset	P1	-
USIM1_DET	39	DI	USIM1 detection	P3	If the hot swap function is not used, please refer to the section 5.3.3 for handling method details of this interface.
USIM2 interface					
USIM2_VCC	21	PO	USIM2 power output	P1	-
USIM2_DATA	22	B	USIM2 data input and output	P1	This pin is pulled up to USIM2_VCC via a 4.7 kΩ resistor.
USIM2_CLK	23	DO	USIM2 clock output	P1	-
USIM2_RESET	24	DO	USIM2 reset	P1	-

USIM2_DET	25	DI	USIM2 detection	P3	If the hot swap function is not used, please refer to the section 5.3.3 for handling method details of this pin.
USB interface					
USB_VBUS	40	PI	Voltage detection	4.5 V - 5.2 V, typical value: 5 V	Route the DM and DP traces as differential pairs with 90 Ω impedance. Leave these pins open if unused.
USB_DM	41	AIO	USB data -	-	
USB_DP	42	AIO	USB data +	-	
USB_ID	43	DI	Master-slave detection	-	Leave this pin open if unused.
ADC interface					
ADC1	88	AI	General analog-to-digital signal	-	12-bit, detectable voltage range: 0.1 V - VBAT. Leave this pin open if unused.
I2C Interface					
I2C_SDA	81	B	I2C data	P3	This pin is pulled up to VDD_1P8 via a 1.8 kΩ resistor.
I2C_SCL	82	DO	I2C clock	P3	This pin is pulled up to VDD_1P8 via a 1.8 kΩ resistor.
LCD interface					
LCD_RST_N	63	DO	Reset control	1.8 V/3.0 V	Leave this pin open if unused.
LCD_TE	64	DO	Data frame read ready flag	1.8 V/3.0 V	Leave this pin open if unused.
LCD_SPI_CS	65	DO	SPI chip selection signal	1.8 V/3.0 V	Leave this pin open if unused.
LCD_SPI_CLK	66	DO	SPI clock signal	1.8 V/3.0 V	Leave this pin open if unused.
LCD_SPI_SDC	67	B	Data or command control signal	1.8 V/3.0 V	Leave this pin open if unused.

LCD_SPI_SIO	68	B	Data input/output	1.8 V/3.0 V	Leave this pin open if unused.
LCD_SPI_SEL	73	DO	Selection signal	1.8 V/3.0 V	Leave this pin open if unused.
VDD_LCD	138	PO	DC power supply	1.6 V - 3.2 V	This analog power is disabled by default. If enabled, the default output is 1.8 V / 200 mA.
LED_K0	139	PI	LED backlight	-	The anode power supply range is 3.45 V - 4.3 V, and the maximum input current is 50 mA.
LED_K1	140	PI	LED backlight	-	The anode power supply range is 3.45 V - 4.3 V, and the maximum input current is 50 mA.
LED_K2	141	PI	LED backlight	-	The anode power supply range is 3.45 V - 4.3 V, and the maximum input current is 50 mA.
CAM interface					
VDD_CAM	53	PO	Camera digital power supply	1.4 V - 2.1 V	This analog power is disabled by default. If enabled, the default output is 1.8 V / 100 mA.
CAM_RST_N	54	DO	Reset signal	P3	Active low
CAM_SPI_DATA0	55	B	Data signal input	P3	Leave this pin open if unused.
CAM_SPI_DATA1	56	B	Data signal input	P3	Leave this pin open if unused.
CAM_SPI_CLK	57	DO	SPI clock signal	P3	Leave this pin open if unused.
CAM_I2C_SDA	58	B	I2C data	P3	Leave this pin open if unused.
CAM_I2C_SCL	59	DO	I2C clock	P3	Leave this pin open if unused.
CAM_PWDN	60	DO	Power down control	P3	Leave this pin open if unused.
CAM_MCLK	61	DO	Clock signal	P3	Leave this pin open if unused.
AVDD_CAM	62	PO	Camera analog power supply	1.6 V - 3.2 V	This analog power is disabled by default. If enabled, the default output is 1.8 V / 100 mA.

SDIO interface					
SDC_PWR_EN	2	DO	SD card external power supply enabling	P3	Leave this pin open if unused.
SDC_DATA_2	3	B	SD card SDIO bus data 2	1.8 V/3.0 V	Leave this pin open if unused.
SDC_DATA_3	4	B	SD card SDIO bus data 3	1.8 V/3.0 V	Leave this pin open if unused.
SDC_CMD	5	DO	SD card SDIO bus command	1.8 V/3.0 V	Leave this pin open if unused.
SDC_CLK	6	DO	SDIO clock	1.8 V/3.0 V	Leave this pin open if unused.
SDC_DATA_0	7	B	SD card SDIO bus data 0	1.8 V/3.0 V	Leave this pin open if unused.
SDC_DATA_1	8	B	SD card SDIO bus data 1	1.8 V/3.0 V	Leave this pin open if unused.
SDC_DET	96	DI	SD card insertion detect	P3	Leave this pin open if unused.
VDD_SDCPULL	103	PO	SD card SDIO bus pull-up power supply	1.6 V - 3.2 V	This power supply is enabled by default, with output 3.1 V/150 mA. It shall not supply power to other loads.
SPI interface					
SPI_CLK	84	DO	Clock signal	P3	Leave this pin open if unused.
SPI_MISO	85	B	Output of slave device, input of master device	P3	Leave this pin open if unused.
SPI_MOSI	86	B	Input of slave device, output of master device	P3	Leave this pin open if unused.
SPI_CS_N	87	DO	Chip selection signal of slave device	P3	Leave this pin open if unused.
GPIO interface					
GPIO_0	50	B	GPIO	P3	Leave this pin open if unused.

GPIO_2	80	B	GPIO	P3	Leave this pin open if unused.
GPIO_3	78	B	GPIO	P3	Leave this pin open if unused.
Audio SPK interface					
SPK_P	15	AO	Speaker output +	-	-
SPK_N	16	AO	Speaker output -	-	-
Audio MIC interface				-	-
MIC_P	18	AI	IMIC input channel +	-	-
MIC_N	19	AI	MIC input channel -	-	-
Antenna Interfaces					
ANT_MAIN	76		Main antenna	-	50 Ω impedance.
ANT_GNSS	92		GNSS antenna	-	50 Ω impedance.
ANT_BT	94		BT antenna	-	50 Ω impedance.
Other functional interfaces					
GNSS_LNA_EN	90	DO	GNSS LNA enabling	P3	Leave this pin open if unused.
VBACKUP	105	PI	GNSS backup power supply	3.0 V - 3.3 V	Button cells or Farad capacitors can be the backup power supply for GNSS. Leave this pin open if unused.
VRTC	113	PI	RTC power supply	2.8 V - 3.2 V, typical value 3.0 V	Button cells or Farad capacitors can be the backup power supply for RTC. Leave this pin open if unused.
RING	13	DO	Incoming call & SMS indicator control	P3	Leave this pin open if unused.

NET_LIGHT	83	DO	Network indication control	P3	Leave this pin open if unused.
1PPS	89	DO	GNSS timing output	-	Timing precision is less than 30 ns. This function is only for the N58 module with GNSS.
Keypad interface					
KEYOUT3	130	DO	Key output	-	-
KEYOUT2	131	DO	Key output	-	-
KEYOUT1	132	DO	Key output	-	-
KEYOUT0	133	DO	Key output	-	-
KEYIN1	134	DI	Key input	-	-
KEYIN2	135	DI	Key input	-	-
KEYIN3	136	DI	Key input	-	-
USB_BOOT	48	DI	Emergency download control	P3	You can pull up USB_BOOT to 1.8 V before powering up the module, and thus the module will enter emergency download mode when powered on. Leave this pin open if unused.
RESERVED	9, 10, 34, 107 - 111, 116 - 120, 124 - 127, 145, 148 - 154		Reserved pin	-	Reserved for future function expansion or functions not open to the user. There may be more than one pin named RESERVED, which may have different functions or definitions. Leave these RESERVED pins open.

- N58 module versions without GNSS:

  The pins #9 and #10 of the module can be used as UART4 interface (pin #9 is UART4_TXD, and pin #10 is UART4_RXD, with interface level 1.8 V). The pin #89 of the module can be used as ADC2 interface (The interface characteristics of ADC2 are the same as those of ADC1).

- N58 module versions with GNSS:

  The pins #9 and #10 of the module are RESERVED pins and leave these pins open if unused. Pin #89 is a 1PPS pin. See section 5.6.9 “1PPS” for details.

5 Application Interfaces

N58 provides interfaces for control, communications, peripherals, audio, display, RF and other functions to meet the requirements of different product application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

5.1 Power Interfaces

The schematic design and PCB layout of the power supply part are the most critical process in application design and they will determine the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin SN	I/O	Function description	Remarks
VBAT	27, 28, 29	PI	Module supply input	3.4 V - 4.2 V (typical value: 3.8 V)
VDD_1P8	45	PO	1.8 V power output	V_{norm}=1.8 V I_{max}=50 mA
GND	1, 14, 17, 20, 26, 30, 31, 44, 49, 74, 75, 77, 91, 93, 95, 97-102, 104, 106, 112, 114, 115, 121-123, 128, 129, 137, 142, 143, 146, 147, 155-192			Make sure all GND pins are grounded.

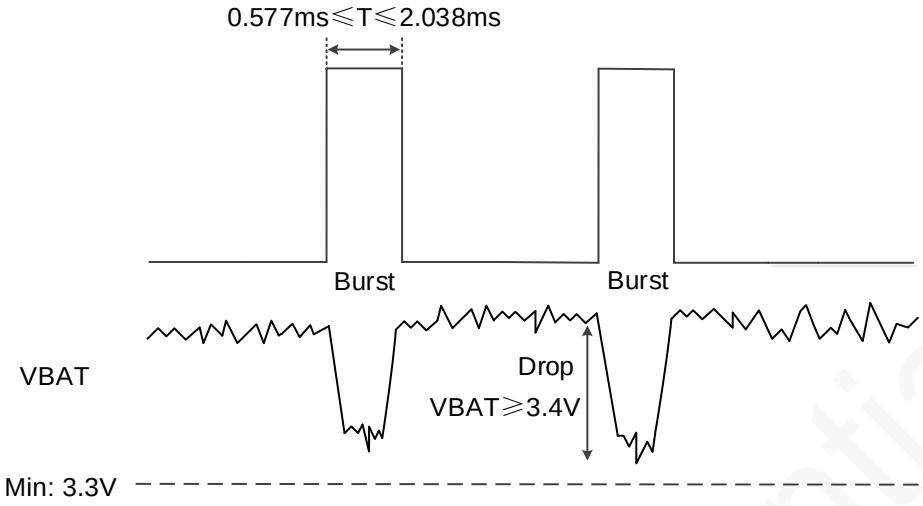
5.1.1 VBAT

The design of power supply includes two parts: schematic design and PCB layout.

Power Supply Design

In GSM/GPRS mode, RF data transmission is intermittent, the frequency of burst transmission is about 217 Hz, and the peak current is up to 2.5 A. Therefore, it is necessary to ensure the following conditions: The driving capacity of the power supply is sufficient, the power supply trace is wide enough to reduce the impedance, and a large capacitance is provided to improve the freewheeling current, thereby ensuring that the voltage will not drop below the minimum operating voltage of the module at the instantaneous peak current.

Figure 5-1 Voltage drop of the power supply.



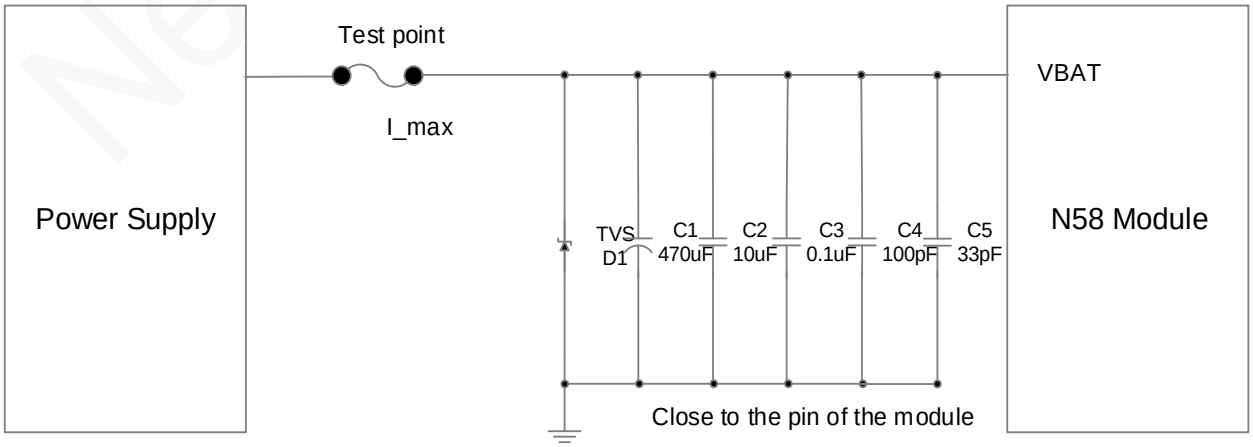
Never use a diode to make the voltage drop between a higher input and the module power supply. The forward voltage drop V_f of diode has two characteristics: one is that it increases with the increase of the forward current. the other is that it increases significantly at a low temperature. Note that, if there is an instantaneous high current, the above characteristics will lead to unstable operating voltage of the module, and even damage the module.

The power supply design of the N58 module depends on the input voltage of power supply. There are three power input types:

- 3.4 V - 4.2 V power input (typical value: 3.8 V, provided by a battery)
- 4.2 V - 5.5 V power input (typical value: 5.0 V, provided by a computer internal rectifier)
- 5.5 V - 24 V power input (typical value: 12 V, provided by system DC power for some industries such as automotive industry)

The design recommendations for 3.4 V - 4.2 V power input are as follows:

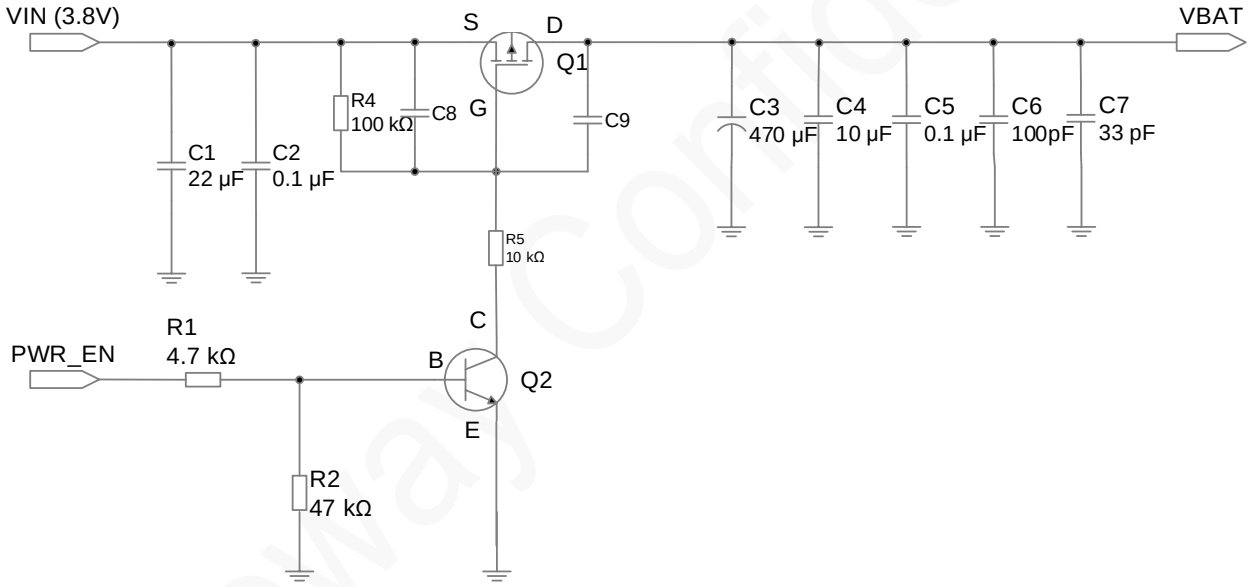
Figure 5-2 Recommended power supply design 1



- The maximum input voltage of the module power supply is 4.2 V, and the typical value is 3.8 V. For VBAT, the recommended PCB trace width is 2.5 mm or above.
- In order to get a stable power source, it is recommended to use a TVS diode with suggested low reverse voltage (VRWM 4.5 V) and peak power (Ppp = 2800 W (tp = 8/20 us)) at D1. Keep the TVS diode close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and the module.
- To decrease voltage drops during bursts, a large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1. Its maximum safe operating voltage should be larger than 2 times the voltage of the power supply.
- Keep low ESR bypass capacitors (C2, C3, C4, C5) as close to the module as possible to filter out high-frequency interference in the power supply.

If it is necessary to control the power supply, the following circuit design is recommended:

Figure 5-3 Recommended power supply design 2

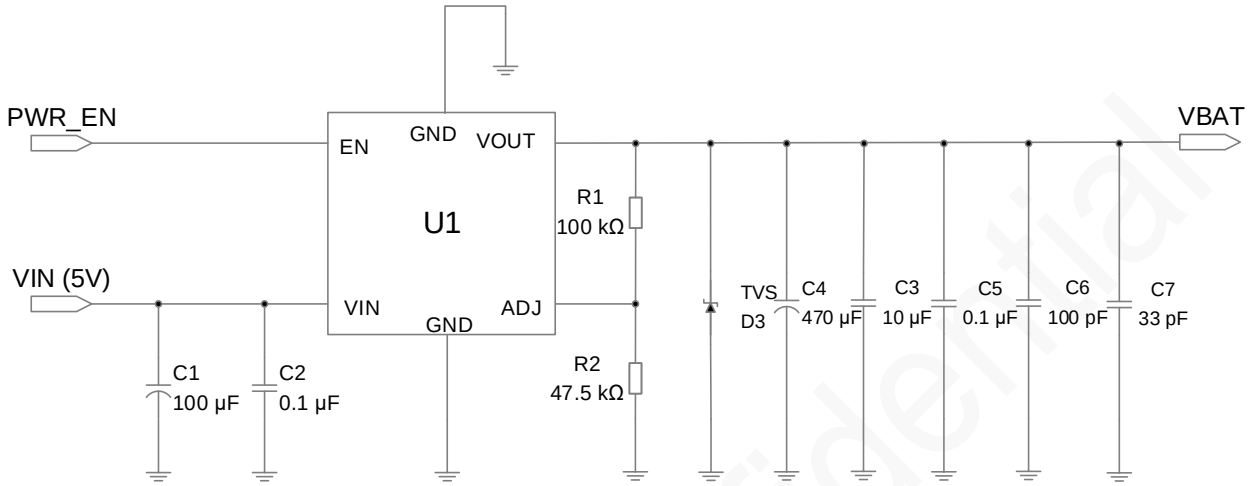


- Select an enhanced P-MOSFET at Q1, of which the withstand voltage is high (V_{dss} = -12 V), drain current is high ($I_{D(MAX)}$ = -3.5 A) and RDS is low ($R_{ds(on)}$ = 108 mΩ).
- Select a common NPN transistor or a digital NPN transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which the break-over voltage on the base of the transistor increases at a low temperature; it is recommended that the value of R2 be at least 10 times that of R1.
- Keep the placement of C3 close to the module. Select a tantalum electrolytic capacitor with large capacitance (220 μF or 100 μF) or an aluminum electrolytic capacitor (470 μF or 1000 μF) at C3 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be larger than 2 times the power supply voltage.

- Keep low ESR bypass capacitors (C4, C5, C6, C7) as close to the module as possible to filter out high-frequency interference in the power supply.

The design recommendations for the 4.2 V - 5.5 V power input are as follows:

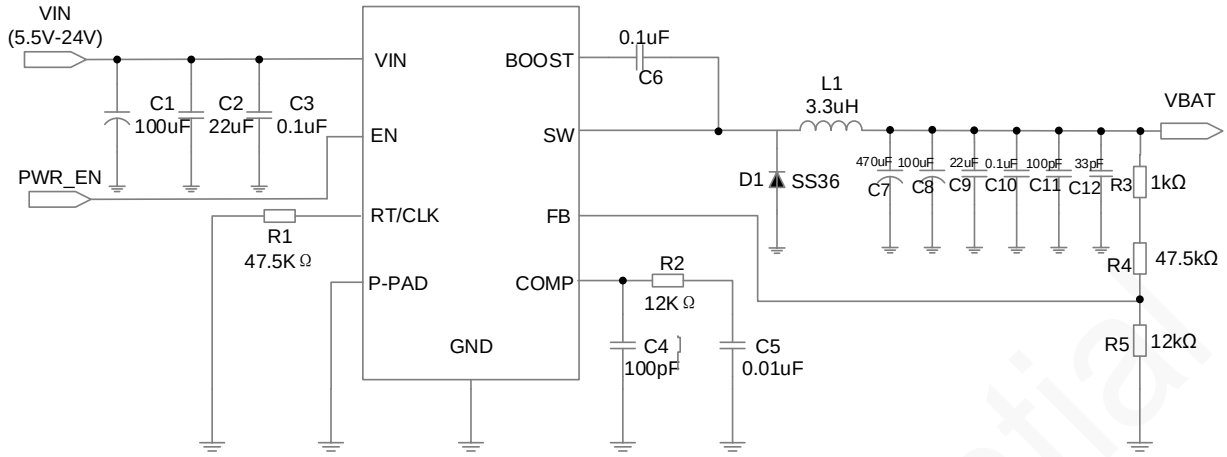
Figure 5-4 Recommended power supply design 3



- Design with LDO is simpler and more efficient when the output of power supply is close to the permissible voltage across VBAT.
- Select an LDO with maximum output current above 2.5 A at U1 to ensure the normal performance of the module.
- Use a TVS diode with suggested low reverse voltage (VRWM = 4.5 V) and peak power (Ppp = 2800 W (tp = 8/20 us)) at D3. Keep the TVS diode close to the power input interface to ensure that the power surge voltage is clamped before entering the back-end circuit, thus protecting the back-end components and modules.
- Keep the placement of C4 close to the module. Select a large tantalum electrolytic capacitor (220 μF or 400 μF) or aluminum electrolytic capacitor (470 μF or 1000 μF) at C5 to improve the instantaneous large current freewheeling ability of the power supply, and its withstand voltage value should be more than 2 times the power supply voltage.
- Keep low ESR bypass capacitors (C3, C5, C6, C7) as close to the module as possible to filter out high-frequency interference in the power supply.

The design recommendations for the 5.5 V - 24 V power input are as follows:

Figure 5-5 Recommended power supply design 4



- If there is a high voltage drop between the power input and VBAT, a DC-DC design should be selected for higher efficiency, and the output current should be at least 2.5 A.
- Note that the switching frequency of the DC-DC power supply is related to the performance of the final product, and may lead to EMC interference.
- For the vehicle battery (lead-acid battery), add the power surge protection to the input front-end, and the component withstand voltage should be greater than 42 V.
- Keep the placement of C7 close to the module. Select a tantalum electrolytic capacitor with large capacitance (220 μF or 100 μF) or an aluminum electrolytic capacitor (470 μF or 1000 μF) at C7 to improve the instantaneous large freewheeling current of the power supply, and its withstand voltage value should be more than 2 times the power supply voltage.
- Keep low ESR bypass capacitors (C9, C10, C11, C12) as close to the module as possible to filter out high-frequency interference in the power supply.

PCB Layout

Place an ESR capacitor at the output of the power source to suppress peak current. In order to protect the back-end components, it is necessary to add a TVS diodes at the input of the power supply to suppress voltage spikes. The circuit design is important, and the component placement and PCB routing are equally important. Several key points in power supply design are as follows:

- The TVS diode can absorb instantaneous high-power pulse, and can withstand instantaneous pulse current peaks up to tens or even hundreds of amperes, with extremely short response time of voltage clamping. Keep TVS diodes as close to the the power input as possible, ensuring that the surge voltage can be clamped before the pulse is coupled to the adjacent PCB traces.
- Place bypass capacitors as close as possible to the power supply interface of the module to filter out high-frequency noise signals in the power supply.

- For the main power circuit of the module, ensure that the PCB trace is wide enough that 2.5 A current can be safely passed, with no significant loop voltage drop. Keep PCB trace width be at least 2.5 mm and ensure that the ground plane of the power supply part is as complete as possible. In addition, try to make power traces short and wide.
- Keep noise-sensitive circuits, such as audio circuits and RF circuits far away from the power circuitry, especially when the DC-DC power supply is used.
- The voltage frequency of the SW pin of the DC-DC power supply is high, so the loop area should be minimized. Keep sensitive components far away from the SW pin of the DC-DC component to prevent noise coupling. Place feedback components as close as possible to the FB pin and COMP pin.
- The thermal-dissipation pads and GND pads of the DC-DC chip should be grounded to ensure good thermal dissipation and noise signal isolation.

5.1.2 VDD_1P8

VDD_1P8 power is normally on and cannot be turned off even in sleep mode. If an external circuit is connected, the sleep power consumption will increase. It is recommended that VDD_1P8 is used only for voltage-level translation, not for other purpose, and ESD protection is required when using VDD_1P8.

N58 provides one VDD_1P8 interface with output currents up to 50 mA.

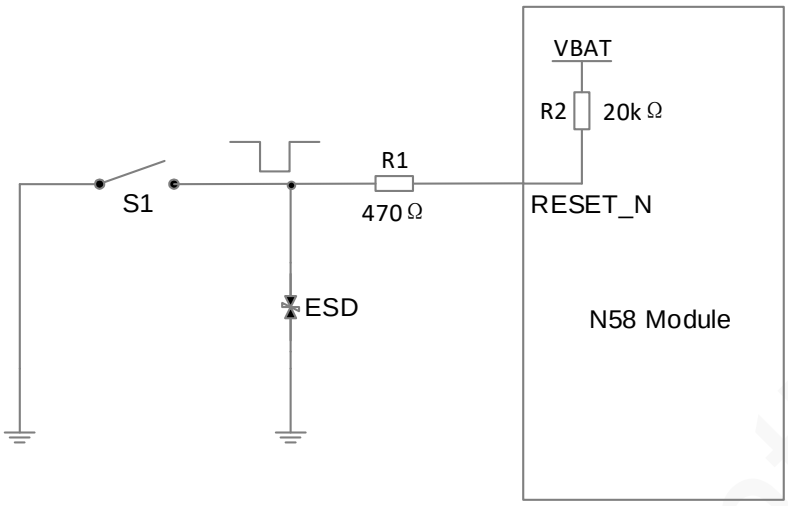
5.2 Control Interfaces

Signal	Pin SN	I/O	Function description	Remarks
RESET_N	32	DI	Module reset input	Active low
PWRKEY_N	33	DI	Module on/off control	Active low
SLEEP	79	DI	Sleep mode control	Leave this pin open if unused.

5.2.1 RESET_N

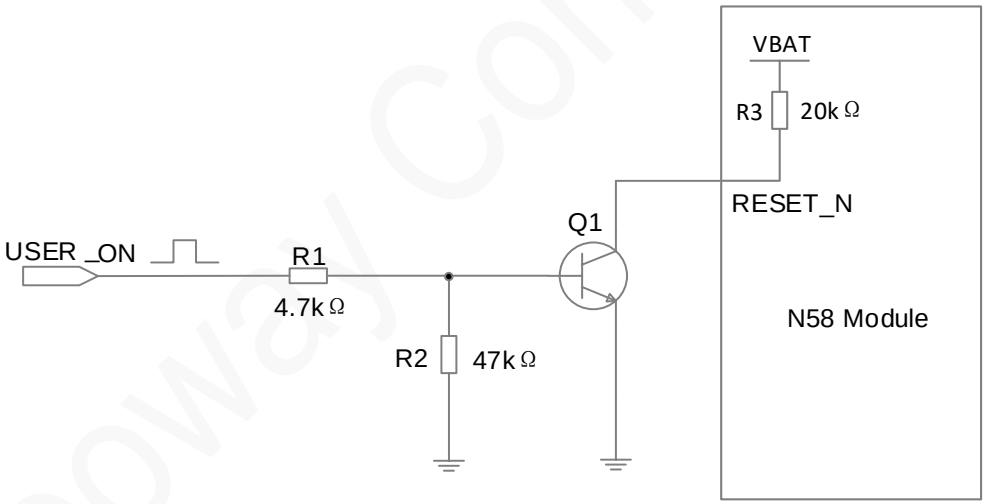
N58 can be reset with the RESET_N pin. When the module is in power-on mode, inputting a negative pulse for more than 50 ms to RESET_N can reset the module. The RESET_N pin is pulled up through a 20 kΩ resistor inside the module to VBAT. Leave this pin open if unused.

Figure 5-6 Reference design of push-button reset



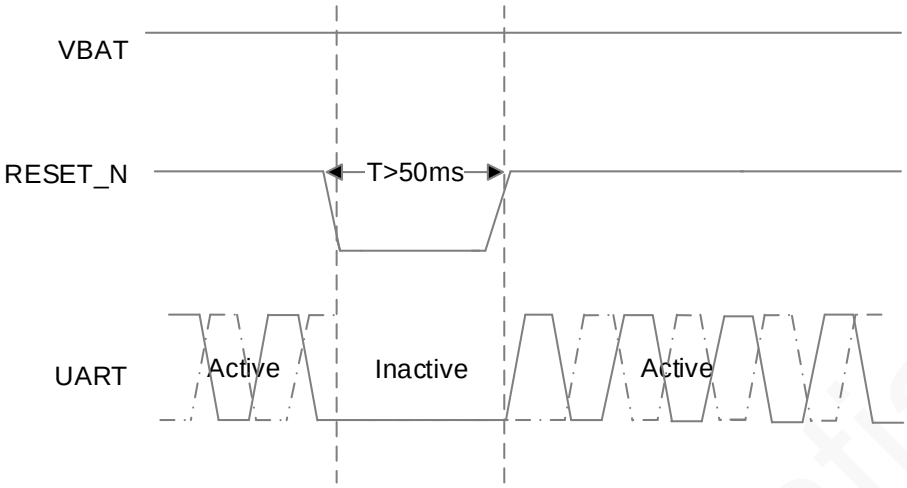
If you use a 1.8 V / 2.8 V / 3.0 V IO system, it is recommended to add a triode to for isolation. Refer to the following figure for specific design.

Figure 5-7 Reference reset circuit in which a triode is used for isolation



N58 module reset process is shown in the following figure.

Figure 5-8 Module reset process



5.2.2 PWRKEY_N

Turning on the N58 module can be done in three different ways, which can be selected according to specific application scenarios. If necessary, please contact Neoway for confirmation.

N58 allows startup by the following methods:

- Figure 5-9 shows the reference design of push-button startup
- Figure 5-10 shows the reference design of MCU-control startup
- Figure 5-11 shows the reference design of automatic startup once powered up

Figure 5-9 Reference design of push-button startup

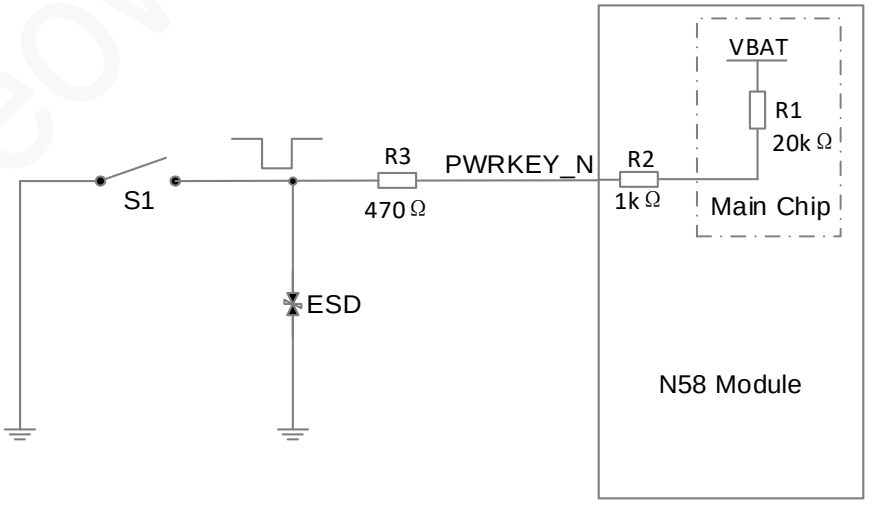
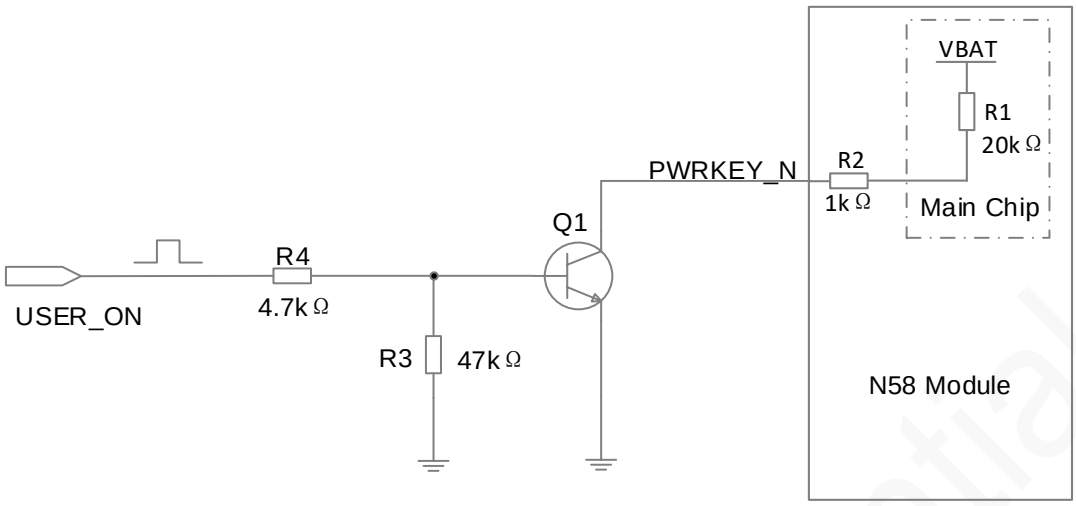
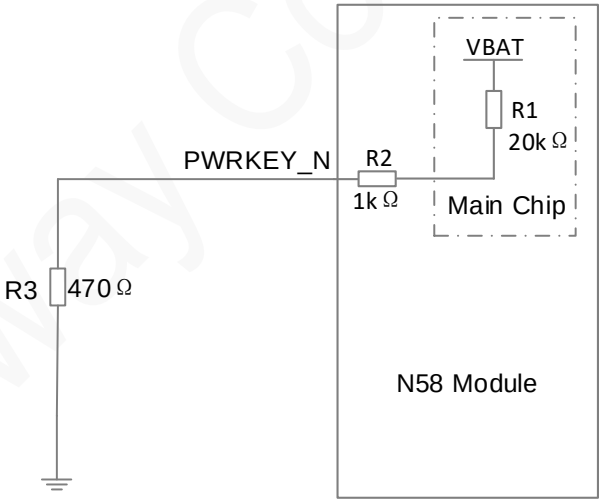


Figure 5-10 Reference design of MCU-control startup



Note that adding a reset solution during designing the auto power-on circuit is a must when the module requires to be repeatedly turned on and off. To ensure a proper power-on/off operation, reset the module at least one time after power-on. For the reset circuit, see Figure 5-7.

Figure 5-11 Reference design of automatic startup once powered up



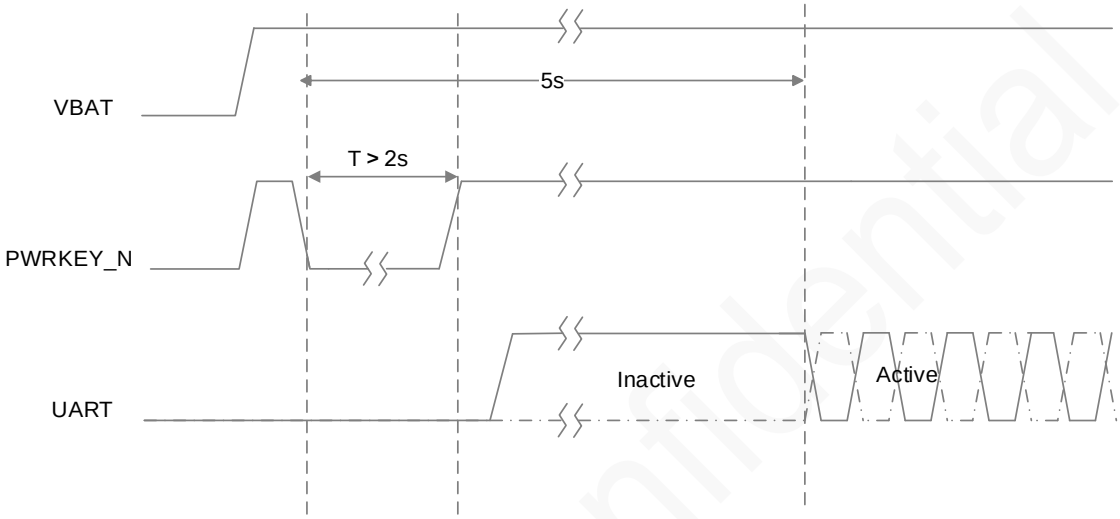
Power-on process

After the VBAT input is powered, to switch the module on, the PWRKEY_N interface must be asserted low for 3s and then released. The AT function is available 5 seconds after the assertion of PWRKEY_N. Do NOT connect an external resistor with large resistance value in series to the PWRKEY_N pin (a 470 Ω resistor is recommended) since there is already an internal 1 kΩ series resistor. Otherwise, the module cannot be switched on since the PWRKEY_N is at a high level all the time.

To set automatic startup once powered up for the module, the PWRKEY_N pin should be connected in series with a 470 Ω resistor to ground.

After the module is switched on, it needs to perform initialization process until its pin state is stable, and during the process, do not perform other operations on it. The module startup process is shown in the following figure.

Figure 5-12 Power-on process



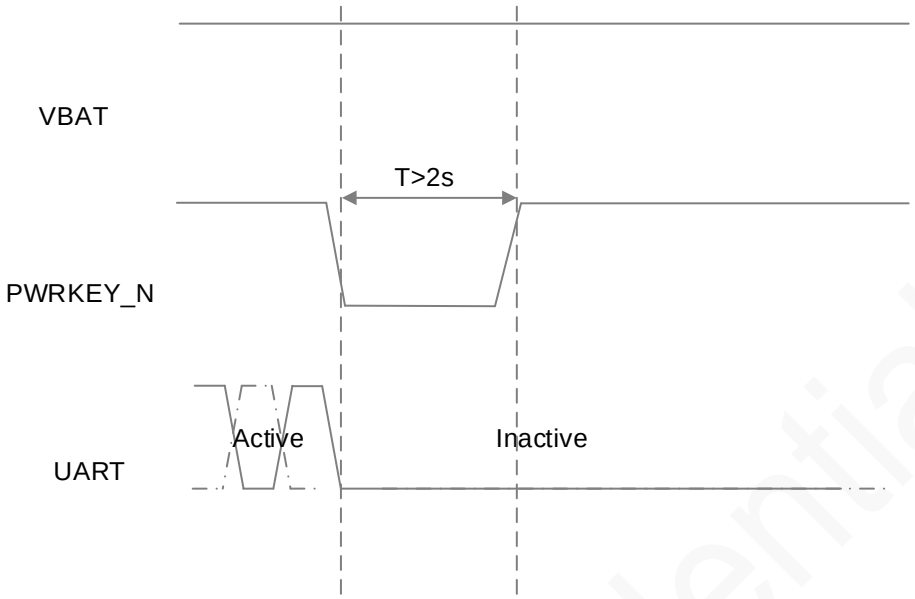
Power-off Process

Two methods are available to turn off the module: hardware shutdown using PWRKEY_N pin and software shutdown.

When the module is in power-on mode, to turn off the module, the PWRKEY_N pin must be asserted low for greater than 2s and then released.

The following figure shows the hardware shutdown process:

Figure 5-13 Hardware shutdown process of N58



The module can be shut down by a software command. Please refer to *Neoway*_N58_*AT_Commands_Manual* for details.

5.2.3 SLEEP

The SLEEP pin is used to control sleep mode of the module and needs to be used together with the AT command. Sending the corresponding AT command to the module via its UART2 interface can set the module into sleep mode or wake up the module from sleep mode. For details, see *Neoway*_N58_*AT_Commands_Manual*. In sleep mode, the module can still responds to voice calls, SMS, and processes data services normally.

The following show the processes:

Figure 5-14 Process of entering into sleep mode

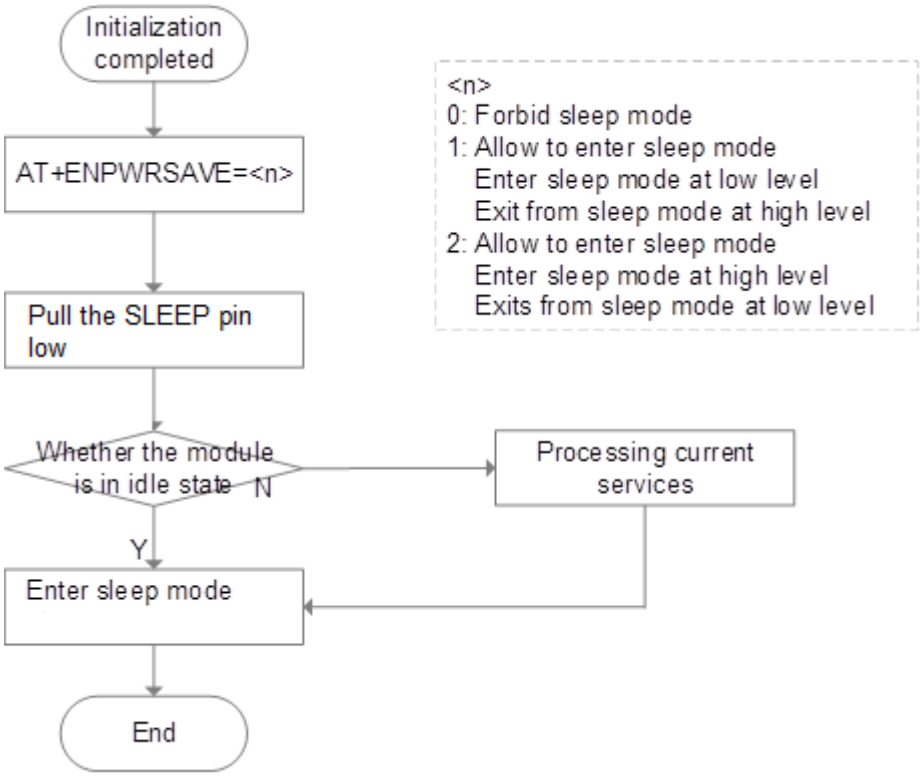


Figure 5-15 Process of processing data services in sleep mode

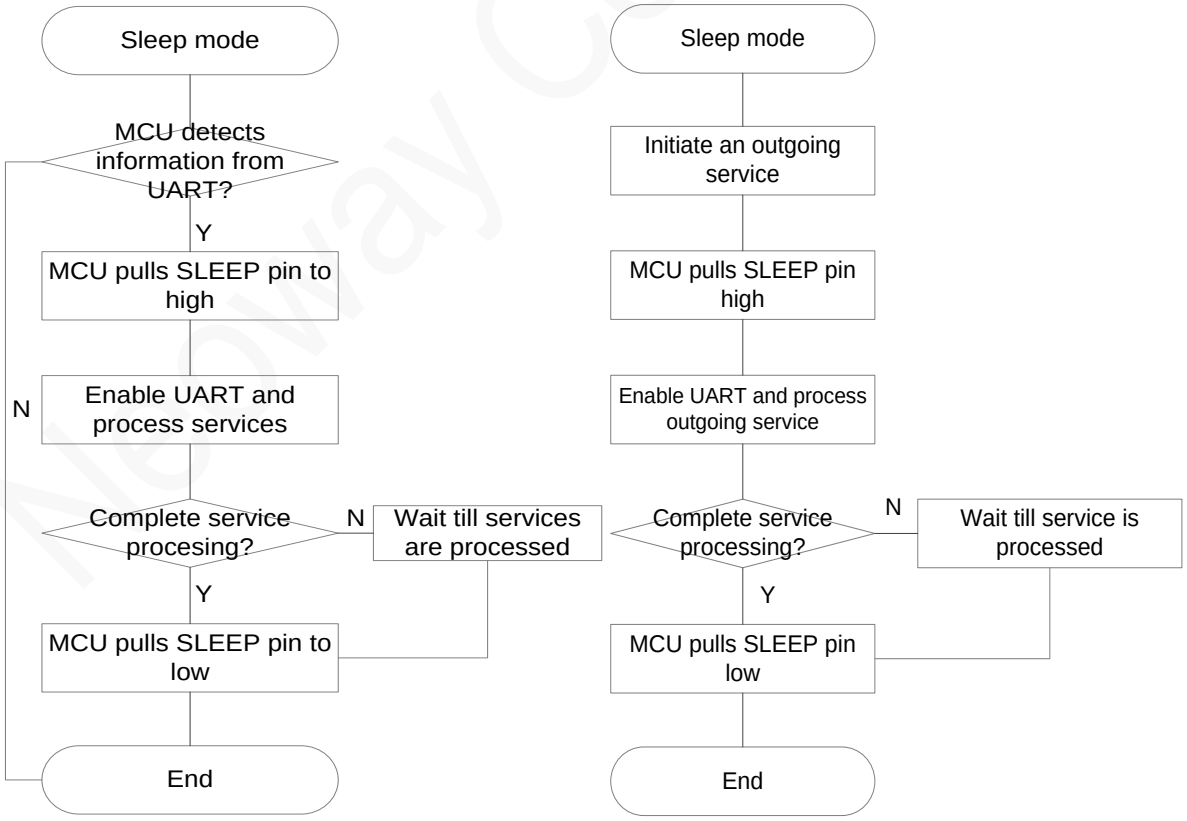
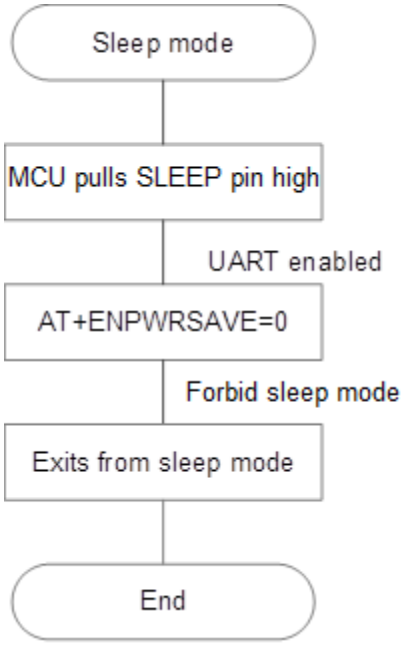


Figure 5-16 Process of waking up the module

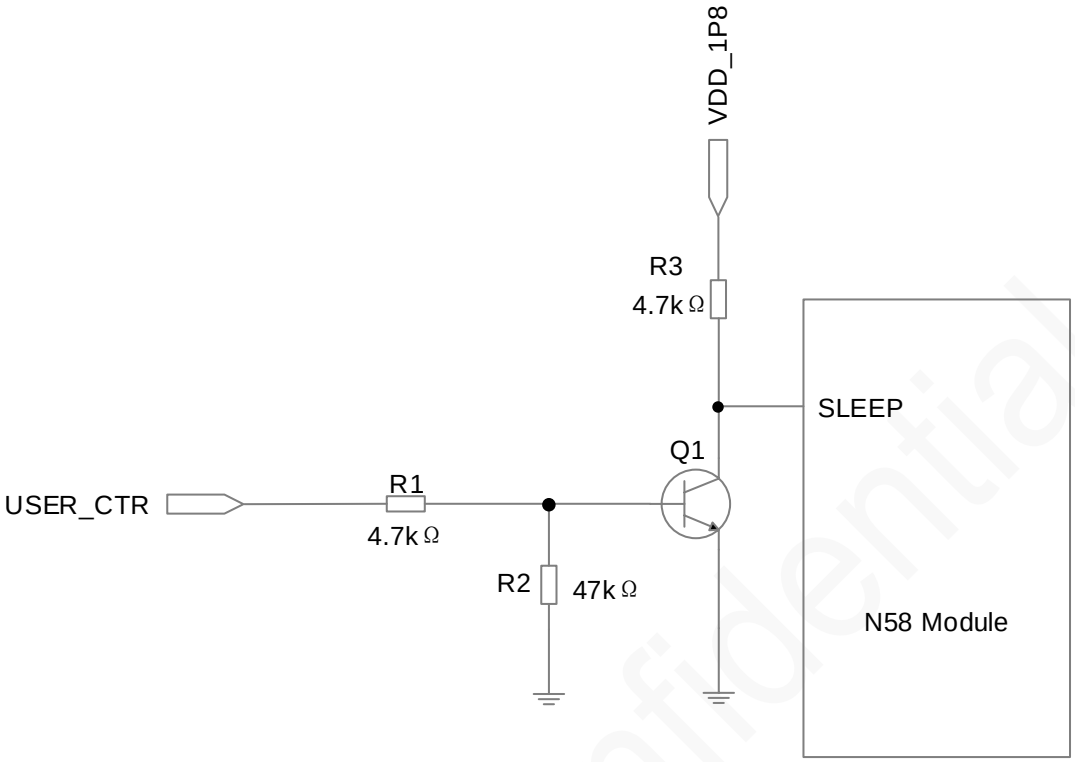


To wake up the module using the SLEEP pin, it is recommended to design your circuit by referring to Figure 5-17.

Enter/exit sleep mode (send "AT+ENPWRSAVE=2" command to the serial interface of the module to enable sleep and wake-up function of the module.)

- Enter into sleep mode: keep USER_CTR low
- Exit from sleep mode: keep USER_CTR high

Figure 5-17 Reference design of module sleep and wake-up control



5.3 Peripheral Interfaces

N58 provides a variety of peripheral interfaces.

In all reference designs in this section, the I/O direction indicated by the module peripheral interface pin name is based on the module, while the peripheral pin naming is based on the peripheral component itself. For example, UART_TXD indicates the pin used by the module to send data, and MCU_RXD indicates the pin used by the MCU to receive data. These two pins should be connected.

In the process of MCU model selection and design, please check the pin naming is based on the module or MCU.

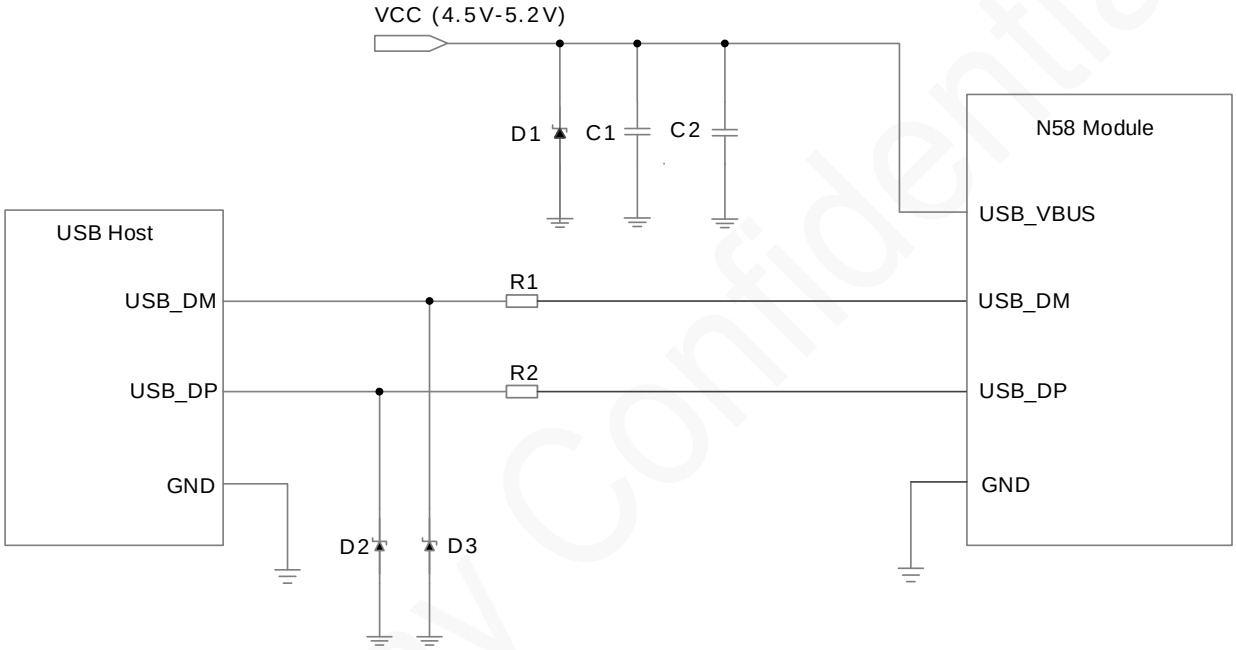
5.3.1 USB

Signal	Pin SN	I/O	Function description	Remarks
USB_VBUS	40	PI	USB insertion detection pin	4.5 V < USB_VBUS < 5.2 V, typical value: 5 V.
USB_DM	41	AIO	USB data -	USB 2.0. This pin is used for software download and data transmission. Route the DM and DP
USB_DP	42	AIO	USB data +	

				traces as differential pairs, and the impedance of the differential pairs is 90 Ω.
USB_ID	43	DI	USB ID pin	Leave this pin open if unused.

N58 can implement program download, data communications, and debugging through the USB interface. Only slave mode is supported for USB of the module, which can be used as required. The recommended USB connection circuit is shown in Figure 5-18.

Figure 5-18 Recommended design of the USB interface



Schematic Design Guidelines

- Connect a 1 μF (C1) and a 33 pF (C2) filter capacitors as well as an ESD component (D1) in parallel to the USB_VBUS trace.
- Ensure that the junction capacitance of the ESD components (D2 and D3) in parallel to the USB_DP and USB_DM traces be smaller than 0.5 pF.
- Resistors of less than 10 Ω are needed in series at the USB_DM and USB_DP pins (R1, R2) to effectively improve the ESD performance of the USB.

PCB Design Guidelines

- Place the filter capacitors (C1, C2) on the USB_VBUS traces as close to the module pins as possible, and place the ESD component (D1) as close to the USB connector as possible.
- Place the paralleled ESD component of the USB_DP and USB_DM traces (D2, D3) as close to the USB connector as possible.

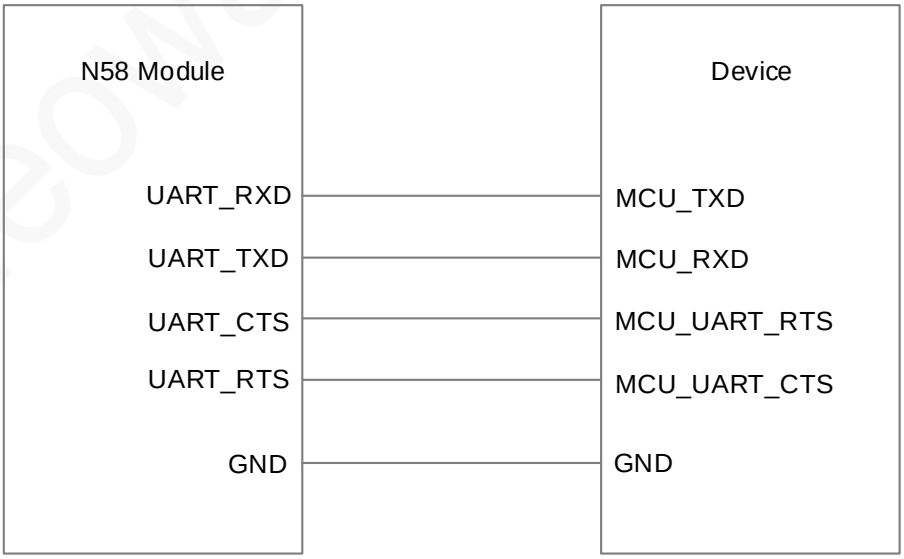
- It is important to route USB signal traces as differential pairs with ground surrounded. The impedance of the USB differential traces should be 90 Ω. The traces from the USB host to the module must be isolated from other signal traces.

5.3.2 UART

Signal	Pin SN	I/O	Function description	Remarks
UART1_TXD	69	DO	UART data output	Software version (Standard): For data transmission. Software version (Open): For data transmission. Note: UART1_CTS (pin #71) can be used to capture CP log.
UART1_RXD	70	DI	UART data input	
UART1_CTS	71	DI	UART clear to send	
UART1_RTS	72	DO	UART ready to send	
UART2_TXD	46	DO	UART data output	Software version (Standard): For communication based on AT commands. Software version (Open): For data transmission.
UART2_RXD	47	DI	UART data input	
UART2_CTS	51	DI	UART clear to send	
UART2_RTS	52	DO	UART ready to send	
UART3_RXD	11	DI	UART data input	For module debugging only.
UART3_TXD	12	DO	UART data output	

N58 provides three UART interfaces, two of which support hardware flow control. They support 1.8 V level and baud rates up to 921600 bps. The following figure shows recommended design of the interface.

Figure 5-19 Reference design of the UART interface



Schematic Design Guidelines

- Pay attention to the correspondence between signal flow direction and connection.
- It is prohibited to use diodes for voltage-level translation.

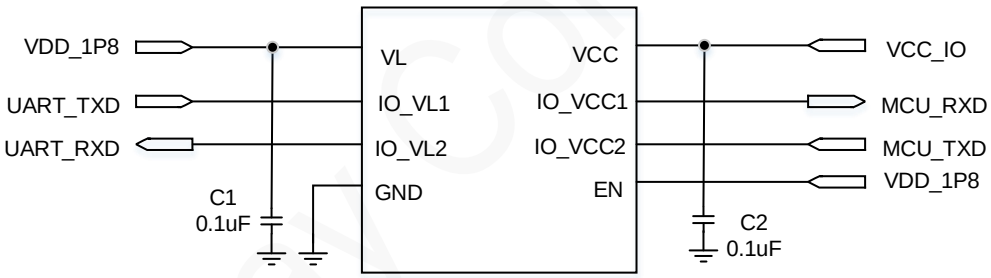
If the the logic voltage of UART does not match that of the MCU, add a voltage-level translation circuit outside the module. Three voltage-level translation circuits are recommended based on the differences in logic levels and rates.

The actual parameter values of the components used in the voltage-level translation circuit should be adjusted according to the actual test results. Note the differences between different circuit voltage-level translation solutions.

- Voltage-level translation chip circuit

  If the UART baud rate is greater than 115200 bps, it is recommended to design the voltage-level translation solution by referring to the recommended voltage-level translation circuit 1. As shown in Figure 5-20.

Figure 5-20 Recommended voltage-level translation circuit 1

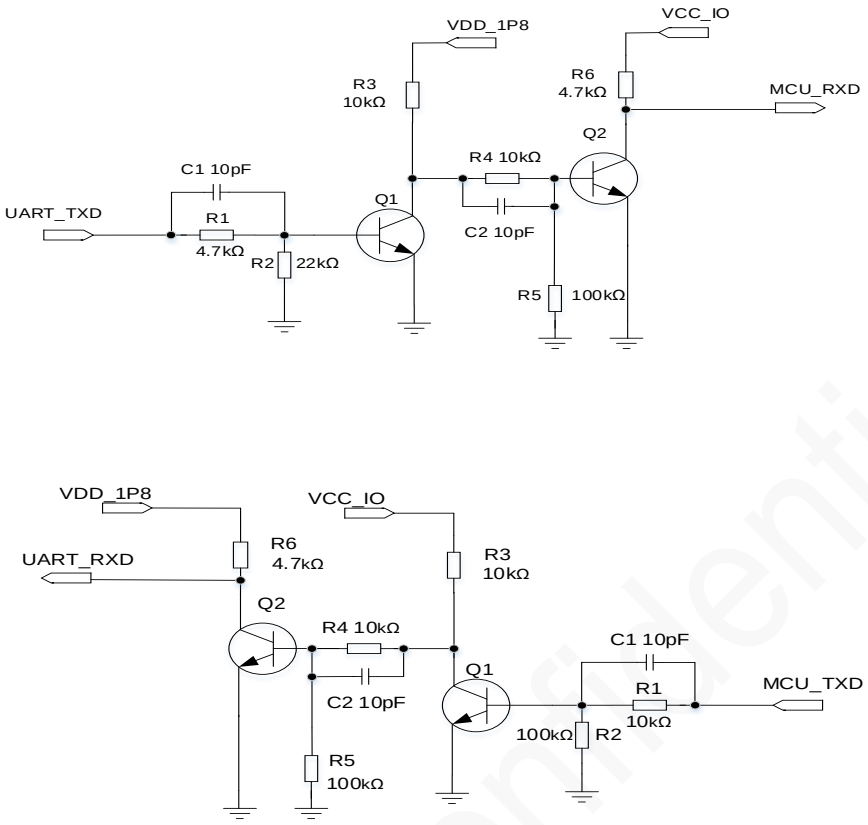


  - VL is the reference voltage for IO_VL1 and IO_VL2, and the voltage range is 1.5 V - 5.5 V.
  - VCC is the reference voltage for IO_VCC1 and IO_VCC2, and the voltage range is 1.5 V - 5.5 V.
  - EN is an enable pin, which works at a voltage of greater than VL-0.2 V. In the above circuit, the EN pin is directly connected to VDD_1P8 and the level translator chip is always working.

- Dual-triode voltage-level translation circuit

  If the UART baud rate is not greater than 115200 bps, it is recommended to design the voltage-level translation solution by referring to the recommended voltage-level translation circuit 2 as shown in Figure 5-21.

Figure 5-21 Recommended voltage-level translation circuit 2



MCU_TXD and MCU_RXD are the sending and receiving ports of MCU respectively, and UART_TXD and UART_RXD are the sending and receiving ports of module respectively. VCC_IO is the IO voltage of MCU and VDD_1P8 is the IO voltage of the module.

The circuit translates the voltage level through conduction and cutoff of the triode, and the dual triode can achieve higher voltage difference after voltage-level translation.

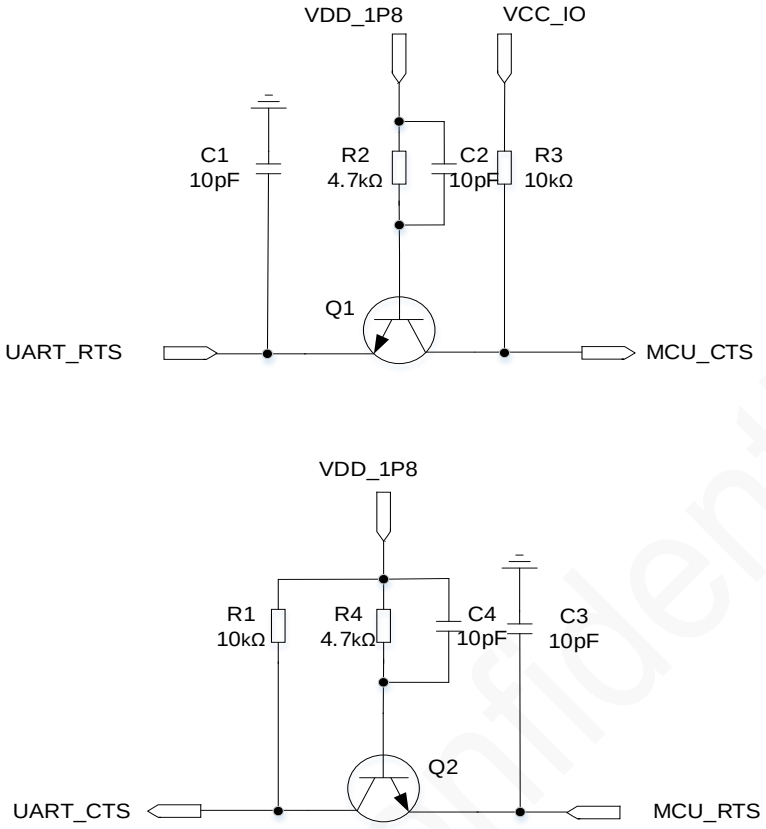
Schematic Design Guidelines

- Ensure that the base voltage of the triode is operating within the temperature range and the transistor can be fully turned on.
- It is recommended to reserve the acceleration capacitor, which can adjust the delay of the voltage-level translation circuit in some cases.

- Single-triode voltage-level translation circuit

  For the CTS/RTS pin, it is recommended to design the voltage-level translation solution by referring to Figure 5-22.

Figure 5-22 Recommended voltage-level translation circuit 3



MCU_CTS and MCU_RTS are the MCU-side signals, while UART_CTS and UART_RTS are the module-side signals. VCC_IO is the IO voltage of MCU and VDD_1P8 is the IO voltage of the module.

This single-triode voltage-level translation circuit is a one-way translation solution that works by conduction and cutoff of the triode. Please note the signal flow direction.

Schematic Design Guidelines

- The voltage difference between the high level and low level does not exceed 2 V.
- It is recommended to reserve the speed-up capacitor and adjust its capacitance value according to actual test results.
- The transistor base voltage is the lower value of the level between both sides.

5.3.3 USIM

Signal	Pin SN	I/O	Function description	Remarks
USIM1_VCC	35	PO	USIM1 power output	Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented.

USIM1_DATA	36	B	USIM1 data input and output	This pin is pulled up to USIM1_VCC via a 4.7 kΩ resistor.
USIM1_CLK	37	DO	USIM1 clock output	-
USIM1_RESET	38	DO	USIM1 reset	-
USIM1_DET	39	DI	USIM1 detection	-
USIM2_VCC	21	PO	USIM2 power output	Both 1.8 V and 3.0 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3.0 V is implemented.
USIM2_DATA	22	B	USIM2 data input and output	This pin is pulled up to USIM2_VCC via a 4.7 kΩ resistor.
USIM2_CLK	23	DO	USIM2 clock output	-
USIM2_RESET	24	DO	USIM2 reset	-
USIM2_DET	25	DI	USIM2 detection	-

N58 provides two USIM card interfaces, which support dual-SIM single-standby, and the card 1 takes precedence by default. Both 1.8 V and 3.0 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3.0 V is implemented. The reference schematic diagram of the USIM card interface is shown in Figure 5-23 and Figure 5-24.

Figure 5-23 Reference design of the USIM interface (normally close connector)

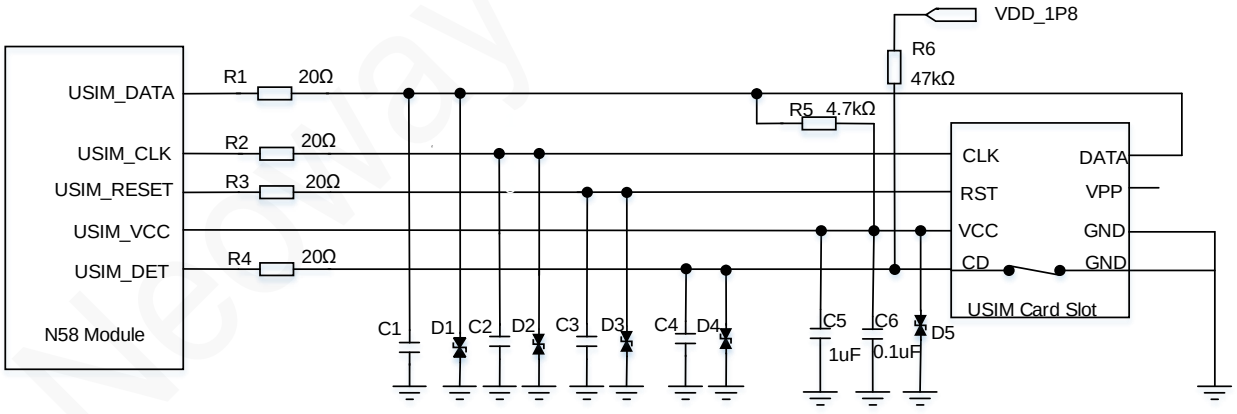
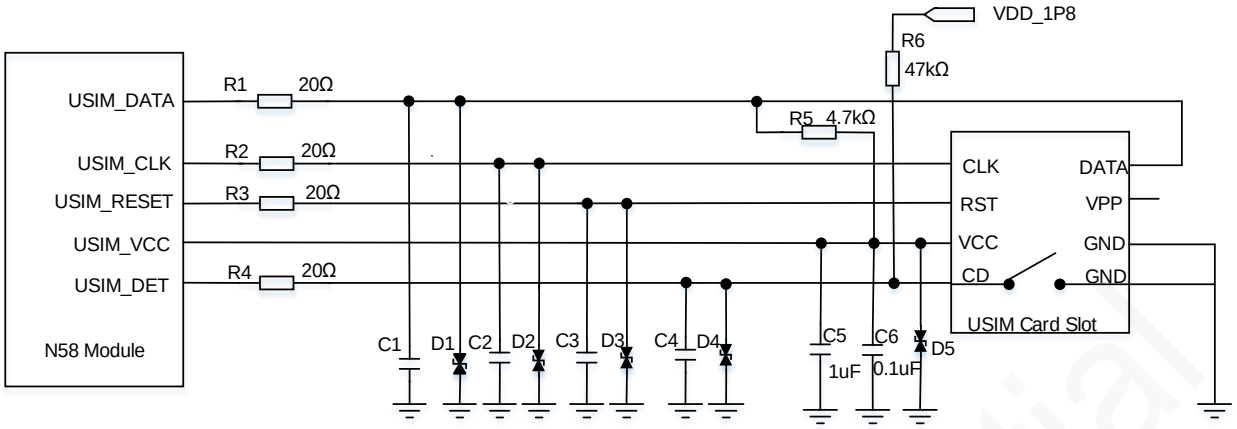


Figure 5-24 Reference design of USIM card interface (normally open connector)

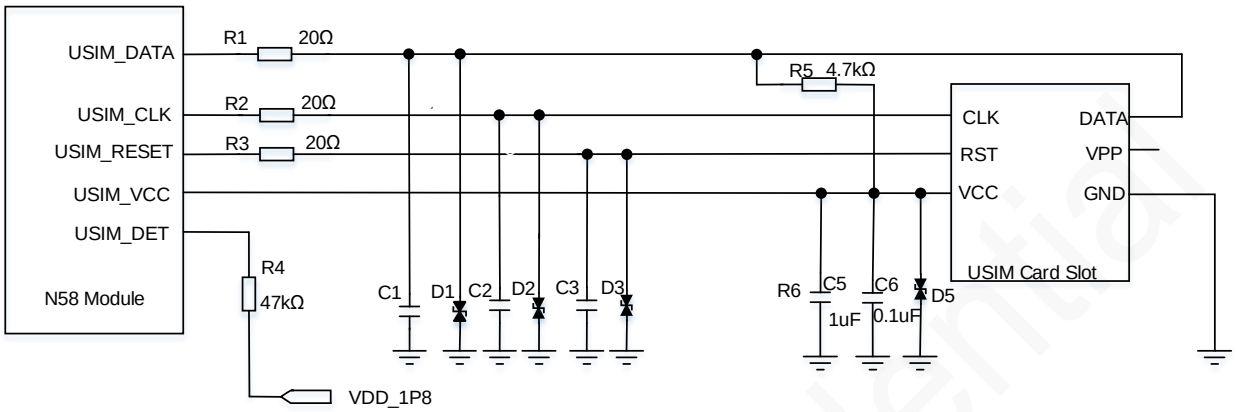


Schematic Design Guidelines

- USIM_VCC is the power supply of the USIM card, with load capacity of up to 50 mA. It is only used as power supply for the USIM card, and shall not supply power to other loads.
- The USIM_DATA pin is not pulled up internally, so connecting it through a 4.7 kΩ external pull-up resistor to USIM_VCC is required.
- USIM_CLK is the clock signal pin for USIM card. The applications in complex electromagnetic environment require ESD protection of high quality, so it is recommended to add ESD protection components (junction capacitance no more than 7 pF) on each signal traces or directly add an integrated ESD device for alternative.
- Resistors of no more than 20 Ω are needed in series at the USIM_DATA, USIM_RESET, USIM_CLK, and USIM_DET pins to enhance ESD performance. The resistors should be placed close to the USIM card slot.
- C1-C4 are design to mount high-frequency filter capacitors on each signal trace, and their capacitance value should be not more than 10 pF. They can be unmounted by default.
- N58 supports USIM card detection, and USIM_DET is a 1.8 V interrupt pin. The USIM detection circuit works by checking the level of the voltage across the USIM_DET pin before and after a USIM card is inserted.
  - For the reference design circuit in Figure 5-23, SIM_DET is grounded before a USIM card is inserted and is pulled up to a 1.8 V voltage after a USIM card is inserted, so the high voltage level means USIM card detected while the low voltage level means no USIM card detected.
  - For the reference design circuit in Figure 5-24, SIM_DET is in a 1.8 V voltage before a USIM card is inserted and is grounded after a USIM card is inserted, so the high voltage level means no USIM card detected while the low voltage level means USIM card detected.

If the USIM hot swap function is not required, the USIM_DET pin must be pulled up to 1.8 V via a 47 kΩ resistor in series, and the USIM hot swap detection function must be disabled in the software. Figure 5-25 shows the reference design of the USIM card interface (without hot swap function) .

Figure 5-25 Reference design of USIM card interface (without hot-swapping function)



PCB Design Guidelines

- USIM signals are like to be jammed by RF radiation, resulting in failure to detect the USIM card. The USIM should be kept far away from the antenna area and RF circuit area.
- Keep USIM card connectors close to the module and keep USIM traces as short as possible.
- On the USIM traces, place the series resistors and ESD protection components close to the USIM card connector.
- To avoid cross-talk between USIM signal traces, surround them with ground.

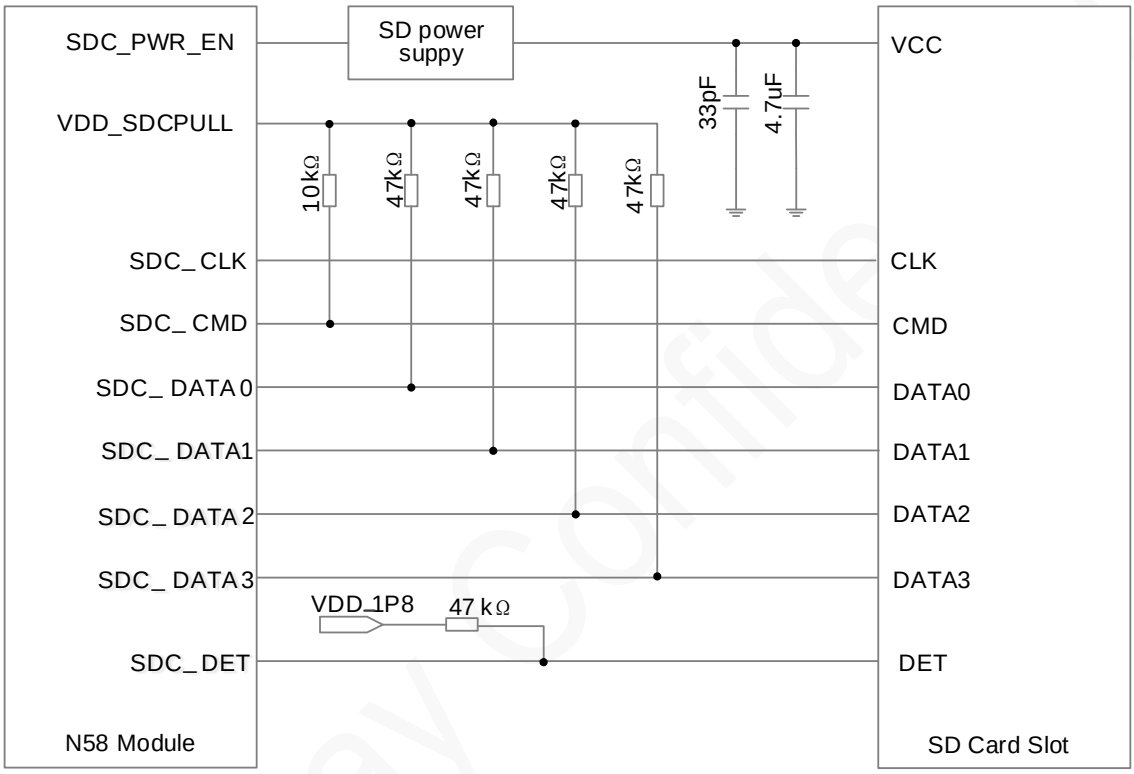
5.3.4 SDIO

Signal	Pin SN	I/O	Function description	Remarks
SDC_PWR_EN	2	DO	SD card power supply enabling	-
SDC_DATA_2	3	B	SD card SDIO bus data 2	-
SDC_DATA_3	4	B	SD card SDIO bus data 3	-
SDC_CMD	5	B	SDIO command	-
SDC_CLK	6	DO	SDIO clock	-
SDC_DATA_0	7	B	SD card SDIO bus data 0	-
SDC_DATA_1	8	B	SD card SDIO bus data 1	-
SDC_DET	96	DI	SD card insertion detect	-
VDD_SDCPULL	103	PO	SD card SDIO bus pull-	It shall not supply power to

	up power supply	other loads. Leave this pin open if unused.

SDIO interface supports dual voltages of 1.8 V / 3.0 V, with clock frequency up to 33.33 MHz. The following shows the reference design.

Figure 5-26 Reference design of the SDIO interface



Schematic Design Guidelines

- VDD_SDCPULL provides dual voltages of 1.8 V / 3.0 V, and can be configured by software according to the SD card voltage. The maximum output current of VDD_SDCPULL is 50 mA. It is only used as pull-up power supply for the SDC data pins and the SDC_CMD pin, and shall not be used for other purposes.
- 2.85 V - 3.2 V (typical value: 3 V) is recommended for SD card power supply, and the current is over 600 mA, which can be provided by LDO or a DC-DC circuit.
- The SD card detection function is implemented by an interrupt, which is triggered by level change at the SDC_DET pin after an SD card is installed in the card connector. According to the structure of the card connector, the effective voltage level of insertion detection can be set as high level or low level by software.

PCB Design Guidelines

- Keep the power trace width greater than 0.5 mm.
- SDIO signal traces should be of equal length on each differential pair. SDC_DATA traces should be matched in length to within 0.5 mm, and the CMD, CLK and DATA traces should be matched in length to within 0.5 mm.
- Spacing between the SDC_DATA traces should be larger than 2 times their trace width.
- Control the impedance for each SDIO signal trace to 50 Ω.

5.3.5 SPI

Signal	Pin SN	I/O	Function description	Remarks
SPI_CLK	84	DO	Clock signal	-
SPI_MISO	85	B	Output of slave device, input of master device	-
SPI_MOSI	86	B	Input of slave device, output of master device	-
SPI_CS_N	87	DO	Chip selection signal of slave device	-

The voltage of SPI interface is 1.8 V, with frequencies up to 50 MHz, and only master mode is supported. The following figure shows the reference design of the SPI interface.

Figure 5-27 Reference design of the SPI interface

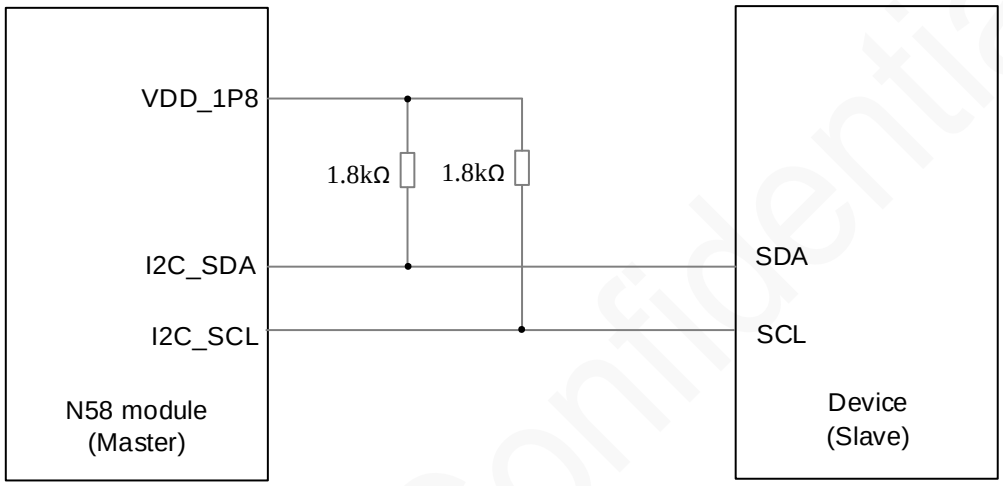
5.3.6 I2C

Signal	Pin SN	I/O	Function description	Remarks
I2C_SDA	81	B	I2C data	This pin is pulled up to VDD_1P8 via a 1.8 kΩ

				resistor.
I2C_SCL	82	DO	I2C clock	This pin is pulled up to VDD_1P8 via a 1.8 kΩ resistor.

N58 provides one 1.8 V I2C interface, supporting only master mode and speed rates up to 3.4 Mbps. Figure 5-28 shows the reference design of the I2C interface.

Figure 5-28 Reference design of I2C interface



5.4 Audio Interfaces

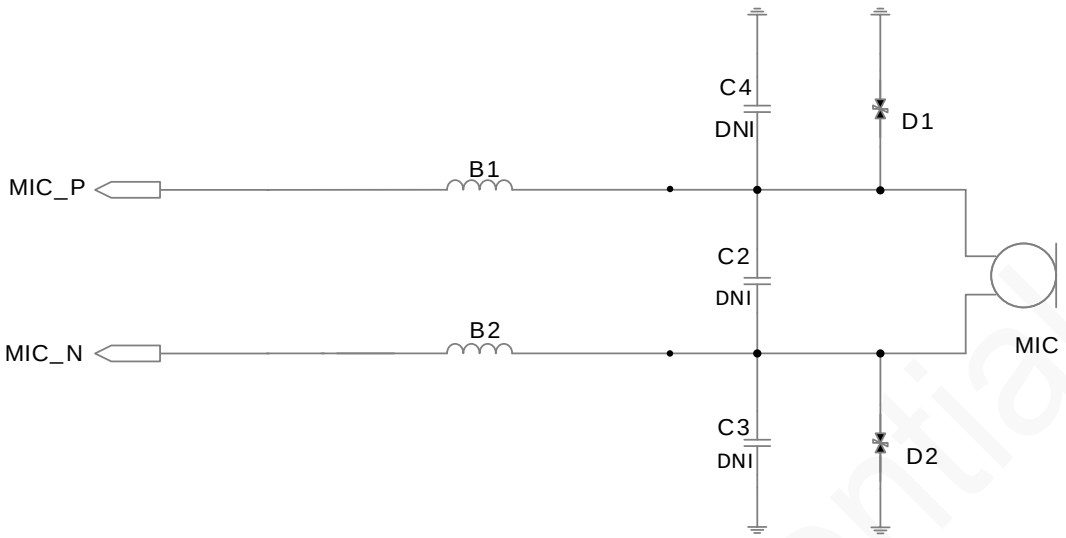
N58 provides audio input and output interfaces (MIC and SPK).

5.4.1 Analog Audio Input Interfaces

Signal	Pin SN	I/O	Function description	Remarks
MIC_P	18	AI	MIC input positive	With internal bias voltage
MIC_N	19	AI	MIC input negative	

N58 supports one differential MIC input with internal bias voltage. The reference design of differential MIC input circuit is shown in the following figure:

Figure 5-29 Reference design of the differential MIC input circuit



Schematic Design Guidelines

- D1 and D2 are designed to mount TVS diodes, which are used to prevent MIC from introducing ESD and damaging the module.
- C2, C3 and C4 are designed to mount filter capacitors, which are mainly used to filter out interference signals and their capacitance values can be adjusted according to actual debugging result.
- B1 and B2 are designed to mount magnetic beads, which are used to filter out high-frequency noise. Magnetic beads with 1800 Ω @ 100 MHz or higher and DC impedance less than 1.5 Ω are preferred. It is recommended to use dedicated magnetic beads for audio.
- It is recommended to use an electret microphone with built-in RF filter dual capacitors (such as 10 pF and 33 pF) to filter RF interference from the source and reduce TDD coupling noise.

PCB Design Guidelines

- MIC_P and MIC_N traces should comply with the differential rules.
- Surround the audio traces with ground. Keep them not less than 3 times the audio trace width away from other signal traces.
- Place RF filter capacitors close to the audio components or pins.
- Keep the audio traces far away from interference sources, such as DC-DC power supply.

5.4.2 Analog Audio Output Interfaces

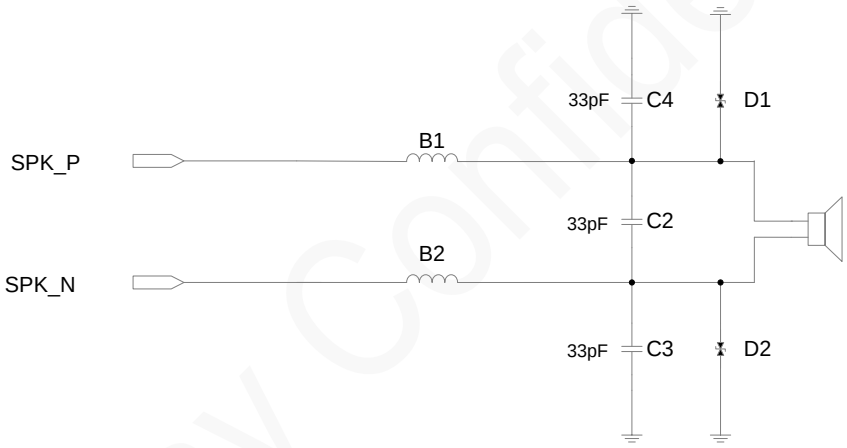
Signal	Pin SN	I/O	Function description	Remarks
SPK_P	15	AO	Speaker output +	Only differential output is supported, with internal Class AB or Class D power
SPK_N	16	AO	Speaker output -	

	amplifier. Maximum output power: Class AB: 600 mW @ 4.2 V, with a 8 Ω load. Class D: 800 mW @ 4.2 V, with a 8 Ω load.

N58 can be designed with internal power amplifier or external power amplifier, and the recommended reference designs are as follows:

Reference Design of Audio interface with Internal Power Amplifier

Figure 5-30 Reference design of audio interface with internal power amplifier



Schematic Design Guidelines

- C2, C3 and C4 are designed to mount filter capacitors, which are used to filter out high-frequency interference.
- D1 and D2 are designed to attach TVS diodes, which are used to prevent ESD from damaging the module.
- B1 and B2 are designed to mount magnetic beads, which are used to filter out high-frequency noise. It is recommended to use dedicated magnetic beads for audio frequency.

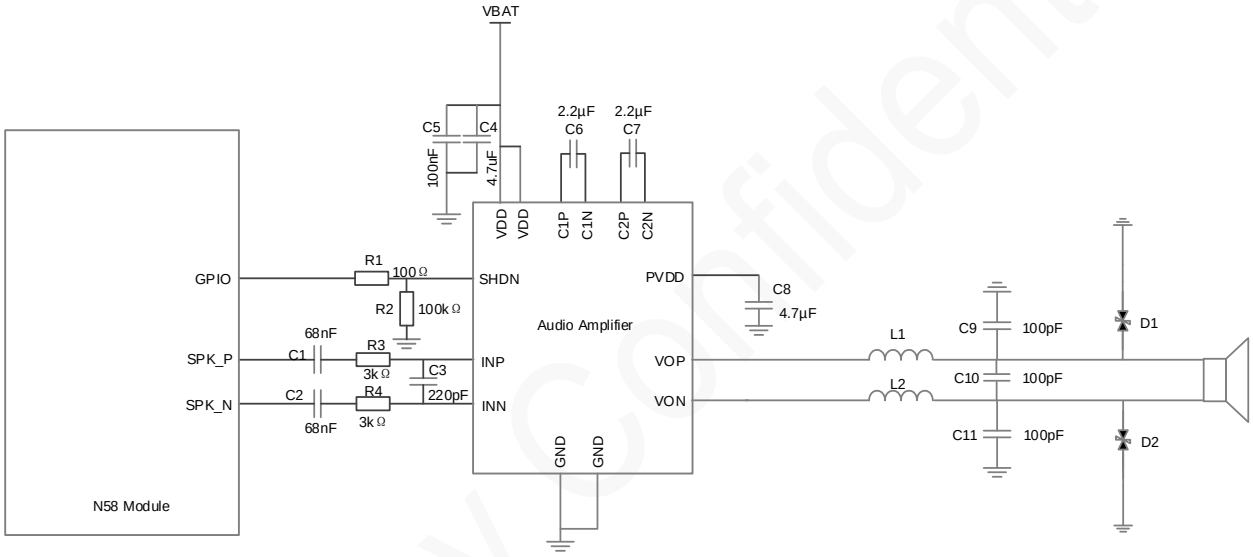
  Special attention should be paid to the DC resistance of the magnetic bead. The impedance of the audio output device is generally small, so if the DC resistance of magnetic bead is too large, too much audio power will be consumed. In principle, the smaller DC resistance of the magnetic bead is preferred. It is recommended to select the magnetic bead with DC resistance less than 0.1 Ω.

PCB Design Guidelines

- The SPK signal traces should be wide enough (0.5 mm is recommended) to bear large current when audios are outputted at a highest volume. Isolate the audio traces from high-speed digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough ground via-holes and ground reference layer protection.
- Keep the audio traces far away from antenna to reduce jamming. Avoid parallel layout between power supply traces and the audio traces.
- It is important to route the audio signal traces as differential pairs.

Reference Design of Audio Interface with External Power Amplifier

Figure 5-31 Reference design of audio interface with external power amplifier



Schematic Design Guidelines

- Connect the SPK output pins to an external power amplifier that supports differential input, and route the their traces in differential pair.
- Note that the current overload capability of L1 and L2 should meet the current demand at maximum power, and a resistance less than 100 mΩ is recommended for DCR.

PCB Design Guidelines

- Ensure that the audio input/output trace width be at least 0.5 mm.
- The analog audio traces should be surrounded with ground and comply with the differential routing rules. Isolate the traces from digital signals and clocks as well as other analog signal traces. No signal trace crossing is allowed. Provide enough ground vias and ground reference plane for protection.

5.5 Video Interfaces

5.5.1 LCD

N58 provides an LCD-dedicated SPI interface, supporting frame rates up to QVGA @ 30fps for LCD display. The following shows the LCD interface pin description.

Table 5-1 LCD interface description

Signal	Pin SN	I/O	Function description	Remarks
LCD_RST_N	63	DO	Reset control	-
LCD_TE	64	DO	Data frame read ready flag	-
LCD_SPI_CS	65	DO	SPI chip selection signal	-
LCD_SPI_CLK	66	DO	SPI clock signal	-
LCD_SPI_SDC	67	B	Data or command control signal	-
LCD_SPI_SIO	68	B	Data input/output	-
LCD_SPI_SEL	73	DO	Selection signal	-
VDD_LCD	138	PO	LCD main power supply is DC 1.8 V by default	With output current up to 200 mA, it can be used for LCD main power supply and interface power supply, but cannot be used as backlight power supply.
LED_K0	139	PI	LED backlight	The anode power supply range is 3.45 V - 4.3 V, and the maximum input current is 50 mA.
LED_K1	140	PI	LED backlight	The anode power supply range is 3.45 V - 4.3 V, and the maximum input current is 50 mA.
LED_K2	141	PI	LED backlight	The anode power supply range is 3.45 V - 4.3 V, and the maximum input current is 50 mA.

5.5.2 Camera

N58 provides a camera-dedicated SPI interface, supporting frame rates up to VGA@15 fps for cameras.

The following shows the camera interface description.

Table 5-2 Camera interface description

Signal	Pin SN	I/O	Function description
VDD_CAM	53	PO	Camera digital power supply is 1.8 V by default.
CAM_RST_N	54	DO	Reset signal
CAM_SPI_DATA0	55	B	Data signal input
CAM_SPI_DATA1	56	B	Data signal input
CAM_SPI_CLK	57	DO	SPI clock signal
CAM_I2C_SDA	58	B	I2C data
CAM_I2C_SCL	59	DO	I2C clock
CAM_PWDN	60	DO	Power-off control
CAM_MCLK	61	DO	Master clock signal
AVDD_CAM	62	PO	Camera analog power supply This power supply is disabled by default. If enabled, its output is 1.8 V / 100 mA.

5.6 Other Functional Interfaces

5.6.1 ADC

The module provides a 12-bit ADC channel, with detectable voltage range 0.1 V - VBAT, which can be used for temperature detection and other related detections. Please refer to *Neoway_N58_AT_Commands_Manual* for details.

Signal	Pin SN	I/O	Function description	Remarks
ADC1	88	AI	General analog-to-digital signal	-

5.6.2 NET_LIGHT

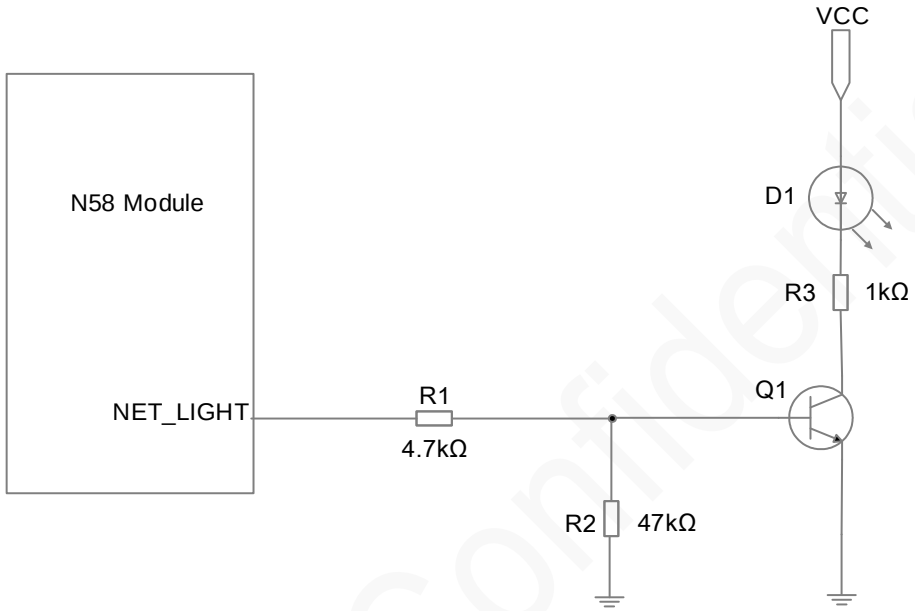
Signal	Pin SN	I/O	Function description	Remarks
NET_LIGHT	83	DO	Network indication control	-

NET_LIGHT is the indication pin of module network status. It can output PWM waveforms with different duty cycles according to different operating states during module operation, and drive LED indicators

to flash at different frequencies. Through AT+SIGNAL command, the LED indicator can be set to flash according to different states. Please refer to *Neoway_N58_AT_Commands_Manual* for details.

Do not use these indication pins to drive the LED indicator directly since they output a high level of 1.8 V. It is recommended to drive the LED indicator by controlling a triode. The following figure shows the recommended reference design.

Figure 5-32 Driving LED indicators with a triode



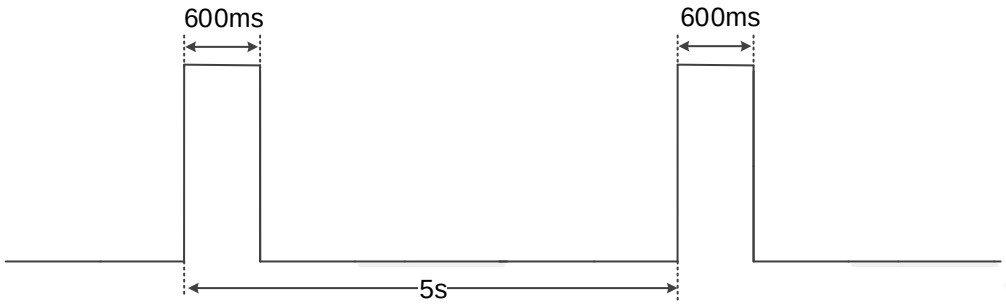
5.6.3 RING

Signal	Pin SN	I/O	Function description	Remarks
RING	13	DO	Incoming call & SMS indicator control	-

- Incoming call RING indication

  Once a voice call is incoming, the UART port outputs "RING" character strings and meanwhile the RING pin outputs high-level pulses with a pulse width of 600 ms in a period of 5 seconds. After the call is answered, the pin restores to low level, as shown in the following figure.

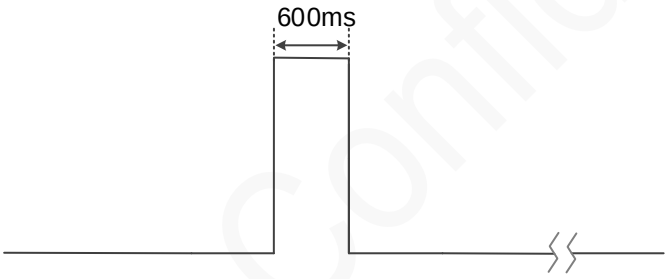
Figure 5-33 Incoming call RING indication



- SMS RING indication

  Once an SMS message is received,the RING pin outputs high-level pulses with a pulse width of 600 ms for indication, as shown in the following figure.

Figure 5-34 SMS RING indication

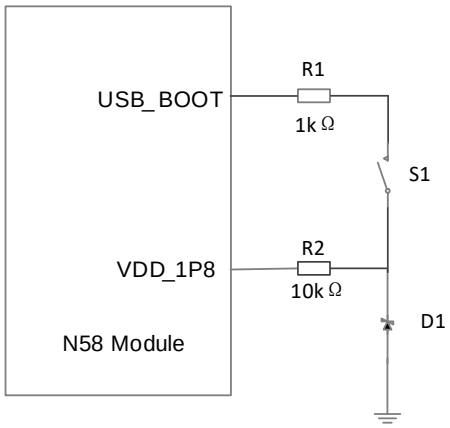


5.6.4 USB_BOOT

Signal	Pin SN	I/O	Function description	Remarks
USB_BOOT	48	DI	Emergency download pin	-

N58 provides a USB_BOOT pin, which is used to enter the emergency download mode. After the USB_BOOT pin is pulled up to VDD_1P8 before the module is powered up, the module can enter the emergency download mode when it is powered on. This method is used as an emergency solution for product startup failure or malfunction. To facilitate the subsequent software upgrade and debugging of the product, it is recommended to reserve this pin. The following figure shows the reference design of this pin. Adding an ESD component to protect USB_BOOT in the circuit is required.

Figure 5-35 Reference design of USB_BOOT pin



5.6.5 VBACKUP and VRTC

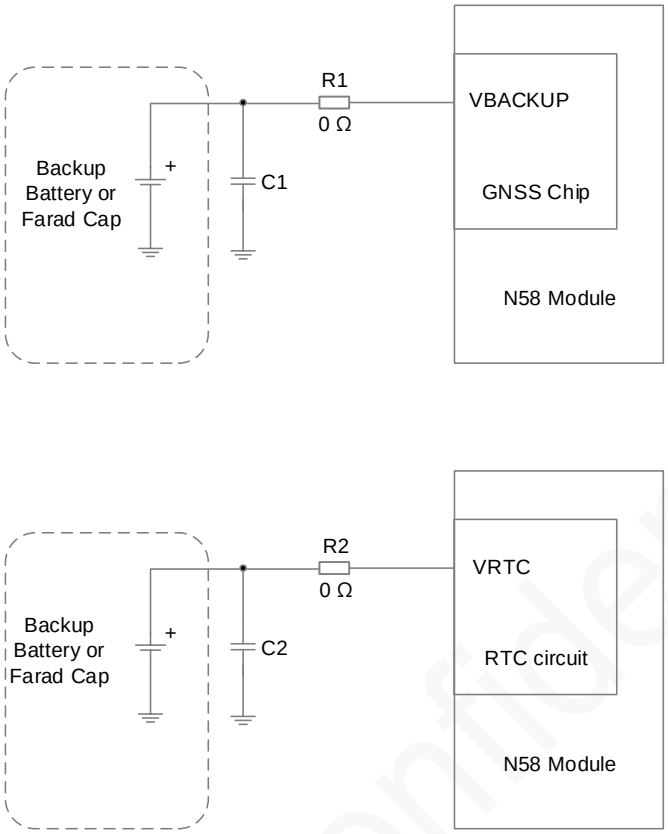
Signal	Pin SN	I/O	Function description	Remarks
VBACKUP	105	PI	GNSS backup power supply	-
VRTC	113	PI	RTC power supply	-

VBACKUP supplies power for the RTC and RAM of the GNSS unit circuit. The voltage ranges from 3.0 V to 3.3 V. Leave this pin open if unused. To use the hot start function of the GPS and save the positioning data, connect it to a backup power supply to prevent the power supply from disconnecting. Otherwise, the GPS is cold started every time.

VRTC is the backup power pin and can be connected to a button battery or Farad capacitor to supply power for RTC. It can supply power in a short time after the VBAT is disconnected to keep the RTC working. The power supply voltage ranges from 2.8 V to 3.2 V and the typical voltage is 3.0 V.

The following shows the reference design of the VRTC power supply.

Figure 5-36 Reference design of the VBACKUP and VRTC power supply



5.6.6 GPIO

Signal	Pin SN	I/O	Function description	Remarks
GPIO_0	50	B	GPIO with interrupt	Leave this pin open if unused.
GPIO_2	80	B	GPIO with interrupt	Leave this pin open if unused.
GPIO_3	78	B	GPIO with interrupt	Leave this pin open if unused.

N58 provides three GPIO interfaces, all with the interrupt function.

5.6.7 GNSS_LNA_EN

Signal	Pin SN	I/O	Function description	Remarks
GNSS_LNA_EN	90	DO	GNSS LNA enabling	Leave this pin open if unused.

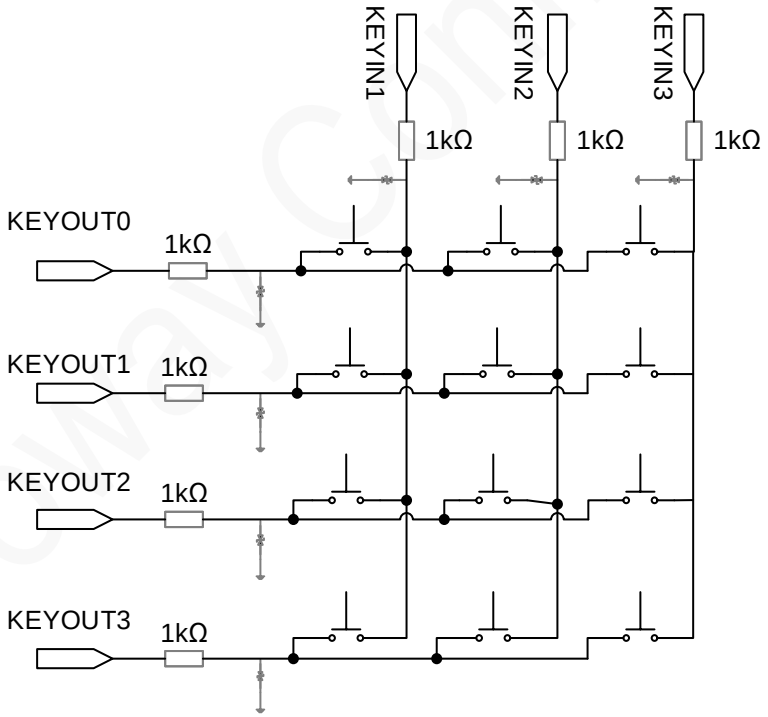
N58 provides an enabling control pin for an external GNSS low-noise amplifier.

5.6.8 Keypad

N58 supports a 4x3 matrix keypad. The following shows the pin definitions.

Signal	Pin SN	I/O	Function description	Remarks
KEYOUT3	130	DO	Key output	Leave this pin open if unused.
KEYOUT2	131	DO	Key output	Leave this pin open if unused.
KEYOUT1	132	DO	Key output	Leave this pin open if unused.
KEYOUT0	133	DO	Key output	Leave this pin open if unused.
KEYIN1	134	DI	Key input	Leave this pin open if unused.
KEYIN2	135	DI	Key input	Leave this pin open if unused.
KEYIN3	136	DI	Key input	Leave this pin open if unused.

Figure 5-37 Keypad reference design



Schematic Design Guidelines

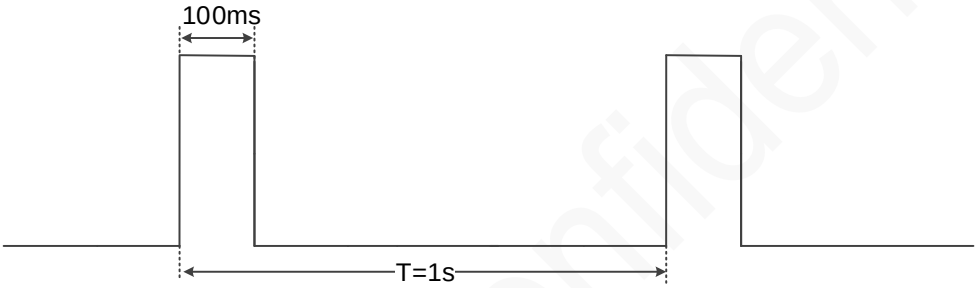
To improve the ESD performance of the keypad, ESD protection components are required, and a 1 kΩ series resistor should be connect between the pins of the keypad and each of the key output/input end.

5.6.9 1PPS

Signal	Pin SN	I/O	Function description	Remarks
1PPS	89	DO	GNSS timing output	Timing precision is less than 30 ns. This function is only for the N58 module versions with GNSS.

The 1PPS interface is used for GNSS timing and supports a time precision less than 30 ns. The output signal is a pulse signal with an amplitude of 3 V and a duty cycle of 10%. The schematic diagram of 1PPS output waveform is shown in Figure 5-38.

Figure 5-38 Schematic diagram of 1PPS output waveform



For the N58 module versions without GNSS, the 1PPS pin can be used as ADC pin. The detectable voltage range is 0.1 V - VBAT with a 12-bit ADC precision.

5.7 RF Interfaces

Signal	Pin SN	I/O	Function description	Remarks
ANT_MAIN	76	-	2G/4G main antenna pin	Requiring 50 Ω impedance characteristic.
ANT_GNSS	92	-	GNSS antenna pin	
ANT_BT	94	-	Bluetooth antenna pin	

5.7.1 ANT_MAIN Antenna Interface

For the module to be applicable to your PCB, the characteristic impedance of the antenna interface should be controlled at 50 Ω and the impedance of the trace from the module's antenna interface to the antenna needs to be kept at 50 Ω to allow reception of radio frequency (RF) signals. In the circuit design, a matching network is essential for antenna matching in the circuit design. The matching

network is generally divided into three types: L type, T type, and π type, which are shown in the following figure. The π-type matching circuitry is preferred.

Figure 5-39 L-type RF matching schematics

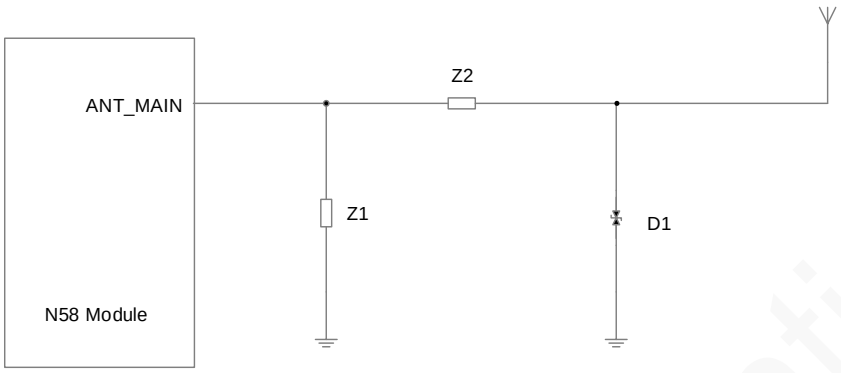


Figure 5-40 T-type RF matching schematics

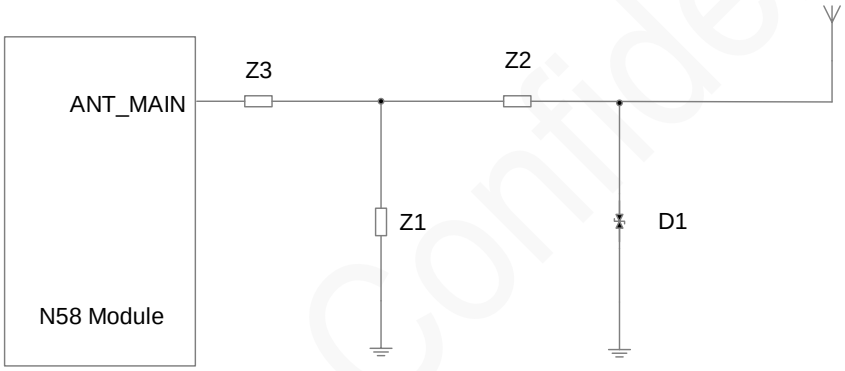
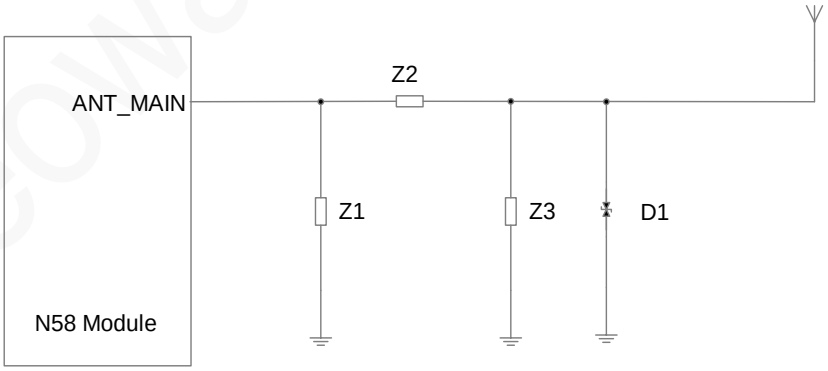


Figure 5-41 π-type RF matching schematics



Schematic Design Guidelines

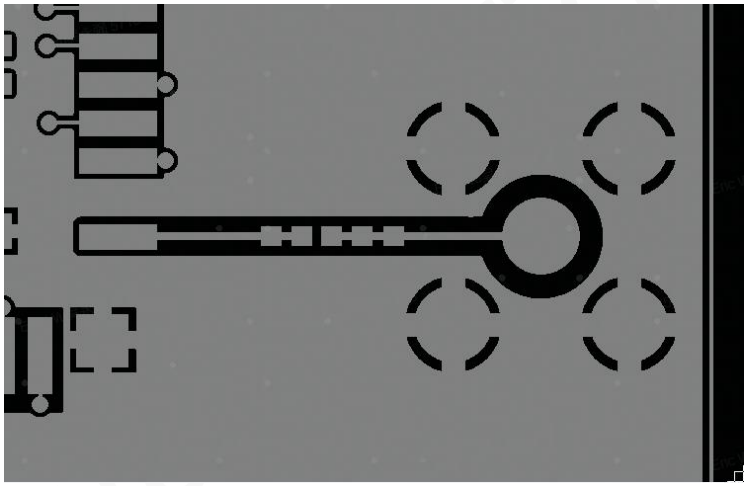
- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.

- If static electricity may be introduced through the antenna, it is recommended to add ESD components with ultra-low junction capacitance for static electricity protection. TVS diodes with junction capacitance less than 0.5 pF are preferred. Besides, it is necessary to ensure that the reverse breakdown voltage of TVS diodes is greater than 10 V, and TVS diodes with reverse breakdown voltage above 15 V are preferred.

PCB Design Guidelines

- Lay grounding copper foil around the RF traces and provide a dense line of ground via-holes along the RF traces for isolation.
- Keep the RF traces as short as possible and control their characteristic impedance at 50 Ω
- To avoid antenna performance being affected significantly by the parasitic capacitance of a large RF pad when using SMA connector, remove the copper on the first and fourth layers or all layers of a multiple-layer PCB under the RF solder pad. The following is the recommended RF PCB design.

Figure 5-42 Recommended RF PCB design



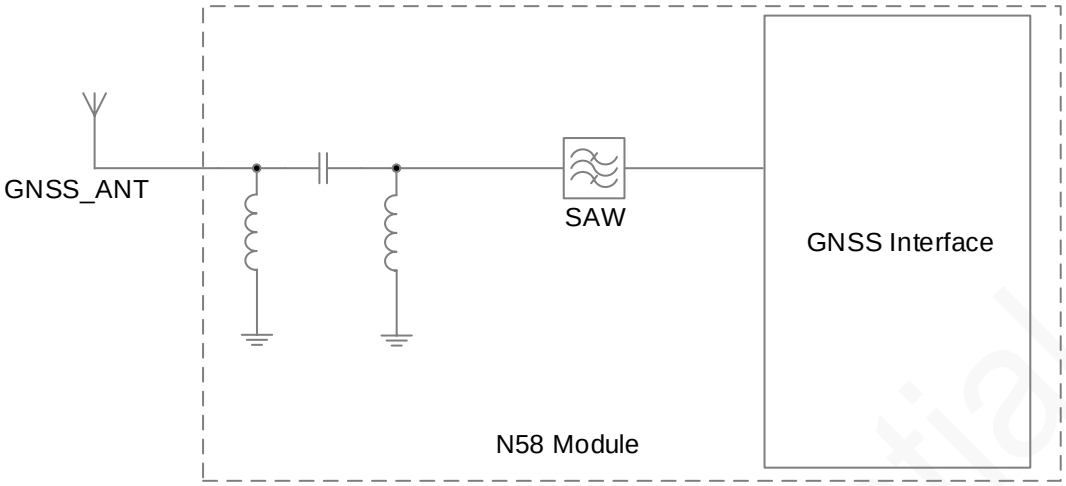
- Keep a proper distance between ANT_MAIN, ANT_GNSS and ANT_BT to avoid mutual interference that may affect the receiving performance.
- On the PCB, keep the RF signals and components far away from digital circuits, switching power supplies, power transformers, power inductors, clock signals, etc.

5.7.2 ANT_GNSS Interface

GNSS Impedance Control

ANT_GNSS (pin #92) is the GNSS RF interface of the module, which requires a characteristic impedance of 50 Ω. The following shows the GNSS structure inside the module.

Figure 5-43 GNSS RF structure



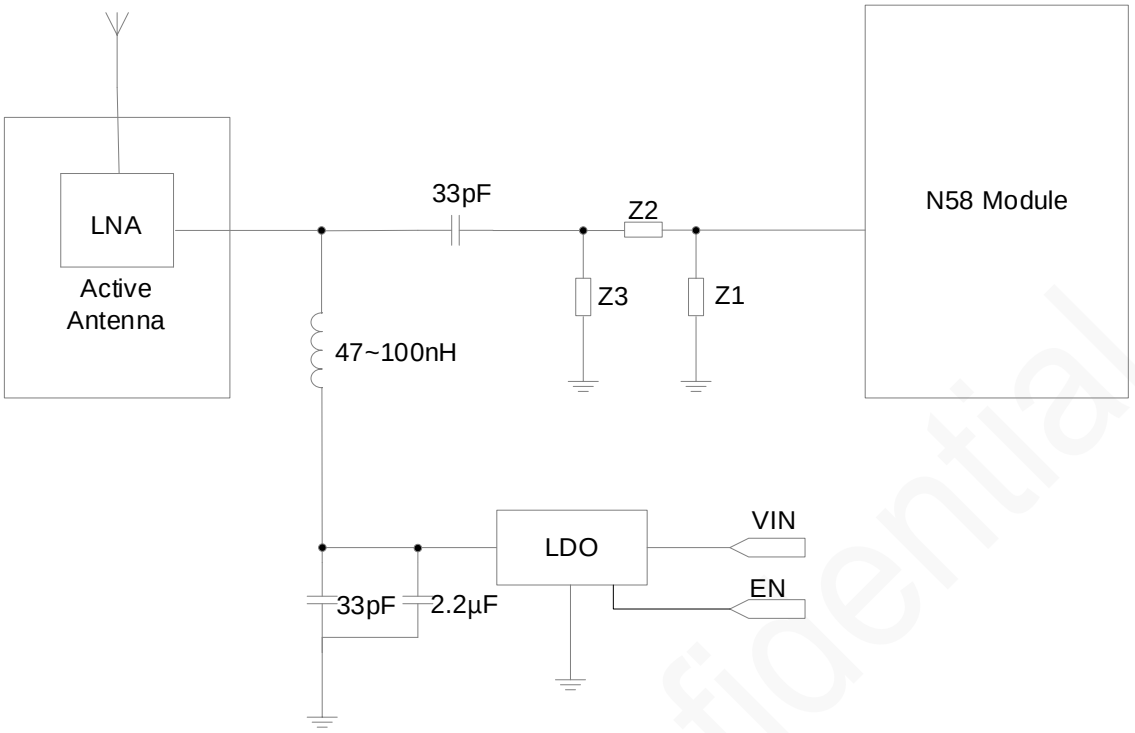
Schematic Design Guidelines

- For the matching circuitry between the module interface and GNSS antenna, please refer to the principle design in section 5.7.1 ANT_MAIN Antenna Interface.
- There is no LNA inside the module. If passive GNSS antenna is used, LNA needs to be added near the antenna feeder. The GNSS_LNA_EN pin of the module can be used for external LNA enabling.

Reference design of active GNSS antenna

After the GNSS antenna receives GNSS satellite signals, the signals are amplified by the front LNA (Low Noise Amplifier) inside the active antenna and then sent to the ANT_GNSS pin of the module through the feeder and PCB traces. The following figure shows the reference design of the active GNSS antenna.

Figure 5-44 Reference design of active GNSS antenna



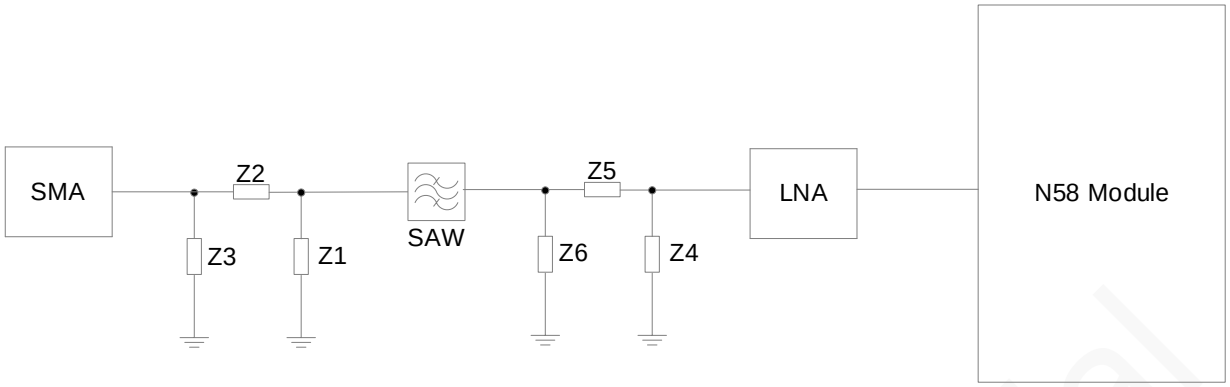
PCB Design Guidelines

- For cautions of PCB design between GNSS interface and antenna, refer to the PCB design guidelines in section 5.7.1 ANT_MAIN Antenna Interface.
- 50 Ω impedance control is required for both antenna feeders and the PCB traces between the antenna interface and LNA, and the traces should not be too long. The power supply of the active antenna is fed via an inductor of 47 nH - 100 nH from the signal line of the antenna.
- The common active antenna requires a 3.3 V to 5 V power supply. The active antenna itself consumes less power, but it requires LDO with a low noise coefficient to supply power to the antenna through an inductor of 100NH, as shown in the figure above.
- Keep the GNSS RF circuit away from the main and BT antenna circuits as far as possible on PCB. Otherwise, the RF performance may be affected.

Reference design of passive GNSS antenna

After the GNSS antenna receives the GNSS satellite signal, it is transmitted to the ANT_GNSS pin of the N58 module through the PCB traces. The following figure shows a reference design of the passive GNSS antenna.

Figure 5-45 Reference design of passive GNSS antenna



PCB Design Guidelines

- For cautions of PCB design between the GNSS interface and the antenna, refer to the PCB design guidelines in 5.7.1 “ANT_MAIN Antenna Interface”.
- Keep the GNSS RF circuit away from the main and BT antenna circuits as far as possible on your application PCB. Otherwise, the RF performance may be affected.

5.7.3 ANT_BT Interface

The pin #94 of the module is Bluetooth antenna interface, with a characteristic impedance of 50 Ω.

For the schematic diagram design and PCB design of Bluetooth antenna interface, please refer to the requirements in section 5.7.1 ANT_MAIN Antenna Interface.

This interface is also for Wi-Fi signal receiving, and it can support Wi-Fi and BT/BLE at the same time depending on the application scenario.

5.7.4 Antenna Assembling

The antenna used by the module must comply with the mobile device standard. The standing wave ratio should be between 1.1 and 1.5, and the input impedance should be 50 Ω. Requirements for antenna gain vary according to the application environment. You can choose an appropriate antenna according to specific application scenarios and environments.

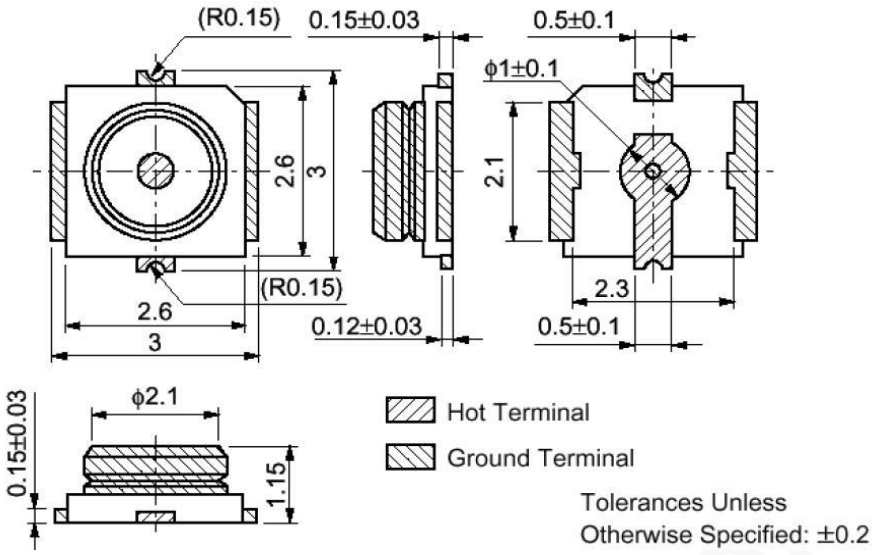
The module antenna interface can be connected with rubber rod antenna, sucker antenna or internal Picofarad antenna, and good shielding is required between the external antenna and the RF pin. While using an external RF antenna, keep the external RF cables far away from all interference sources, especially digital signals and switching power supply.

The following methods are commonly used to assemble antennas:

- Reference design for external antennas (GSC RF connector)

  MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

Figure 5-46 Murata RF connector encapsulation specifications



- Connecting to an external antenna by soldering

  It is not recommended to solder the RF cables to the module directly since the stability, consistency, and RF performance are not good.

  The following show the two types of connections.

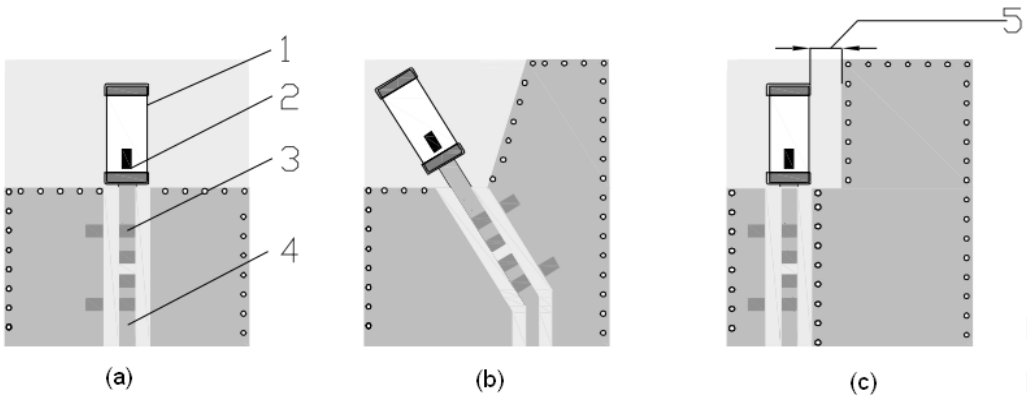
Figure 5-47 RF cable connections

- PCB printing or SMT

  The module works in a wide frequency range, but it is difficult for PCB antennas or ceramic antennas to cover a wide frequency. Therefore, this connection method is recommended only for 2.4 GHz Wi-Fi or BT/ BLE antennas.

The following figure shows the layout of the 2.4 GHz ceramic chip antenna. SLDA52-2R540G-S1TF is used as an example.

Figure 5-48 Antenna layout

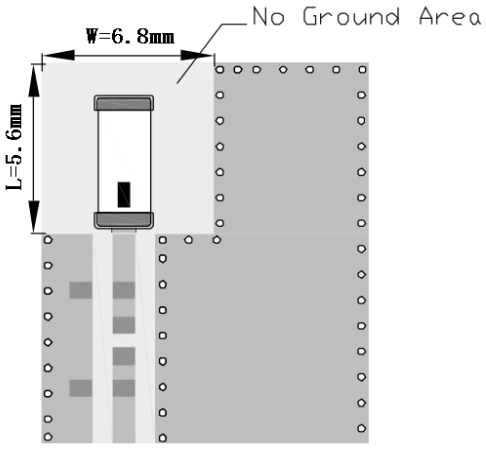


If your PCB is large enough, you can adopt the layout shown in Figure 5-48 (a).

- 1 Chip antenna
- 2 Feeding mark
- 3 Solder pad of the matching circuitry
- 4 50 Ω characteristic impedance RF trace

Figure 5-49 shows the "No Dround Area" between the antenna and ground that is marked as "5" in Figure 5-48.

Figure 5-49 Clearance area (No Ground Area) around the antenna on the PCB board



For more details, please refer to the antenna manual and instruction documentation.

6 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

6.1 Electrical Characteristics

- If the voltage is lower than the threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it outputs at least 2.5 A current. The 2.5 A current corresponds to the maximum power level of the module at GSM mode, and the peak current during burst transmission lasts for a short time. Placing a large capacitor at the VBAT pin of the module can effectively enhance the freewheeling current of the power supply and avoid abnormalities such as module shutdown caused by excessive voltage drop.

Table 6-1 Electrical characteristics

Parameter		Minimum value	Typical value	Max. value
VBAT	V_{in}	3.4 V	3.8 V	4.2 V
	I_{in}	N/A	N/A	2.5 A

Table 6-2 Current consumption (typical)

States / Frequency band	Sleep (mA)	Idle (mA)	Active (mA) @ max power
FDD-LTE: B1, B2, B3, B4, B5, B7, B8, B20, B28, B66	< 3 mA	< 16 mA	< 600 mA
TDD-LTE: B34, B38, B39, B40, B41	< 3 mA	< 16 mA	< 340 mA
GSM900/850	< 3 mA	< 15 mA	< 170 mA
GSM1800/1900	< 3 mA	< 15 mA	< 170 mA

6.2 Temperature Characteristics

Parameter	Minimum value	Typical value	Max. value
Operating	-30℃	25℃	75℃
Extended	-40℃	25℃	85℃
Storage	-40℃	25℃	90℃

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse and cannot meet the requirements of 3GPP specification, but it will not have a great impact on the normal use of the module. After the temperature is restored, the RF performance can be restored to meet the 3GPP specification.

6.3 ESD Protection Characteristics

As electronic products need to undergo strict ESD testing, the following items are the electrostatic protection capabilities of the main pins of the module. When designing related products, you need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25℃

Table 6-3 ESD Protection Characteristics

Test point	Contact discharge	Air discharge
GND	±8 kV	±15 kV
ANT	±8 kV	±15 kV
Shielding cover	±8 kV	±15 kV

The above test data are obtained from the test using a N58_Mini_EVB of Neoway.

7 RF Characteristics

N58 provides data connectivity on GSM, FDD-LTE (Cat 1), TDD-LTE (Cat 1) networks. It supports Wi-Fi positioning, BT/BLE wireless connection, and optional GNSS. This chapter introduces the RF characteristics of N58.

7.1 Operating Frequency Bands

Table 7-1 Operating frequency bands

Operating band	Uplink	Downlink
GSM850	824 - 849 MHz	869 - 894 MHz
EGSM900	880 - 915 MHz	925 - 960 MHz
DCS1800	1710 - 1785 MHz	1805 - 1880 MHz
PCS1900	1850 - 1910 MHz	1930 - 1990 MHz
FDD-LTE B1	1920 - 1980 MHz	2110 - 2170 MHz
FDD-LTE B2	1850 - 1910 MHz	1930 - 1990 MHz
FDD-LTE B3	1710 - 1785 MHz	1805 - 1880 MHz
FDD-LTE B4	1710 - 1755 MHz	2110 - 2155 MHz
FDD-LTE B5	824 - 849 MHz	869 - 894 MHz
FDD-LTE B7	2500 - 2570 MHz	2620 - 2690 MHz
FDD-LTE B8	880 - 915 MHz	925 - 960 MHz
FDD-LTE B20	832 - 862 MHz	791 - 821 MHz
FDD-LTE B28	703 - 748 MHz	758 - 803 MHz
FDD-LTE B66	1710 - 1780 MHz	2110 - 2200 MHz
TDD-LTE B34	2010 - 2025 MHz	2010 - 2025 MHz
TDD-LTE B38	2570 - 2620 MHz	2570 - 2620 MHz
TDD-LTE B39	1880 - 1920 MHz	1880 - 1920 MHz
TDD-LTE B40	2300 - 2400 MHz	2300 - 2400 MHz
TDD-LTE B41	2535 - 2655 MHz	2535 - 2655 MHz

7.2 TX Power and RX Sensitivity

Table 7-2 RF transmit power

Frequency band	Max power	Min. power
GSM850	33 dBm ± 2 dB	5 dBm ± 2 dB
EGSM900	33 dBm ± 2 dB	5 dBm ± 2 dB
DCS1800	30 dBm ± 2 dB	0 dBm ± 2 dB
PCS1900	30 dBm ± 2 dB	0 dBm ± 2 dB
FDD-LTE B1	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B2	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B3	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B4	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B5	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B7	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B8	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B20	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B28	23 dBm ± 2 dB	< -40 dBm
FDD-LTE B66	23 dBm ± 2 dB	< -40 dBm
TDD-LTE B34	23 dBm ± 2 dB	< -40 dBm
TDD-LTE B38	23 dBm ± 2 dB	< -40 dBm
TDD-LTE B39	23 dBm ± 2 dB	< -40 dBm
TDD-LTE B40	23 dBm ± 2 dB	< -40 dBm
TDD-LTE B41	23 dBm ± 2 dB	< -40 dBm

Table 7-3 RX sensitivity

Frequency band	RX sensitivity
GSM850	≤ -108 dBm
EGSM900	≤ -108 dBm
DCS1800	≤ -108 dBm
PCS1900	≤ -108 dBm
FDD-LTE B1	≤ -97 dBm
FDD-LTE B2	< -97 dBm

FDD-LTE B3	≤ -97 dBm
FDD-LTE B4	< -97 dBm
FDD-LTE B5	≤ -97 dBm
FDD-LTE B7	≤ -95 dBm
FDD-LTE B8	≤ -98 dBm
FDD-LTE B20	≤ -97 dBm
FDD-LTE B28	≤ -97 dBm
FDD-LTE B66	< -97 dBm
TDD-LTE B34	< -98 dBm
TDD-LTE B38	≤ -98 dBm
TDD-LTE B39	≤ -98 dBm
TDD-LTE B40	≤ -98 dBm
TDD-LTE B41	≤ -98 dBm

The preceding indicators are tested in a shielded environment in a laboratory. The LTE band indicators are the test results when the bandwidth is 10 MHz, the modulation mode is QPST and RB is set according to the protocol. On no-shielded environments, deviations may exist in the receiver sensitivity of some individual bands due to the interference.

7.3 GNSS Technical Parameters

Table 7-4 GNSS technical parameters

Parameter	Notice
GPS L1 operating frequency	1575.42±1.023 MHz
GLONASS operating frequency	1597.5 - 1605.9 MHz
BDS operating frequency	1559.1 - 1563.1 MHz
Tracking sensitivity	-160 dBm
Acquisition sensitivity	-154 dBm
Positioning accuracy (open space)	< 3 m (CEP50)
Hot start (open space)	≤ 1s
Cold start (open space)	< 33s
Update frequency	< 10 Hz

Max. positioning altitude	18000m
Max. positioning speed	515 m/s
Max. positioning acceleration	1G
CNRin/CNRout	3 dB
GNSS data type	NMEA-0183
GNSS antenna type	Passive/active antenna

Tracking sensitivity and acquisition sensitivity are the results of signaling test on SPIRENT 6300. The values are the maximum values obtained from multiple measurements performed on samples. No external LNA, active antenna and other signal amplification measures are used during the test.

7.4 WLAN/BT Characteristics

Table 7-5 WLAN/ BT TX power and RX sensitivity

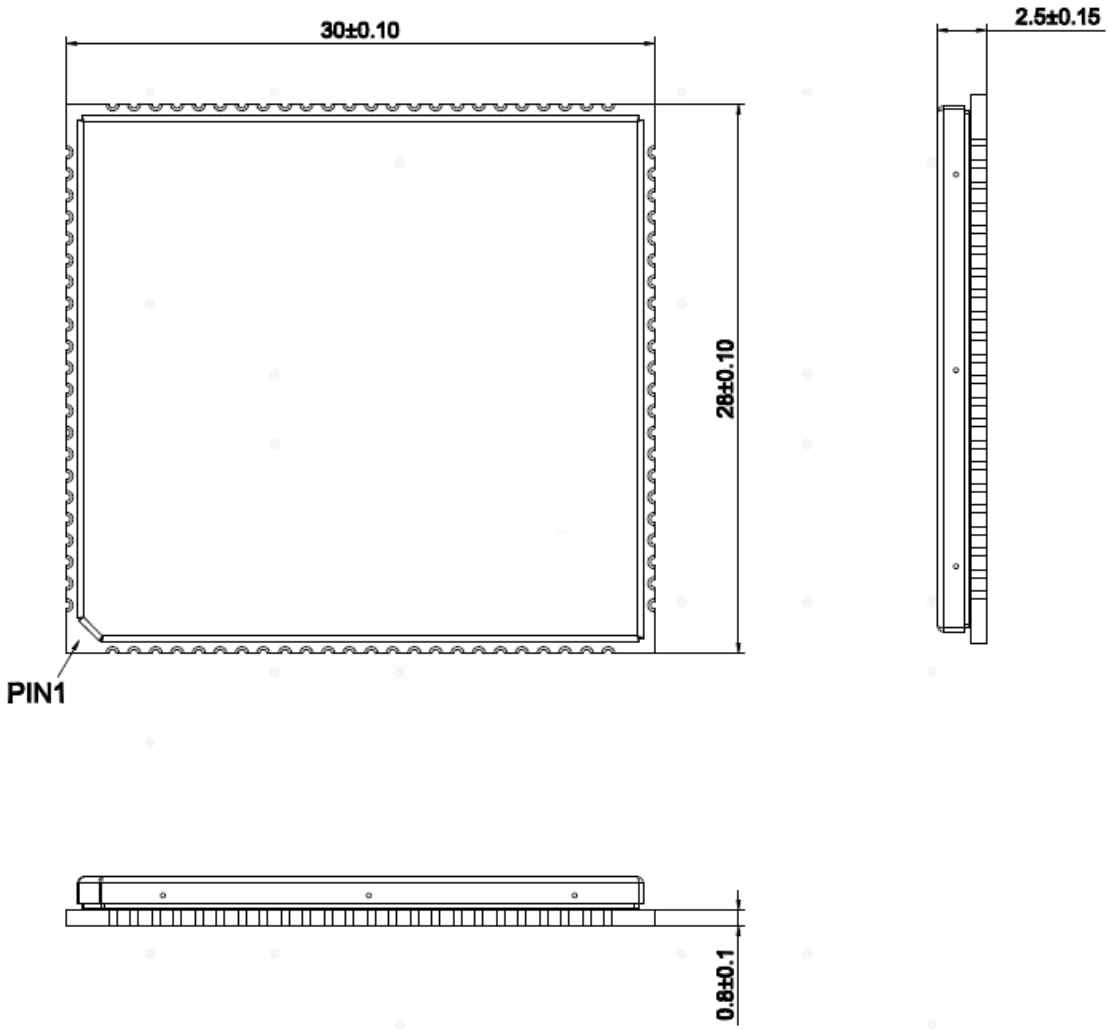
Operating frequency band	Transmitting rate	Transmitting power	Receiving sensitivity
802.11b (2.4G)	1/2/5.5/11 Mbps	N/A	-88 dBm
Bluetooth	DH5	3.2 dBm	-88 dBm
	2HD5	1 dBm	-88 dBm
	3DH5	1 dBm	-80 dBm
	BLE/1 Mbps	2 dBm	-94 dBm

8 Mechanical Characteristics

This chapter introduces mechanical characteristics of N58.

8.1 Dimensions

Figure 8-1 Top and side view dimensions (unit: mm)



8.2 Labeling

N58 module labels are laser-engraved and can withstand high temperatures of up to 260°C. There are two types of the N58 labels: the label with CMIIT ID is applicable to China, and the label without CMIIT ID is applicable to countries or regions outside China.

Figure 8-2 N58 labels

The above figure is for reference only. For authentic appearance, please refer to the module that you receive from Neoway.

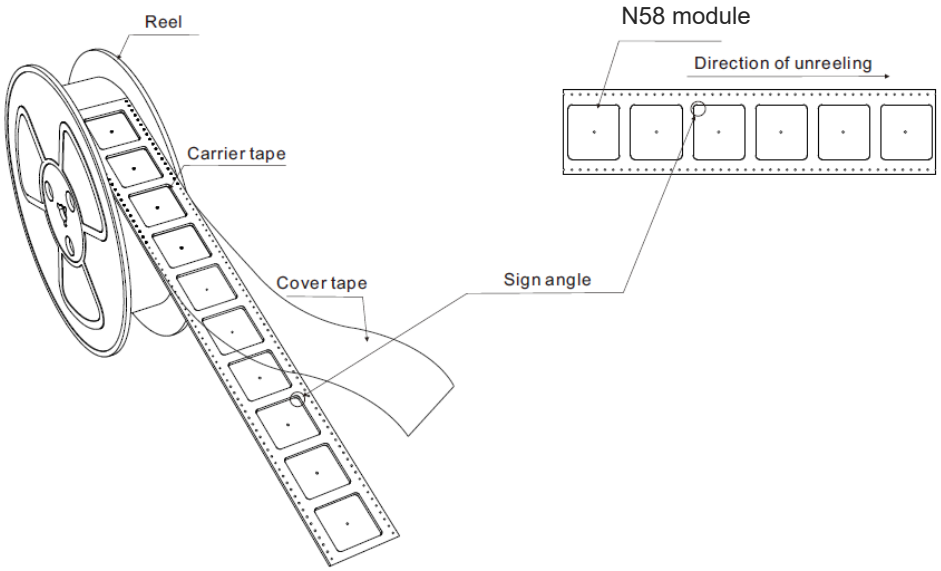
8.3 Packaging

N58 adopts SMD reflow soldering process for the electronics assembly. To prevent the modules from being damped, the modules are delivered as hermetically sealed reeled tapes for moisture-proof packaging and use the aluminum foil bag, desiccant, humidity indicator card, vacuum and other

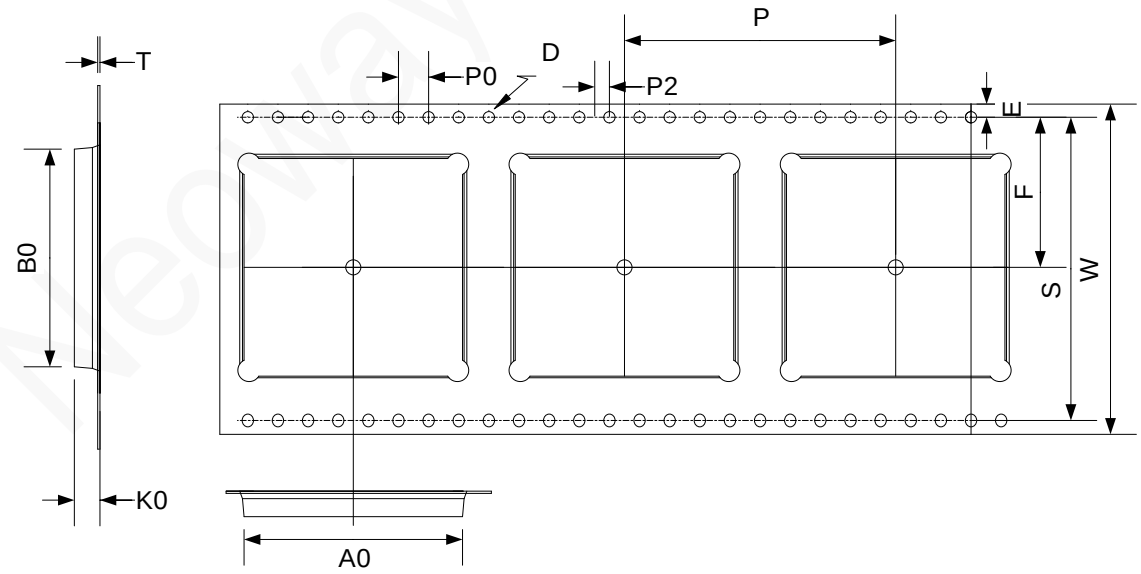
processing methods to ensure the dryness of the product and prolong its service life.

8.3.1 Reel

Neoway modules are delivered as reeled tapes as shown below:

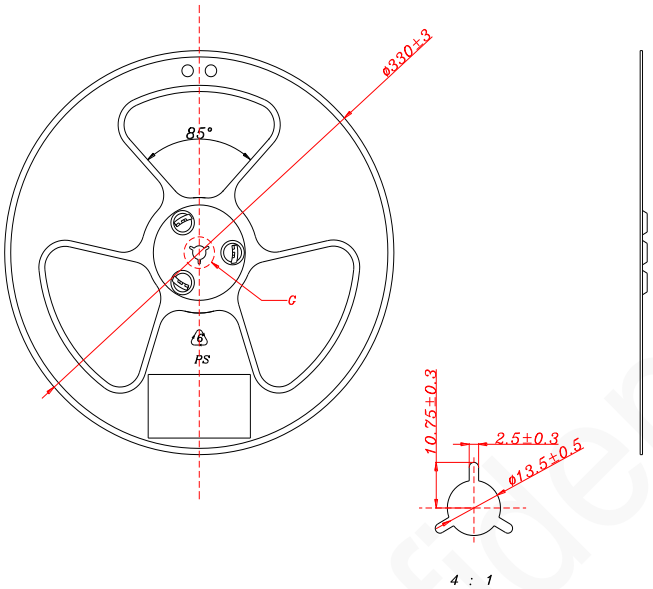


Tape Dimensions



ITEM	W	A0	B0	S	D	E	F	K0	P0	P2	P	T
DIM	44.0	28.7	28.70	40.4	1.5	1.75	20.2	3.55	4.0	2.0	36.0	0.30
TOLE	+0.3 -0.3	+0.1 -0.1	+0.1 -0.1	+0.1 -0.0	+0.1 -0.0	±0.1	±0.10	+0.1 -0.1	±0.1	±0.1	±0.1	±0.05

Reel Dimensions



8.3.2 Moisture Sensitivity Level

N58 series modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions. The MSL standard is available in IPC/JEDEC J-STD-020.

- Production environment condition: 30°C/60%

The module should be pre-baked under the following circumstances:

- The vacuum-sealed packaging is removed for more than 48 hours.
- The relative humidity is greater than 10% (you can see the humidity card that comes with the package).

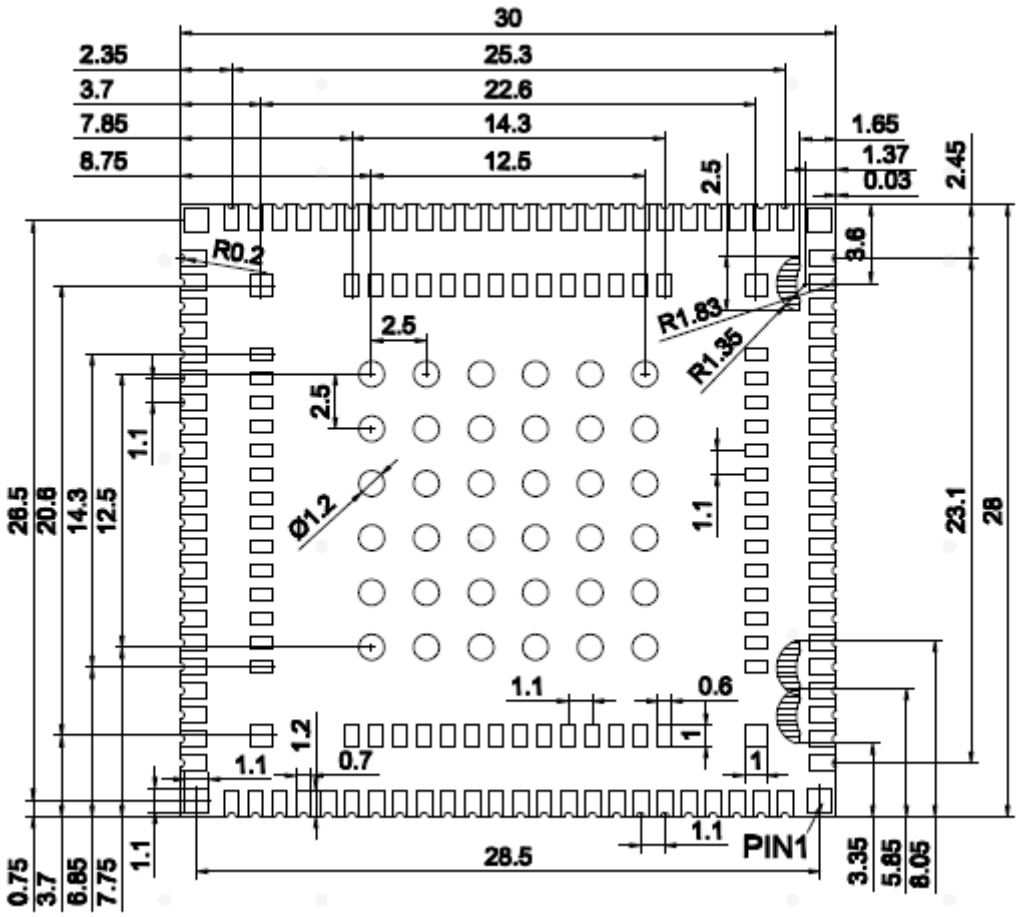
After the module is unpacked, if it is exposed to air for a long time, the module will get damped, and may be damaged during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at temperatures higher than 120 degrees for more than 12 hours. Do not bake Neoway modules while contained in a tape and rolled up in reels. For baking, place modules individually onto the oven tray.

9 Mounting N58 onto Application Board

This chapter describes the package of N58, the recommended footprint of the application PCB, and SMT specifications.

9.1 N58 PCB Package

Figure 9-1 Bottom view of N58 PCB package (unit: mm)

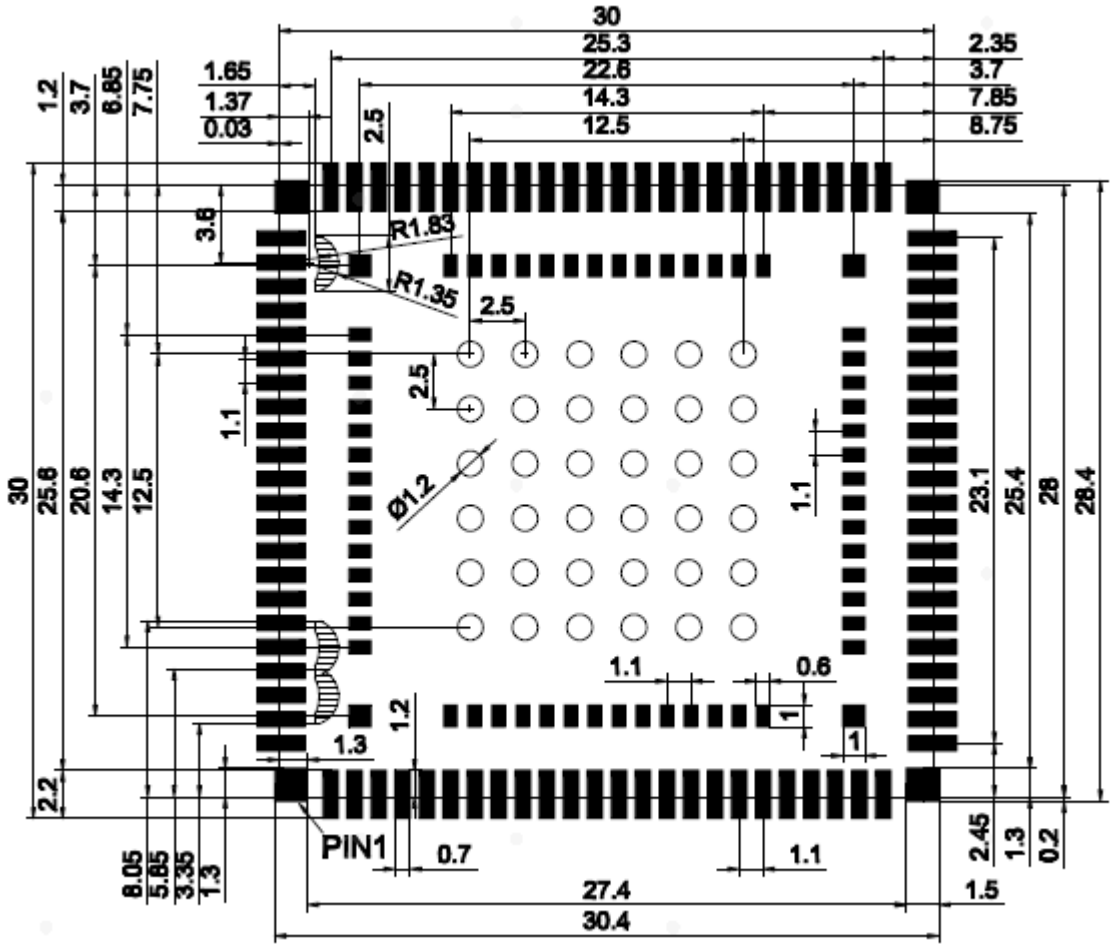


9.2 Application PCB Package

N58 is equipped with 192 pads which are introduced in 100-pin LCC + 92-pin LGA package.

- Only GND via-holes and copper pouring are allowed in the shaded area "" of the PCB package to ensure the proper operation of the module.
- To achieve higher yield during module production, it is recommended that the distance between other components on the PCB board and the module pads be at least 3 mm to avoid the risk of tin connection when using stepped stencil.

Figure 9-2 Recommended footprint of the N58 application PCB (unit: mm)



9.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm, which can be fine-tuned according to the actual situation.

9.4 Solder Paste

The thickness of solder paste and the flatness of PCB are essential for the production yield.

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

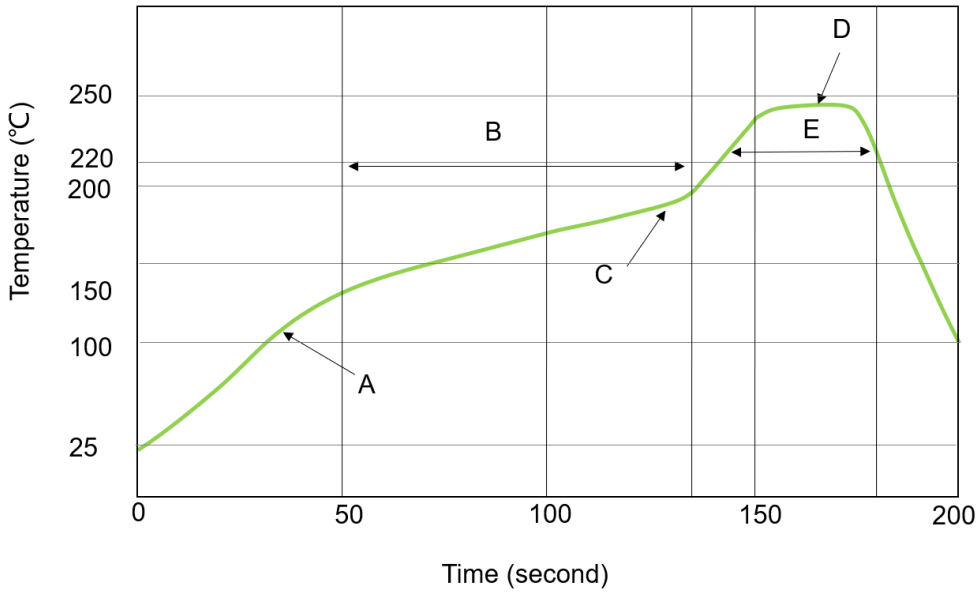
- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process is also lower than that of the lead-free solder paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LCC/LGA in the module is in a semi-melted state during the secondary reflow.
- When using only solder pastes with lead, please ensure that the time above 220°C (reflow temperature) exceeds 45 seconds and the peak temperature does not exceed 240°C.

9.5 Oven Temperature Profile

Neoway will not provide warranties for temperature-sensitive element abnormalities caused by improper temperature control.

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 9-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4°C/sec
- Ramp down rate: -3 to -1°C/sec
- Soaking zone: 150 - 180°C, Time: 60 - 100s
- Reflow zone: >220°C, Time: 40 - 90s
- Peak temperature: 235 – 245℃

For information about cautions in storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When removing the module manually from your application PCB board is required, use heat guns with great opening, adjust the temperature to about 245°C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module at high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

A Abbreviations

Abbreviation	Full name
ADC	Analog-to-Digital Converter
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
ARM	Advanced RISC Machine
BT	Bluetooth
bps	Bits per Second
CCC	China Compulsory Certification
CEP	Circular Error Probable
CNR	Carrier to Noise Rate
CS	Chip Select
CTS	Clear to Send
DC	Direct Current
DCS	Digital Cellular System
DI	Digital Input
DIO	Digital Input/Output
DL	Downlink
DO	Digital Output
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DRX	Discontinuous Reception
DTR	Data Terminal Ready
ECM	Ethernet Control Model
eDRX	Extended DRX
EGSM	Enhanced GSM
ESD	Electronic Static Discharge
ESR	Equivalent Series Resistance

EVK	Evaluation Kit
FDD	Frequency Division Duplexing
FPC	Flexible Printed Circuit
FTP	File Transfer Protocol
GFSK	Gauss Frequency Shift Keying
GLONASS	GLOBAL NAVIGATION SATELLITE SYSTEM
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
3GPP	3rd Generation Partnership Project
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
IO	Input/Output
ISP	Image Signal Processor
LCC	Leadless Chip Carriers
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCLK	Main Clock
MCU	Microcontroller Unit
MIC	Microphone
PCB	Printed Circuit Board
PCS	Personal Communications Service
PWM	Pulse Width Modulation
QVGA	Quarter Video Graphics Array
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output

SPK	Speaker
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver-Transmitter
UL	Uplink
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Battery Voltage
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless Fidelity
WCDMA	Wide-band Code Division Multiple Access
WCI	Wireless Coexistence Interface
WLAN	Wireless Local Area Network

