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N21

Hardware User Guide

Issue 1.8 Date 2022-04-20

Notice

This document provides guide for users to use N21.

This document is intended for system engineers (SEs), development engineers, and test engineers.

THIS GUIDE PROVIDES INSTRUCTIONS FOR CUSTOMERS TO DESIGN THEIR APPLICATIONS. PLEASE FOLLOW THE RULES AND PARAMETERS IN THIS GUIDE TO DESIGN AND COMMISSION. NEOWAY WILL NOT TAKE ANY RESPONSIBILITY OF BODILY HURT OR ASSET LOSS CAUSED BY IMPROPER OPERATIONS.

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About This Document

Scope

This document is applicable to N21 series.

It defines the features, indicators, reference designs, and test standards of the N21 module.

Reference designs in this document are only for reference. Design applications based on the actual scenarios and conditions. Please contact Neoway technical support team for further technical support.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Changes	Revised By
1.0	2018-06	Initial release.	Huang Jianlong
1.1	2018-08	• Updated operating voltage range. • Updated temperature ranges. • Updated bands supported. • Updated pin description.	Huang Jianlong
1.2	2018-10	• Deleted AP and changed bands of EU version to B3, B5, B8, B20, B28. • Modified reference designs of UART and changed level from module side to VDDIO_2P8. • Added reference design of WAKEUP and power domain. • Updated reference design of RESET and power domain. • Added cautions about initialization. • Updated current data.	Huang Jianlong
1.3	2018-12	Divided VBAT into VBAT_BB and VBAT_RF.	Huang Jianlong
1.4	2019-03	• Updated startup timing, shutdown timing, and reset timing. • Added the caution of supply voltage.	Huang Jianlong

1.5	2019-11	• Added BLE antenna. • Added the operating current, frequency band and baud rate of BLE.	Huang Jianlong
1.6	2020-01	• Updated the schematic diagram of reset reference design. • Updated remarks of UART_RX 13 pin.	Zhao Rongzhou
1.7	2020-06	• Updated the wireless rate. • Updated the dimensional tolerance.	Huang Jianlong
1.8	2021-09	• Deleted the design of the low-voltage power supply solution. • Updated the input voltage range of the module.	Rongzhou.zhao

Conventions

Symbol	Description
	Indicates danger or warning. This information must be followed. Otherwise, a catastrophic module or user device failure or bodily injury may occur.
	Indicates caution. This symbol alerts the user to important points about using the module. If these points are not followed, the module or user device may fail.
	Indicates instructions or tips. This symbol provides advices or suggestions that may be useful when using the module.

Related Documents

Neoway_N21_Datasheet

Neoway_N21_Product_Specifications

Neoway_N21_AT_Command_Mannual

Neoway_N21_EVK_User_Guide

1 Safety Recommendations

Ensure that this product is used in compliance with the requirements of the country and environment. Read the following safety recommendations to avoid bodily injuries or damages of the product or workplace:

- Do not use this product at any places with a risk of fire or explosion.

  If this product is used in a place with flammable gas or dust, such as propane gas, gasoline, and flammable spray, it will cause an explosion or a fire.

- Disable the wireless communication function in places where wireless communication is prohibited.

  Do not use this product that can interfere with other electronic devices in environments, such as hospitals and airplanes.

Follow the requirements below during the application design and use of this product:

- Do not disassemble this product without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Design your application correctly based on the hardware user guide. Connect this product to a stable power supply and route traces following fire safety standards.
- Avoid touching the pins of this product to prevent damages caused by ESD.
- Do not insert or remove a SIM card when it is not powered off.

2 About N21

N21 is an compact industrial-grade NB-IoT module that supports Cat NB1.

2.1 Product Overview

N21 series include multiple variants. Table 2-1 Lists the variants and bands supported.

Table 2-1 Variants and bands

Function	Variant	Network Type	Band
N21	N21-CN-011AS1	Cat NB1	HD-FDD: B3, B5, B8
	N21-EU-011AS1	Cat NB1	HD-FDD: B3, B5, B8, B20, B28

Featured with ultra-low power consumption, extensive coverage and simple peripheral circuits, N21 is well applicable for IoT applications that requires low data rate and low power consumption. It adopts 22-pin LGA package and its dimensions are 18 mm x 13.8 mm x 2.5 mm, which can meet the comact product design requirement .

It provides the following hardware resources and functionalities:

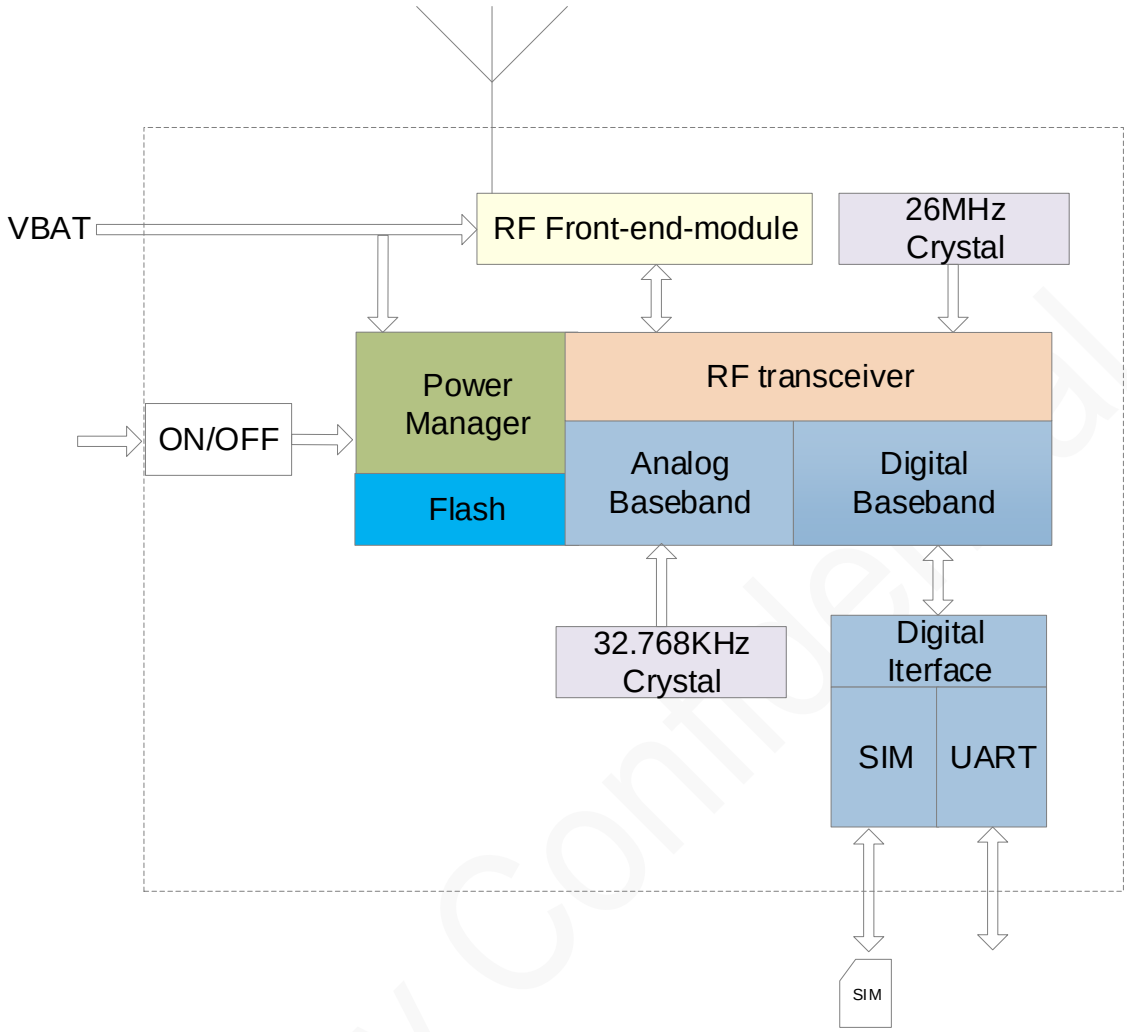
- UART interface, used for data communication, firmware update, and commissioning
- Compatibility with 1.8 V/3.0V USIM card
- STATUS (working status) indicator/NET_LIGHT (network status indicator)/WAKEUP (PSM wakeup)/RESET

2.2 Block Diagram

N21 consists of the following functionality modules:

- Power management unit
- Clock unit
- Digital interfaces (UIM, UART)
- RF section

Figure 2-1 Block diagram



2.3 Basic Features

Parameter	Description
Physical features	• Dimensions: (18.0±0.10) mm × (13.8±0.10) mm × (2.5±0.10) mm • Package: 22-Pin LGA • Weight: around 1.3 g
Temperature ranges	Operating: -30°C to +75°C Extended: -40°C to +85°C Storage: -45°C to +90°C
Operating voltage	VBAT: 3.3 V to 4.3 V, typical value: 3.8 V
MIPS processor	Main frequency: 192 MHz, 16KB L2 cache
Memory	RAM: 32 Mb

	ROM: 32 Mb
Band	B3, B5, B8, B20, B28
Wireless rate	LTE Cat NB1: 26 Kbps (DL)/62.5 Kbps (UL) LTE Cat NB2: 126.8 Kbps (DL)/158.5 Kbps (UL)
Transmit power	LTE: +23 dBm+/-2 dBm (Power Class 3)
Application interfaces	• 4G antenna interface, 50 Ω characteristic impedance • BLE antenna interface
	1 UART interface, used to send AT commands
	1 USIM interface, compatible with 1.8V/3V USIM card
	2*2 mm embedded eSIM (optional)
AT commands	3GPP Rel-13/Rel-14 Neoway extended commands
Protocol	TCP, UDP, HTTP, HTTPS, FTP, MQTT, COAP, LWM2M*
Certification approval	CCC, SRRC, CTA, RoHS, CE, NCC*, TIM* China Mobile/China Unicom/China Telecom Ali cloud*

* indicates in development.

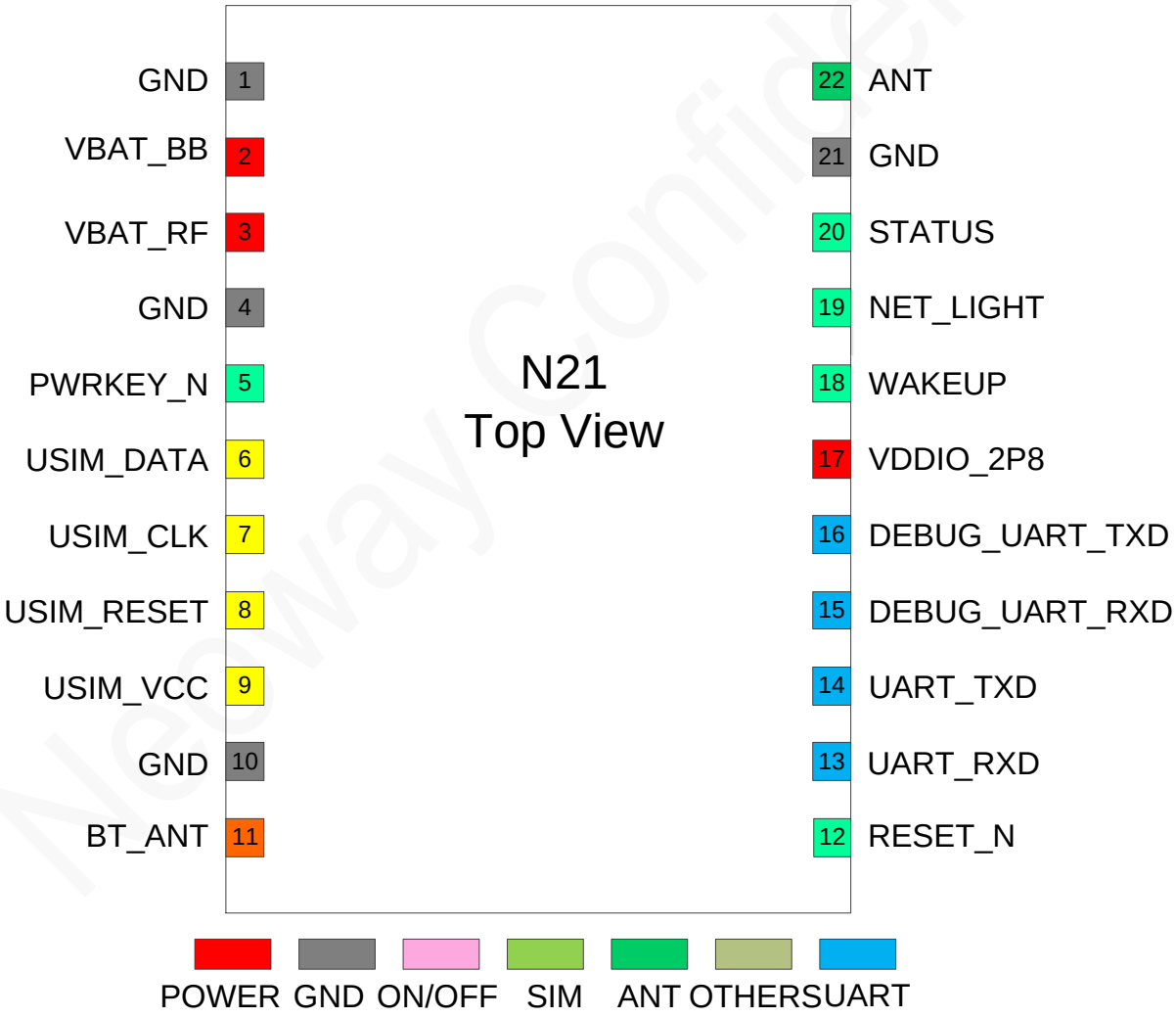
3 Module Pins

There are 22 pins on N21 and their pads are introduced in LGA package.

3.1 Pad Layout

Figure 3-1 shows the pad layout of N21.

Figure 3-1 Pin definition of N21



3.2 Pin Description

Table 3-1 lists the definition of IO types.

Table 3-1 IO definition

IO Type			
DO	Digital output, COMS logic level		
DI	Digital input, COMS logic level		
PO	Power output		
PI	Power input		
AO	Analog output		
AI	Analog input		
Level Feature			
P1	1.8V/3.0V	1.8 V level feature: V_{IH}=1.26V~1.8V V_{IL}=-0.3V~0.36V V_{OH}=1.44V~1.8V V_{OL}=0V~0.4V	3.0 V level feature: V_{IH}=2V~3V V_{IL}=-0.3V~0.57V V_{OH}=2.28V~3V V_{OL}=0V~0.4V
P2	2.8V digital IO	V_{IH}=2.1V~2.8V V_{OH}=2.1V~2.8V	V_{IL}= 0V~0.7V V_{OL}=0V~0.7V
P3	1.1V of V_RTC power domain	$V_{IH\ min}$=0.83V $V_{IL\ min}$=-0.3V	$V_{IH\ max}$= 1.41V $V_{IL\ max}$= 0.36V

Table 3-2 Pin description

Signal	**Pin**	**I/O**	**Function**	**Level**	**Remarks**
Power Supply Pins					
VBAT_X	2, 3	PI	Main power input	V_{max}=4.3V	Connect the 2nd pin and the 3rd pin together when using a power source that supplies normal voltage.
VDDIO_2P8	17	PO	2.8V power output	V_{norm}=2.8V I_{max}=50mA	Used only for level shifting. Leave this pin floating if it is not used.

GND	1, 4, 10, 21				Ensure that all GND pins are connected to the ground.
Control Interfaces					
RESET_N	12	DI	Reset input	P3	Triggered by low level.
PWRKEY_N	5	DI	ON/OFF button	P3	Triggered by low level to start or shut down the module.
WAKEUP	18	DI	PSM wakeup input	P3	Input high level for 1 second at this pin and the module wakes up.
STATUS	20	DO	Status indicator	P2	Leave this pin floating if it is not used.
NET_LIGHT	19	DO	Network status indicator	P2	Used with AT commands.
UART Interface					
UART_TXD	14	DO	Data transmitting	P2	Used for data transmission. Leave these pins floating if not used.
UART_RXD	13	DI	Data receiving	P2	
DEBUG_UART Interface					
DEBUG_UART_RXD	15	DI	Data receiving	P2	Used for commissioning. Leave these pins floating if not used.
DEBUG_UART_TXD	16	DO	Data transmitting	P2	
USIM Interface					
USIM_VCC	9	PO	USIM power output	IO_{max} =50mA	USIM_VCC.
USIM_DATA	6	DIO	USIM data IO	P1	
USIM_CLK	7	DO	USIM clock	P1	
USIM_RESET	8	DO	USIM reset	P1	
Antenna Interface					
ANT	22	AI/O	Antenna		50 Ω impedance for traces.
BT	11	BT_ANT	Antenna		

4 Application Interfaces

N21 provides power supply, communications, RF, and other interfaces to meet customers requirements in different application scenarios.

This chapter describes how to design each interface and provides reference designs and guidelines.

4.1 Power Supply

The schematic design and PCB layout of the power supply part are the most critical process in application design and they determine the performance of customers application. Please read the guidelines to design power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin	I/O	Function	Remarks
VBAT_BB	2	PI	Power input of baseband	3.3 V to 4.3 V DC (typical value: 3.8 V DC).
VBAT_RF	3	PI	Power input of RF	3.3 V to 4.3 V DC (typical value: 3.8 V DC).
VDDIO_2P8	17	PO	2.8V power output	Output max. 50 mA, used only for level shifting. Add ESD protector when using this pin.
GND	1, 4, 10, 21			Connect all GND pins to the ground plane.

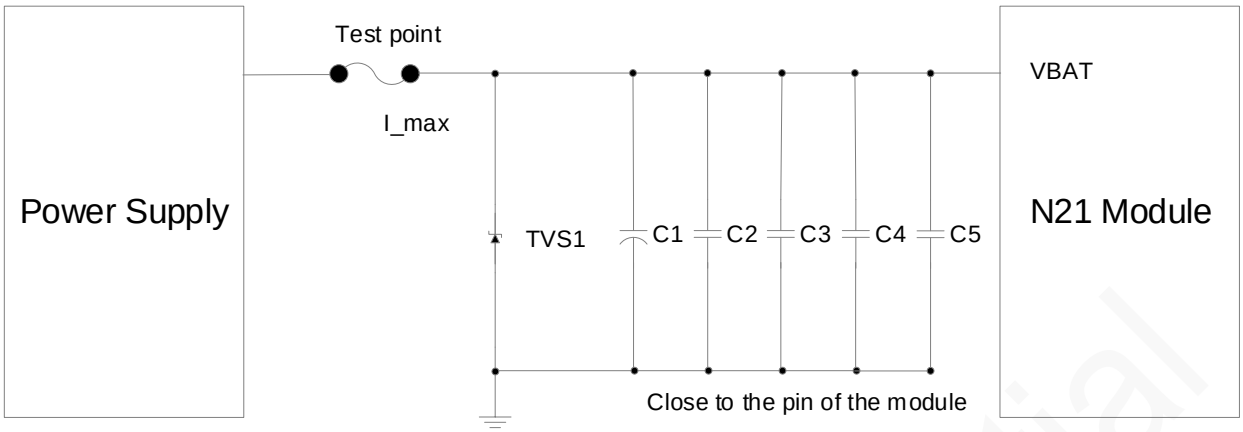
4.1.1 VBAT

The power supply design consists of two parts: schematic design and PCB layout.

Schematic Design

N21 adopts a 3.3 V to 4.3 V voltage input that is supplied by a battery and the typical voltage is 3.8 V. Figure 4-1 shows the schematic design of N21 power supply.

Figure 4-1 Recommended circuit design 1

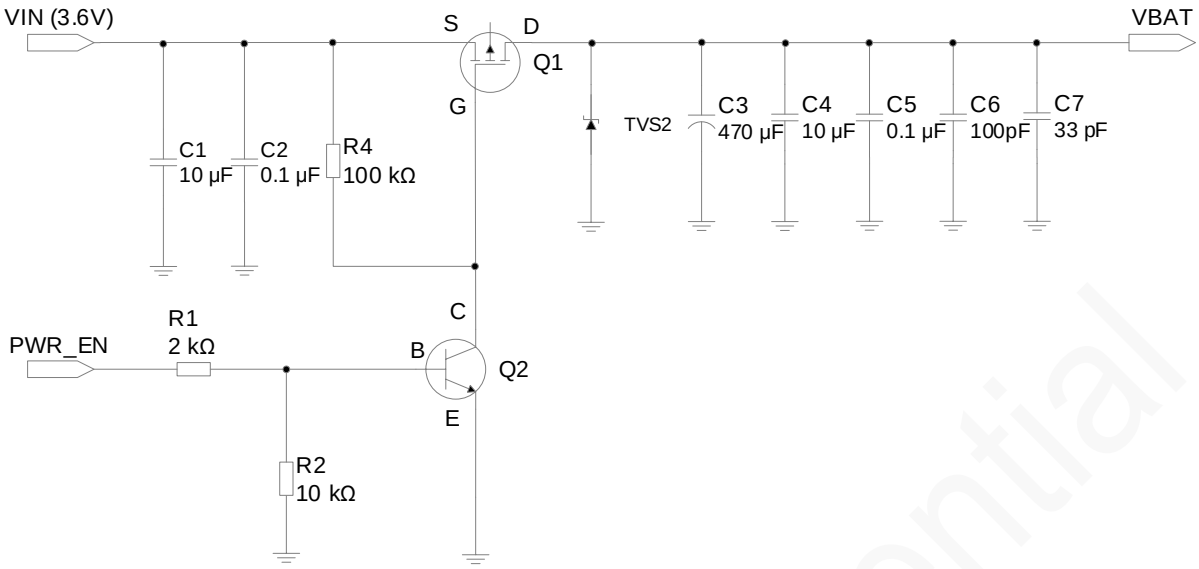


- The maximum input voltage is 4.3 V and the typical value is 3.8 V.
- The protection voltage across TVS1 should not exceed the maximum input voltage at which the module can operate.

  To protect back-end components and the module, place the TVS diode close to the input interface of the power supply to clamp the surge voltage before the voltage enters back-end circuits.
- Select a large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be higher than 1.5 times the voltage across the power supply.
- Place a bypass capacitor of low-ESR close to the module to filter out high-frequency noise from the power supply.

A controllable power supply is preferable if the module is used in harsh conditions. Figure 4-2 shows the recommended schematic design.

Figure 4-2 Recommended schematic design 2



Schematic Design Guidelines

- Select an enhanced p-MOSFET at Q1, of which the maximum safe operating voltage and drain current is high and Rds is low.
- Select a common NPN bipolar transistor or a digital NPN bipolar transistor at Q2. Reserve enough tolerances of resistors at R1 and R2 in design, especially for the situation in which operating voltage of the bipolar transistor might increase in low temperature.
- Place TVS2 close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Place C3 close to the module. A large bypass tantalum capacitor (220 µF or 100 µF) or aluminum capacitor (470 µF or 1000 µF) is expected at C1 to reduce voltage drops during bursts. Its maximum safe operating voltage should be higher than 1.5 times the voltage across the power supply.
- Place a low-ESR bypass capacitor close to the module to filter out high-frequency noise from the power supply.

PCB Layout Guidelines

Place an ESR capacitor at the output of the power supply to absorb surge current. Place a TVS diode at the input of VBAT to protect back-end components. The layout of components and PCB trace are critical to the hardware design of a device. Follow rules below in the power supply design:

- TVS diodes dissipate the transient pulse power during a surge and can handle a peak pulse current of dozens or more than 100 A. They have a short response time. Place the TVS as close to the interface as possible to ensure that the surge voltage can be clamped before the pulse is coupled to the neighbor traces.

- Place bypass capacitors close to the power pin of the module to filter out the high-frequency noise from the power supply.
- Ensure that the width of PCB traces for VBAT circuits allows 1 A current and ensure no obvious decrease of loop voltages. Trace width of VBAT should be at least 1 mm and the ground plane should be as complete as possible. The traces of power supply circuit should be as short and wide as possible.
- Noise-sensitive circuits such as audio and RF, should be placed far away from power supply circuits, especially when the DC-DC is adopted in the design. Connect GND pins and bottom pads to ground to optimize heat sink and separate noise.

Never use a diode to make the drop voltage between a higher input and module power. Otherwise, Neoway will not provide warranty for product issues caused by this. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, because the forward voltage of diode will vary greatly in different temperature and current. The module might not work properly with a diode power supply.

4.1.2 VDDIO_2P8

N21 provides one VDDIO_2P8 pin that outputs 2.8 V@50 mA.

VDDIO_2P8 is enabled automatically when the module is awake or in running state.

It is recommended that VDDIO_2P8 is used for level shift only and an ESD protector should be added.

4.2 Control Interfaces

Signal	Pin	I/O	Function	Remarks
RESET_N	12	DI	Reset input	Reset at low level.
PWRKEY_N	5	DI	ON/OFF button	Triggered by low level to start or shut down the module.

4.2.1 PWRKEY_N

N21 allows startup by the following controls:

- Button
- MCU
- Automatic start once powered up

Figure 4-3 Reference design of startup controlled by button

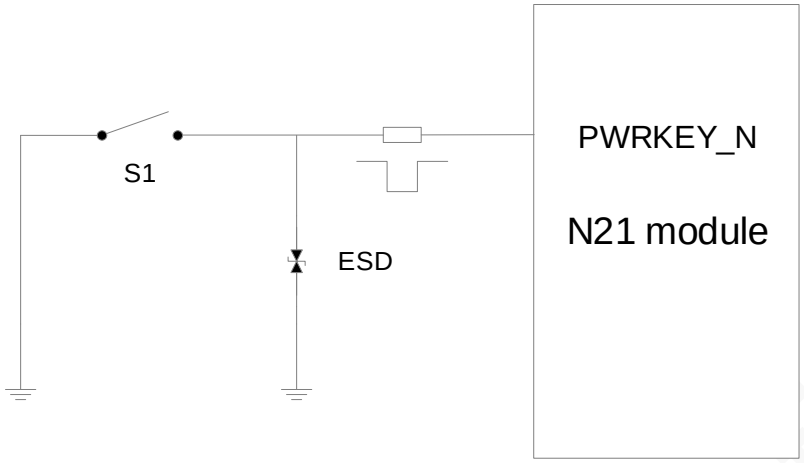


Figure 4-4 Reference design of startup controlled by MCU

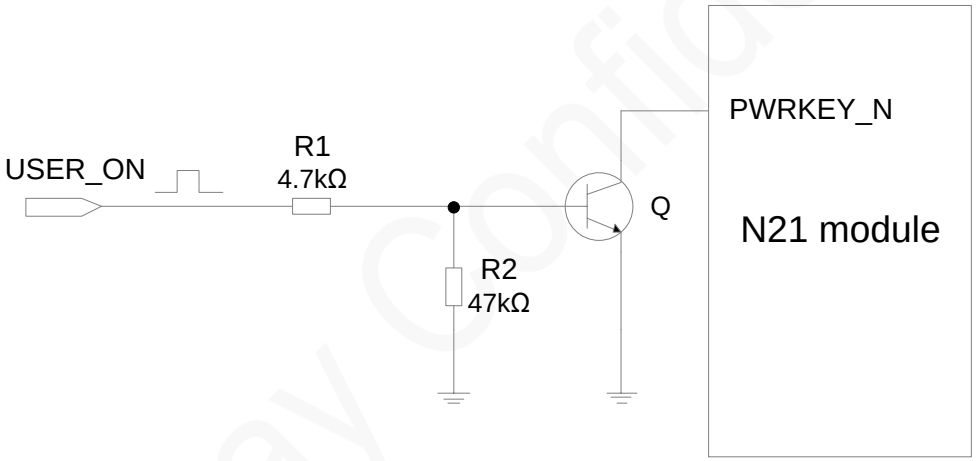
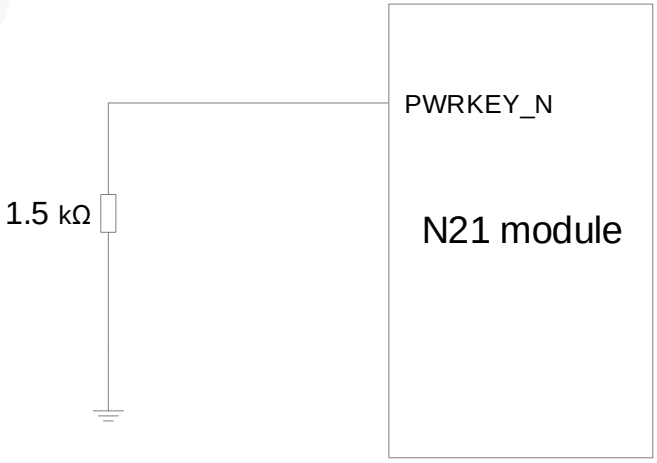


Figure 4-5 Reference design of automatic start once powered up



Startup Process

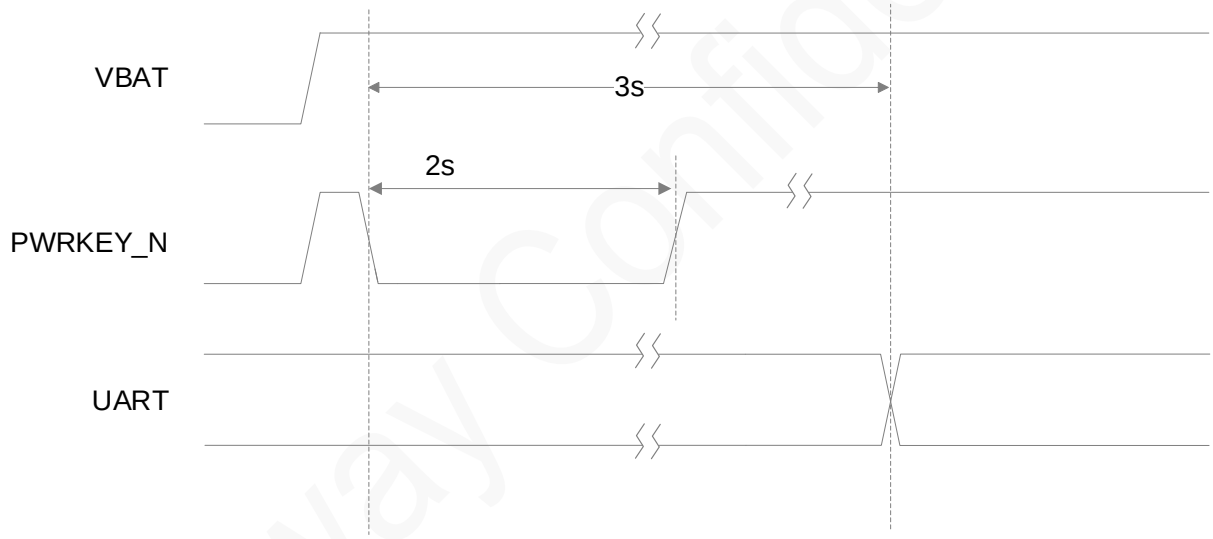
After powering up the VBAT pin, input low level for 2 seconds at PWRKEY_N to start the module. Pull PWRKEY_N high after the module is started. The STATUS indicator turns on, indicating that the module completes initialization. The baud rate of N21 is flexible since the module embeds automatic baud rate detection. Before sending data through UART port, issue AT so that the UART port can automatically detects the baud rate and outputs **+PBREADY**, indicating that the UART is ready.

In program design, use **+PBREADY** to check whether the module is reset due to any fault.

To use the function of automatic startup once powered up, refer to Figure 4-5. Note that this startup design does not support shutdown.

Prior to turning on the module, power on the host MCU and complete the UART initialization. Otherwise conflicts may occur during initialization due to unstable conditions.

Figure 4-6 Startup timing



No power failure is allowed during initialization. Otherwise, the hardware might encounter faults or be damaged.

If the power button is held for less than 2 seconds (1.2 second to 2 seconds), the voltage at PWRKEY pin might slightly increase by a step of 0.3V for short time.

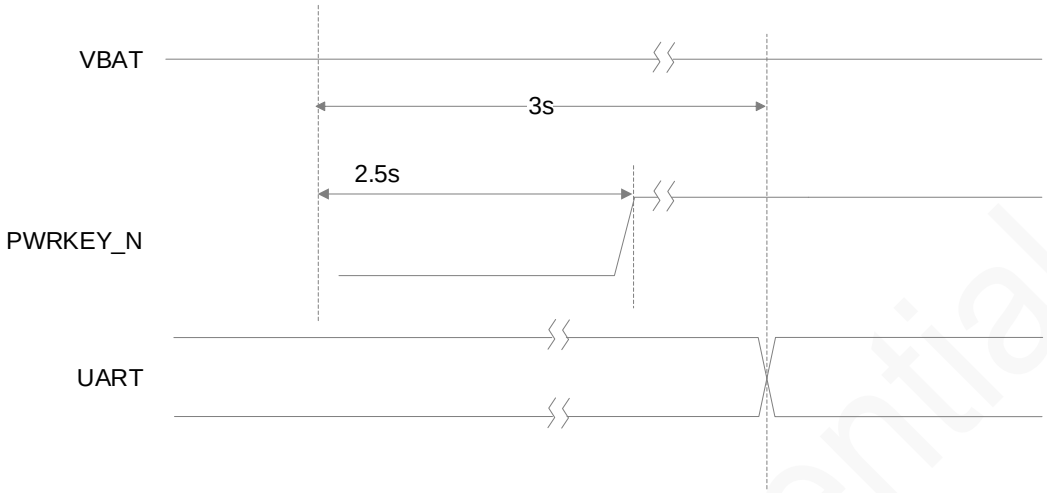
Shutdown Process

The module can be powered off through hardware and software.

PWRKEY_N is used to hardware shut down the module. When the module is working, inputting negative pulses for more than 2.5 seconds to PWRKEY_N can trigger the shutdown process of the module. The module is shut down after around 3 seconds, and then turns off the power supply.

Figure 4-7 shows the hardware shutdown timing.

Figure 4-7 Shutdown timing



For how to power off through software, see *Neoway_N21_AT_Command_Manual*.

4.2.2 RESET_N

RESET_N is used to reset the module. When the module is working, inputting negative pulse for more than 1 second to RESET_N can trigger the reset process of the module.

If 2.8V/3.0V/3.3V IO system is used then add a triode to separate it. Refer to the following designs.

Figure 4-8 Reset controlled by button

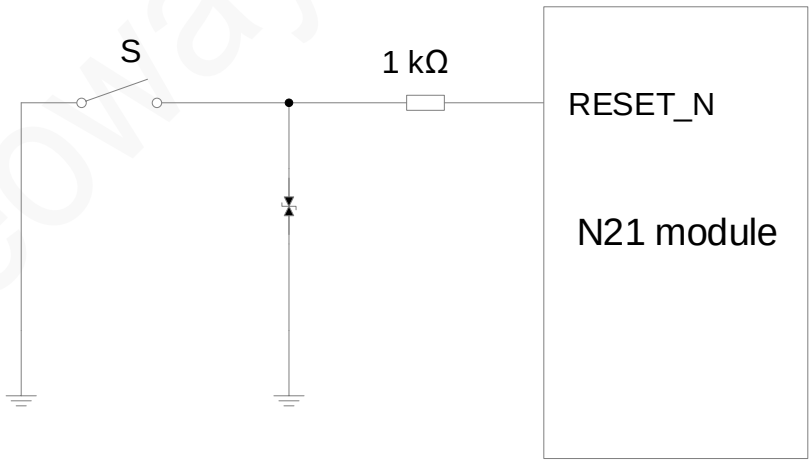
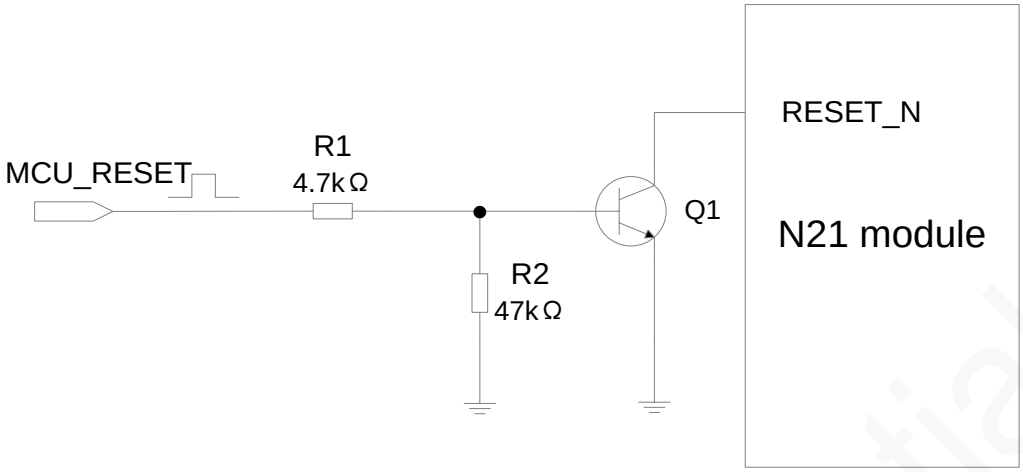


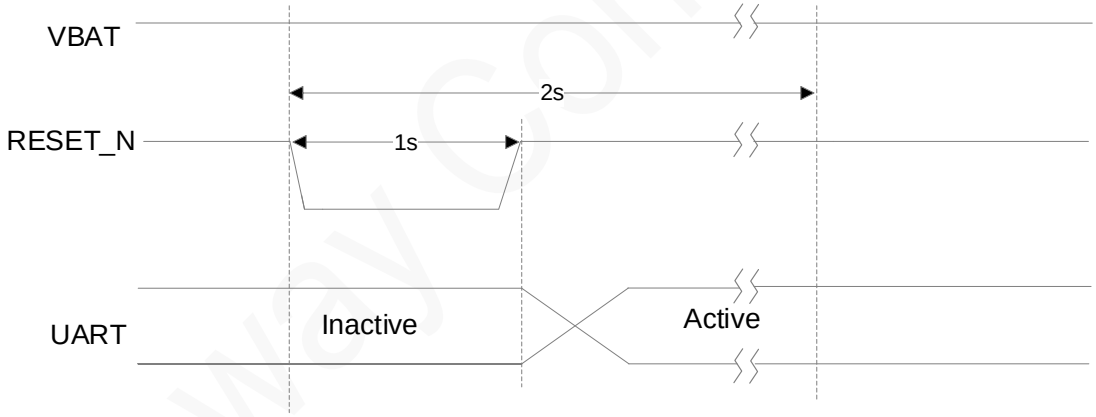
Figure 4-9 Reset circuit with triode separating



To reset the module through high level (MCU-RESET), refer to Figure 4-9.

Figure 4-10 shows the reset timing of N21.

Figure 4-10 Reset timing of N21



4.3 Peripheral Interfaces

N21 provides various peripheral interfaces.

In all reference designs of this section, the signals of pins on the module is named in perspective of module while peripheral pins are named from the view of the components. For example, UART_TXD indicates the pin that the module sends data while MCU_RXD indicates the pin that MCU receives data. These two pins should be connected.

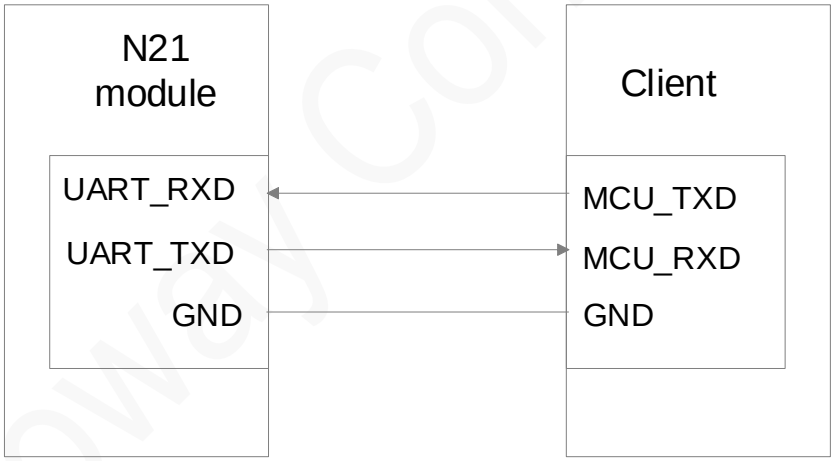
Please note the signal naming of pins on the components in peripheral selection and design.

4.3.1 UART

Signal	Pin	I/O	Function	Remarks
UART_TXD	14	DO	Data transmitting	-
UART_RXD	13	DI	Data receiving	Connect UART_RX to VDDIO_2P8 through a pull-up resistor. Otherwise, the startup and the PSM wakeup function might fail.

N21 provides one UART interface that supports automatic baud rate detection. The level at the UART interface is 2.8V.

Figure 4-11 UART connection



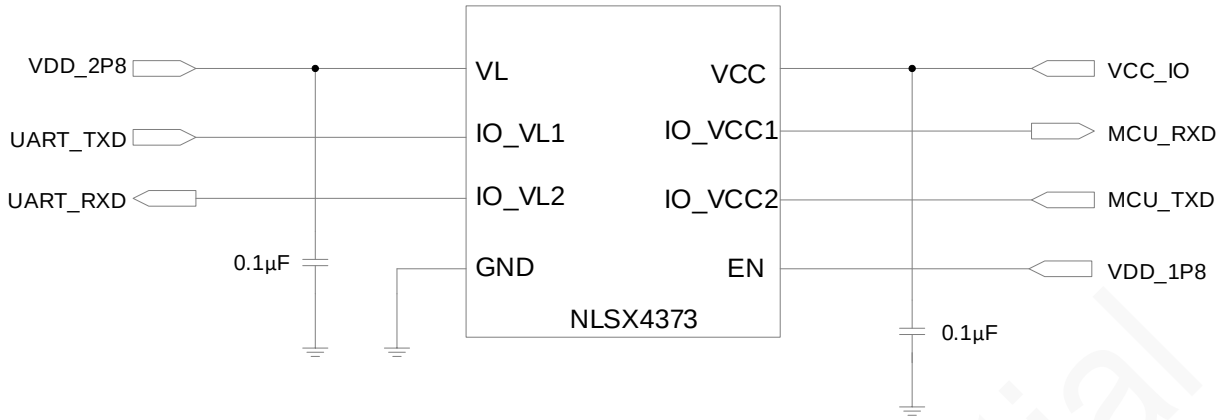
Schematic Design Guidelines

- Note the match of signals.
- If the UART does not match the logic voltage of the MCU, add an external level shifting circuit.

Three types of level shifting circuit are recommended based on the logic level quality. The first one is preferred and the other two are cost-effective simple circuits. Note their application senarios.

Level shift chip is recommended if the level of MCU is higher than 3.3V or the baudrate is higher than 1 MHz. Figure 4-12 shows the reference design.

Figure 4-12 Recommended level shifting circuit 1

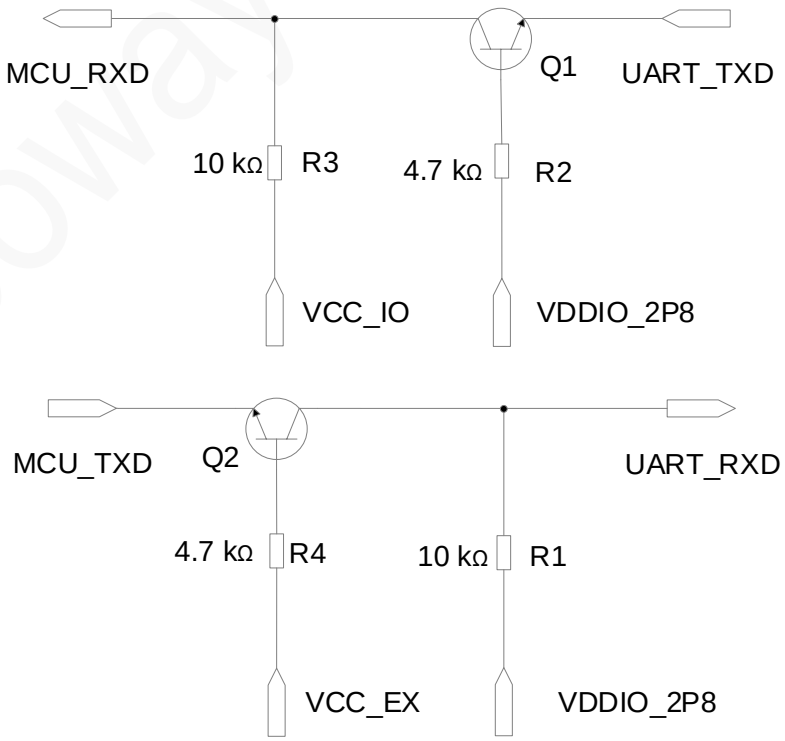


- NLSX4373 is a dual-supply level shifter, the rate of which is up to 20 Mb/s.
- VL is the reference voltage of IO_VL1 and IO_VL2, ranging from 1.5V to 5.5V.
- VCC is the reference voltage of IO_VCC1 and IO_VCC2, ranging from 1.5V to 5.5V.
- EN is the enable pin, which works at a voltage of greater than VL-0.2V.

In the above circuit, the EN pin is connected to VDD_1P8 and the level shifter is always working.

If the low level at MCU_UART (V_{IL}) is lower than 200 mV and baudrate is lower than 1 MHz, adopt recommended level shifting circuit 2.

Figure 4-13 Recommended level shifting circuit 2



In the above circuit, note VCC_EX:

- VCC_EX=VCC_IO when VIH≤2.8V
- VCC_EX=VDDIO_2P8 when VIH≥2.8V

Components:

- R2, R4: 2 kΩ to 10 kΩ

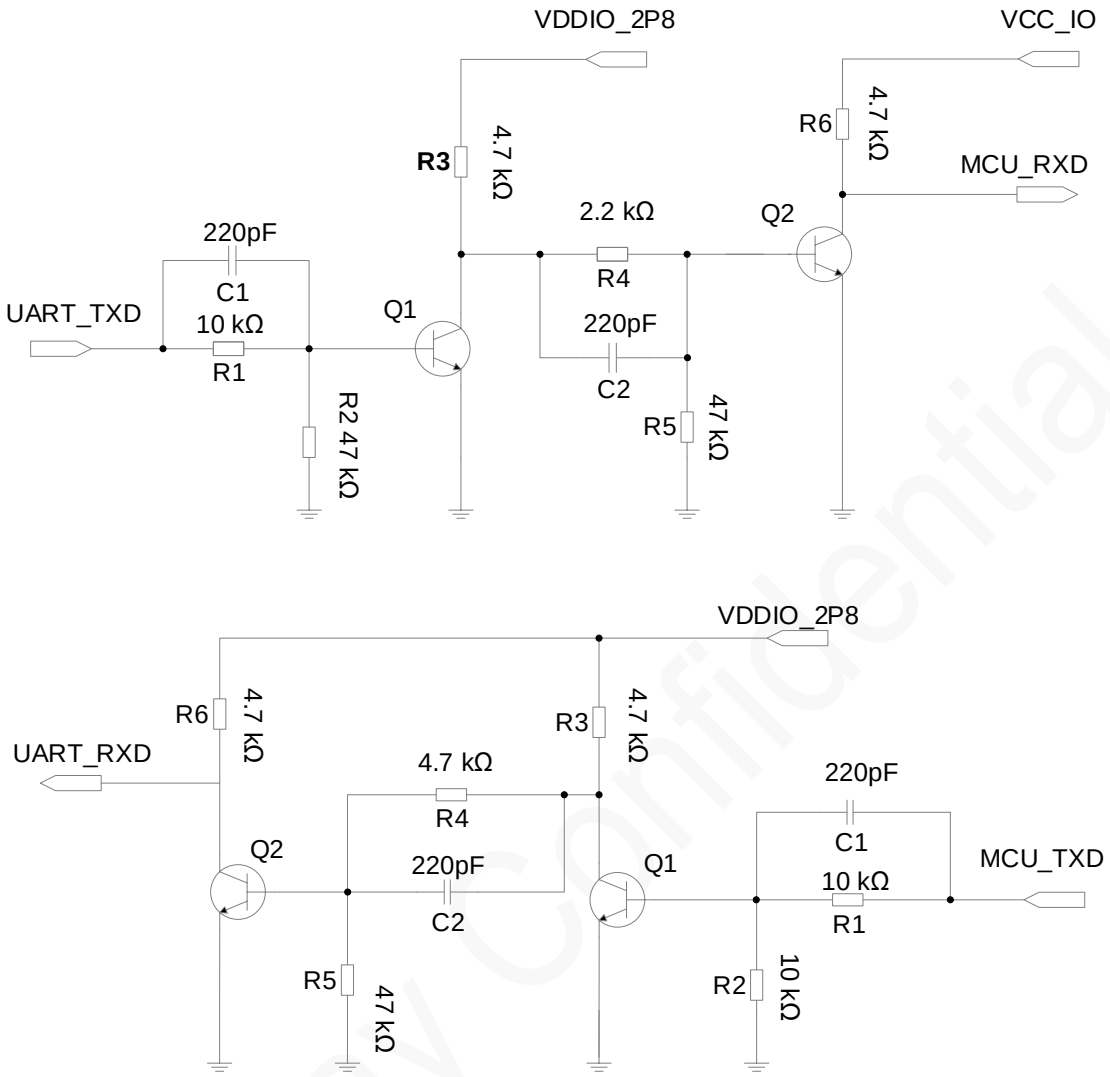
  The greater the UART baud rate is, the lower the R2 and R4 values are.
- R1, R3: 4.7 kΩ to 10 kΩ

  The greater the UART baud rate is, the lower the R1 and R3 values are.
- Q1, Q2: MMBT3904 or MMBT2222.

  High-speed transistor is better.

If the low level at MCU_UART (V_{IL}) is greater than 200mV and baudrate is lower than 1 MHz, adopt recommended level shifting circuit 3. Otherwise, low level at UART might be higher than required, resulting in failure to identify signals.

Figure 4-14 Recommended level shifting circuit 3



Q1, Q2: MMBT3904 or MMBT2222. High-speed transistor is better.

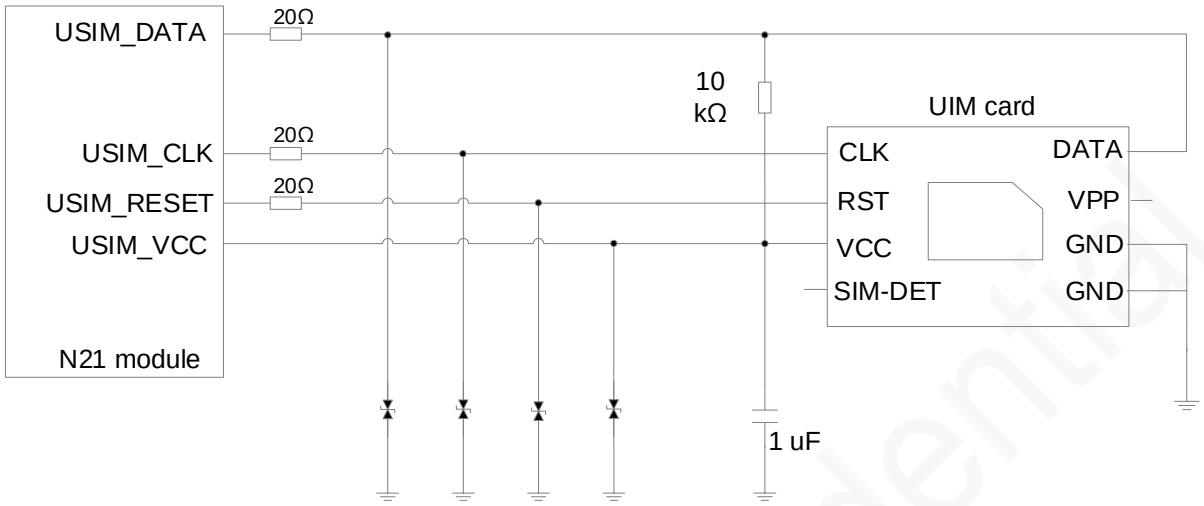
MCU_TXD and MCU_RXD are respectively the TX and RX of the MCU while UART_TXD and UART_RXD are respectively the TX and RX of the module. VCC_IO is the IO voltage of the MCU.

4.3.2 USIM

Signal	Pin	I/O	Function	Remarks
USIM_VCC	9	PO	USIM power	Compatible with 1.8 V/3 V USIM card.
USIM_DATA	6	DIO	USIM card data IO	A 10 kΩ resistor is required between USIM_VCC and USIM_DATA.
USIM_CLK	7	DO	USIM clock	-
USIM_RESET	8	DO	USIM reset	-

N21 provides one USIM card interface that is compatible with 1.8V/3V USIM cards. Figure 4-15 shows the reference design of the USIM card interface.

Figure 4-15 Reference design of USIM card interface



Schematic Design Guidelines

- USIM_VCC is the pin to supply power for SIM card and its maximum load is 30 mA. Do NOT use it for any other purpose.
- Reserve a position for pull-up resistor externally in design since the USIM_DATA pin is not pulled up internally.
- USIM_CLK is the clock signal pin, supporting a clock frequency of 3.25 MHz.
- Add ESD protectors, such as ESD diodes or TVS diodes (with a junction capacitance less than 33pF) on the USIM signal lines in applications with a high requirement of ESD protection.
- Connect a 20 Ω resistor respectively to USIM_DATA, USIM_RST, and USIM_CLK in series to enhance the ESD performance.

PCB Layout Guidelines

- USIM signals are likely to be jammed by RF radiation, resulting in failure to detect the USIM card. Place USIM far away from RF circuits.
- Place USIM card closed to the module and USIM traces should be as short as possible.
- Place ESD protection resistors and components close to USIM card.
- Connect the ground of USIM to main ground to enhance jamming capability.

4.4 RF Interface

Signal	Pin	I/O	Function	Remarks
ANT	22	AI/O	Antenna	50Ω impedance.
ANT_BT	11	AI/O	BT antenna	To use it, you need to design the function in software and prepare the hardware component in your BOM.

4.4.1 Antenna Design

ANT of N21 requires a characteristic impedance of 50 Ω. Control the impedance of the traces between the pins and antenna to ensure the RF performance. An impedance matching circuit, such as L network, T network, and pi network is mandatory in between. Pi network is recommended.

Figure 4-16 L network

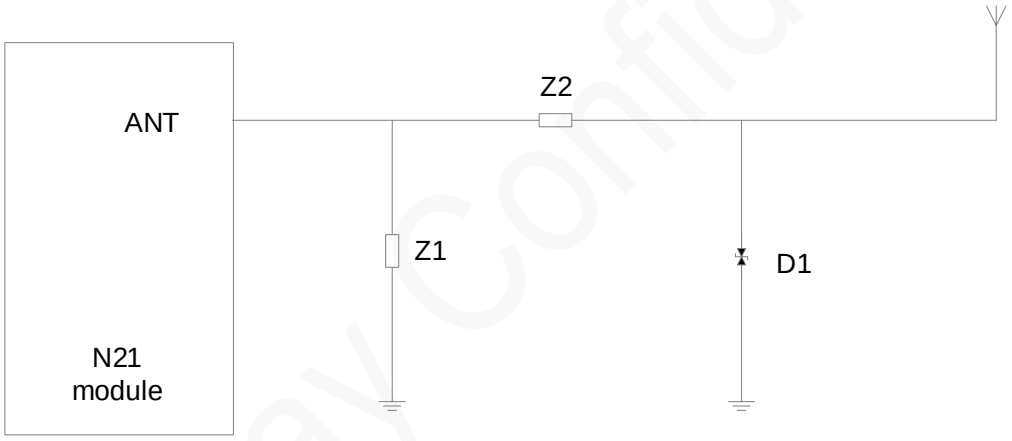


Figure 4-17 T network

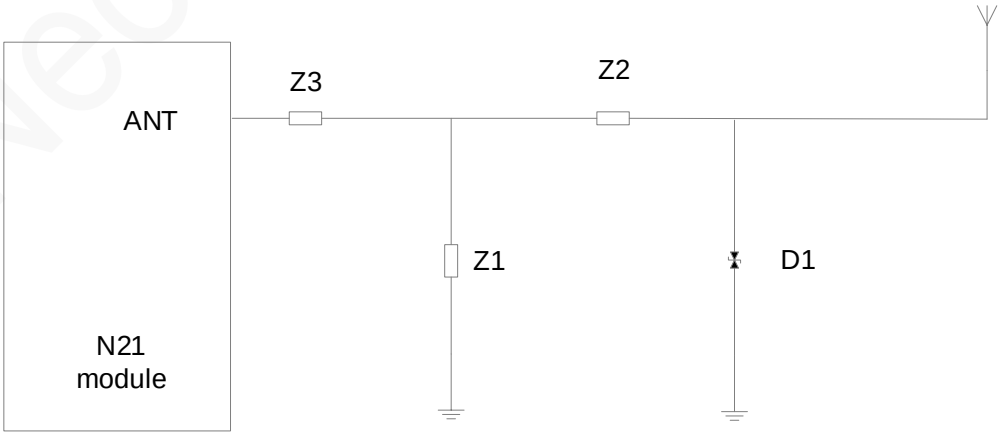
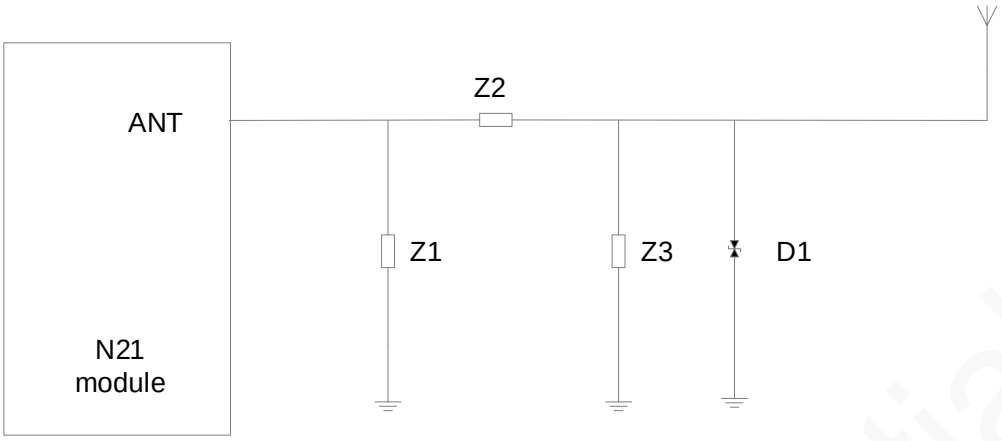


Figure 4-18 Pi network



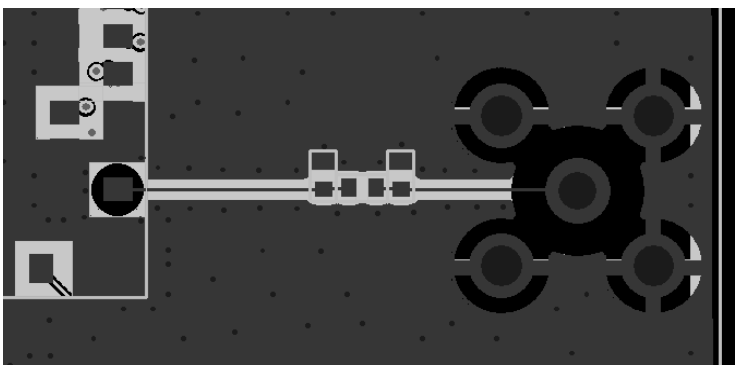
Schematic Design Guidelines

- Element components in the above figures are capacitors, inductors, and 0 Ω resistors. Place these RLC components as close to the antenna interface as possible.
- Add an ESD protector if the antenna might generate static electricity. The protector can be a TVS diode with a junction capacitance of lower than 0.5 pF. Ensure that the reverse breakdown voltage of the TVS is higher than 15 V.

PCB Design Guidelines

- Pour the ground around RF connector. Dig as many vias as possible on the ground plane to ensure lowest ground impedance.
- The traces between N21 and the antenna connector, should be as short as possible. Control the trace impedance to 50Ω.
- If customers adopt SMA connector, big RF solder pad might result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and second layers under the RF solder pad.

Figure 4-19 Recommended RF PCB design



- On the PCB, keep the RF signals and components far away from high-speed circuits, power supplies, transformers, great inductors, the clock circuit, etc.

4.4.2 Antenna Assembling

Antenna used for the module should meet the mobile device requirements: The VSWR ranges from 1.1 to 1.5 and the input impedance is 50Ω. Antenna should be well matched to achieve the best performance in different application scenarios.

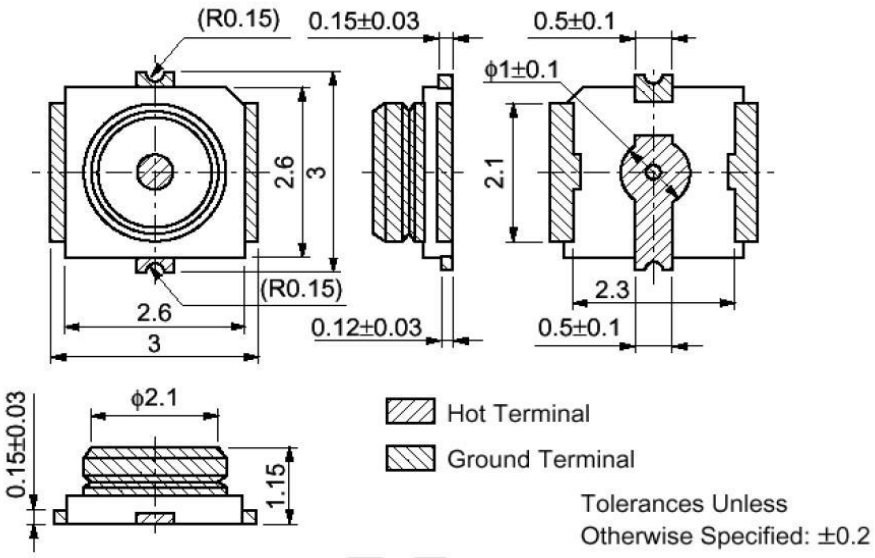
Antenna interfaces can be connected to rubber ducky antenna, magnet antenna, or embedded Planar Inverted F antenna (PIFA). Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.

The following methods are commonly used to assemble antenna:

- GSC RF connector

  MM9329-2700RA1 from Murata is recommended. Figure 4-20 shows its encapsulation specifications.

Figure 4-20 Specifications of MM9329-2700RA1



- Soldering

  RF wire can also be soldered to connect to the module. Ensure sufficient soldering in case of damage that lowers RF performance.

Figure 4-21 shows the two types of connections.

Figure 4-21 RF connections

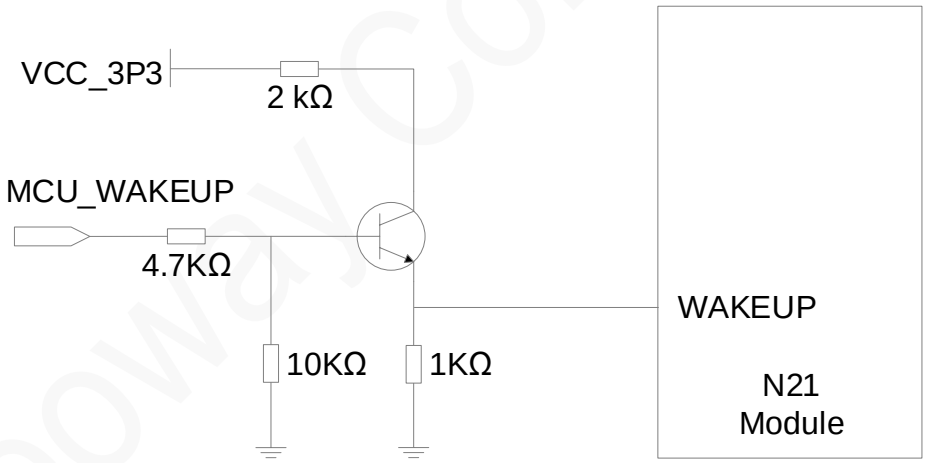
4.5 Other Interfaces

4.5.1 WAKEUP

This pin is used to wake up N21 from PSM mode. After N21 enters PSM mode, input high level at WAKEUP pin for more than 1 second to wake up the module to send data. However, the module will not register with networks proactively after wake up. Therefore, users need to send a data transmitting request. For details, see *Neoway_N21_AT_Command_Manual*.

Figure 4-22 shows the reference design of WAKEUP pin.

Figure 4-22 Reference design of WAKEUP

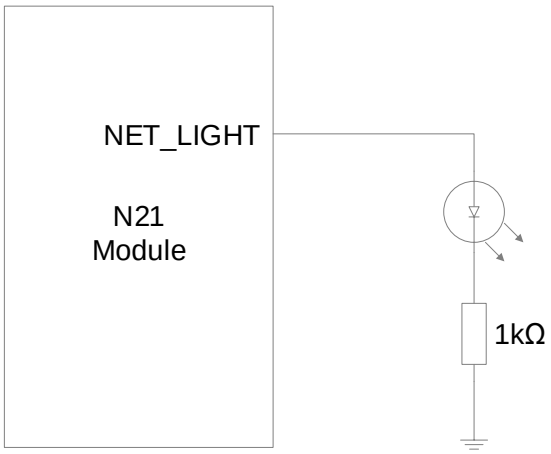


4.5.2 NET_LIGHT

NET_LIGHT outputs a high level of 2.8V and a maximum driving current of 4 mA.

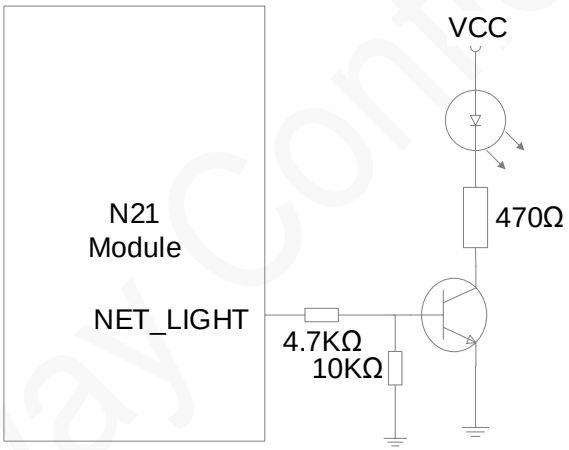
High level is allowed to drive a common LED indicator directly. See Figure 4-23.

Figure 4-23 Driving LED directly



For better luminance, drive the LED with a transistor instead. See Figure 4-24.

Figure 4-24 Driving LED with a triode



For details, see *Neoway_21_AT_Command Manual*.

4.5.3 STATUS

STATUS is used to indicate whether N21 is started up successfully. It can drive an LED indicator directly or through an triode. Its schematic design is simillar to that of NET_LIGHT. See Figure 4-23 and Figure 4-24.

5 Electric Features and Reliability

This chapter describes the electrical features and reliability of N21.

5.1 Electric Features

Table 5-1 Operating conditions of N21

Pin	Parameter	Minimum Value	Typical Value	Maximum Value
VBAT	V_{in}	3.3 V	3.8 V	4.3 V
	I_{in}	/	/	500 mA

If the input voltage is lower than the minimum value, the module might fail to start. If the voltage exceeds the high threshold or there is a voltage burst during the startup, the module might be damaged permanently.

If LDO or DC-DC is used to supply power for the module, ensure that it outputs a current of at least 500 mA.

Table 5-2 Current consumption of N21 (typical)

Status / Band	Power (dBm)	PSM (μA)	Idle (DRX/eDRX) (mA)	Active (mA)	
				TX	RX
Cat NB1: B3, B5, B8, B20, B28	23	<4.5	1.7/1	180	30
	0	<4.5	1.7/1	51	30
	-10	<4.5	1.7/1	36	30

5.2 Temperature Features

Table 5-3 Temperature features of N21

Status	Minimum Value	Typical Value	Maximum Value
Operating	-30°C	25°C	75°C
Storage	-45°C		90°C

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse but it can still work properly.

5.3 ESD Protection

Electronics need to pass ESD tests. The following table shows the ESD capability of key pins of this module. It is recommended to add ESD protection based on the application scenarios to ensure product quality when designing a product.

Humidity 45%, Temperature 25°C

Table 5-4 N21 ESD protection

Testing Point	Contact Discharge	Air Discharge
VBAT	±8KV	±15KV
GND	±8KV	±15KV
ANT	±8KV	±15KV
Cover	±8KV	±15KV
Others	±2KV	±4KV

6 RF Features

This chapter describes the RF features of N21.

6.1 Operating Bands

Table 6-1 Operating bands of N21

Operating Band	Uplink	Downlink
FDD-LTE B3	1710~1785MHz	1805~1880MHz
FDD-LTE B5	824~849MHz	869~894MHz
FDD-LTE B8	880~915MHz	925~960MHz
FDD-LTE B20	832~862MHz	791~821MHz
FDD-LTE B28	703~748MHz	758~803MHz

6.2 TX Power and RX Sensitivity

Table 6-2 RF TX power of N21

Band	Max Power	Min. Power
HD-FDD LTE B3	23dBm+2/-2dBm	<-40 dBm
HD-FDD LTE B5	23dBm+2/-2dBm	<-40 dBm
HD-FDD LTE B8	23dBm+2/-2dBm	<-40 dBm
HD-FDD LTE B20	23dBm+2/-2dBm	<-40 dBm
HD-FDD LTE B28	23dBm+2/-2dBm	<-40 dBm

Table 6-3 RX sensitivity of N21 Cat NB1 (retransmission unsupporting)

Band	Sensitivity	Duplex Mode
LTE B3, B5, B8, B20, B28	≤-113 dBm	HD-FDD

The values were obtained by RF analyzers in lab.

7 BLE Function

Developed on the RDA8908A chip, the N21 implemented the BLE-GATT data transmission function to allow customers configure and upgrade over a wireless connection.

N21 provides the following functions relevant to BLE:

- The device name can be modified through AT commands.
- Only the slave mode of the BLE function is supported.
- Authentication is not supported for the BT connection.

The transmissioin rate of the BLE-GATT reachs 4.77KBps(TX) and 5.328KBps(RX). After the BLE function is enabled, the power consumption increases by 5 mA to 9.6 mA and the operating frequency is 2.4 GHz.

The data came from the test on the data interaction between the N21 module and the App of a mobile phone or common BT modules.

Table 7-1 Operating current of GATT

Test Content	Current	Remarks
Idle mode	1.5 mA	Test instrument: CMW500
BLE is enabled but unpaired	9.2 mA	-
BLE is enabled and paired	7.5 mA	-
Transmit data over the BLE connection	10.1 mA	Uplink speed: 200 Byte/s
Receive data over the BLE connection	11.1 mA	Downlink speed: 200 Byte/s

Table 7-2 Transmission speed of GATT

Test Content	Speed	Remarks
N21->APP	4.774 KBps	Data transmitting
N21->HM-16	4.774 KBps	
N21->E104-BT02	3.7 KBps	
APP->N21	5.328 KBps	Data receiving
HM-16->N21	5.239 KBps	

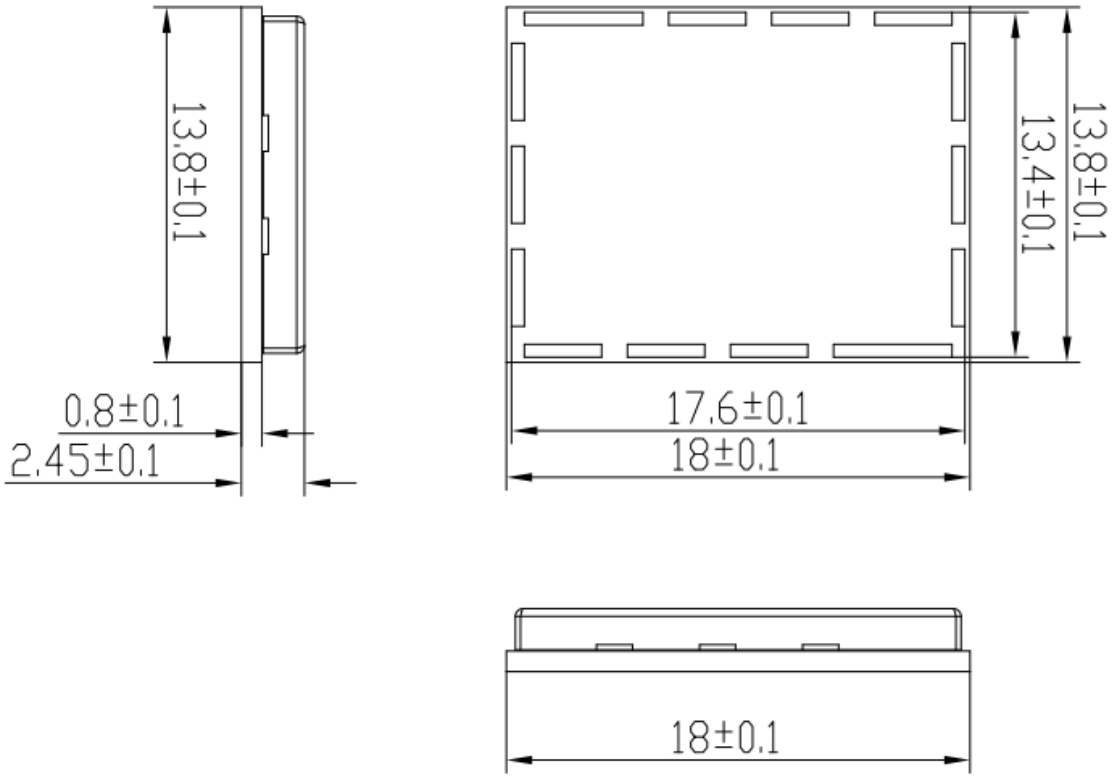
E104-BT02->N21	1.4 KBps

8 Mechanical Features

This chapter describes the mechanical features of N21.

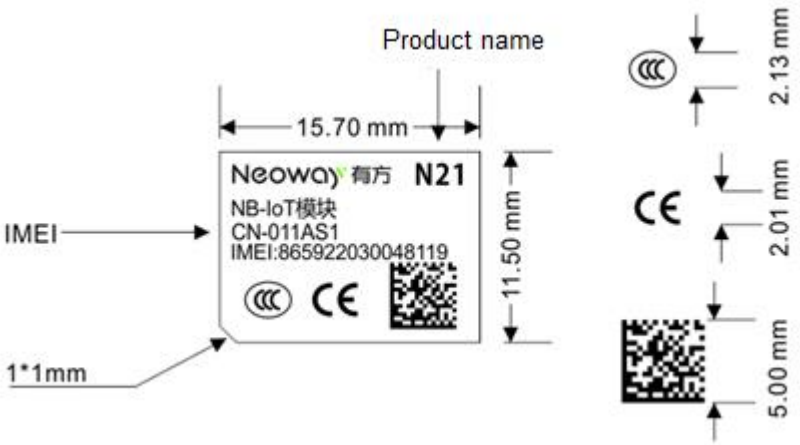
8.1 Dimensions

Figure 8-1 N21 dimensions (unit: mm)



8.2 Label

The label is made of materials that are deformation-resistant, fade-resistant, and high-temperature-resistant and it can endure high temperature up to 260 °C.



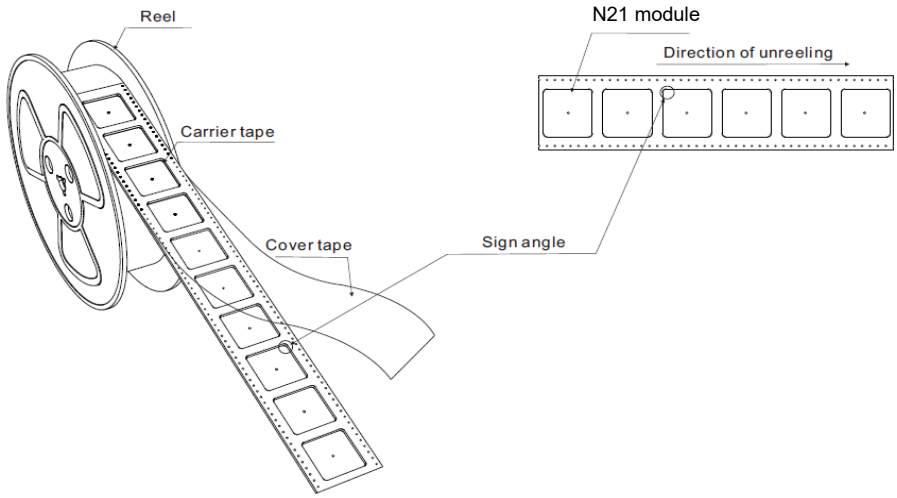
- The picture above is only for reference.
- The silk-screen printing must be clear. No blur is allowed.
- The material and surface finishing must comply with RoHS directives.

8.3 Package

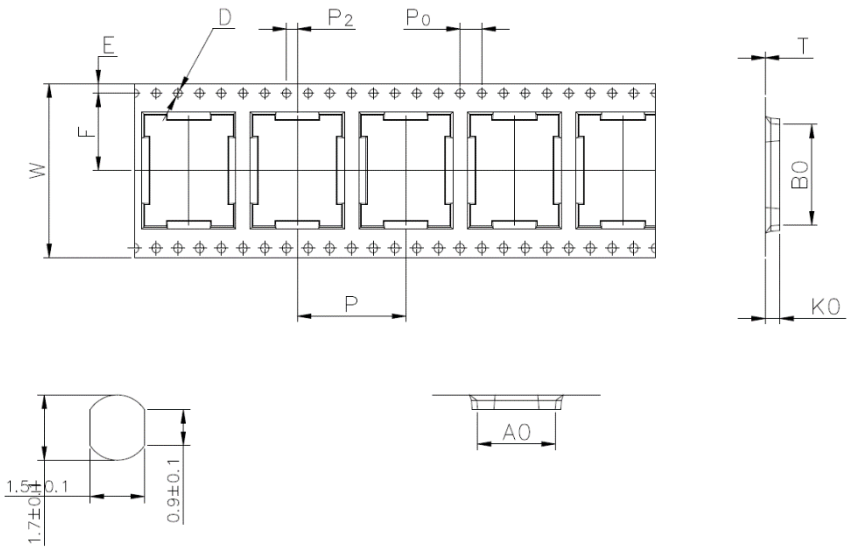
N21 modules are packed in sealed bags on delivery to guarantee a long shelf life. Follow the same package of the modules again in case of opened for any reasons.

8.3.1 Tape&Reel Packaging

N21 in mass production are shipped in the following package.

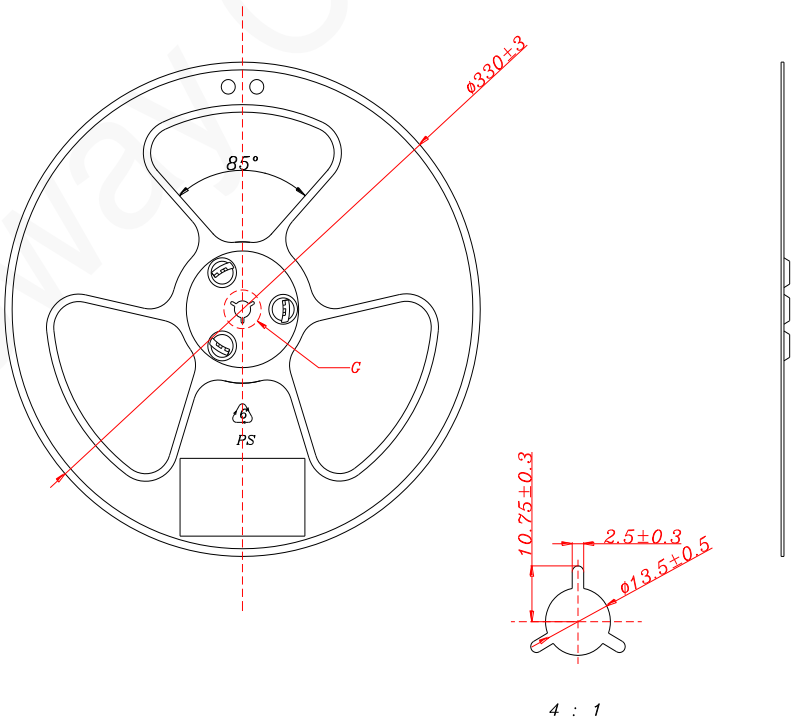


Tape



EIA DIMENSIONS	
W	$32.0^{+0.30}_{-0.30}$
E	$1.75^{+0.10}_{-0.10}$
F	$14.2^{+0.15}_{-0.15}$
P	$24.0^{+0.10}_{-0.10}$
P_0	$4.00^{+0.10}_{-0.10}$
P_2	$2.00^{+0.15}_{-0.15}$
D	$1.50^{+0.10}_{-0.10}$
T	$0.35^{+0.05}_{-0.05}$
A_0	$14.3^{+0.10}_{-0.10}$
B_0	$18.5^{+0.10}_{-0.10}$
K_0	$2.70^{+0.10}_{-0.10}$

Reel



8.3.2 Moisture-Sensitive

N21 is a level 3 moisture-sensitive electronic elements, in compliance with IPC/JEDEC J-STD-020 standard.

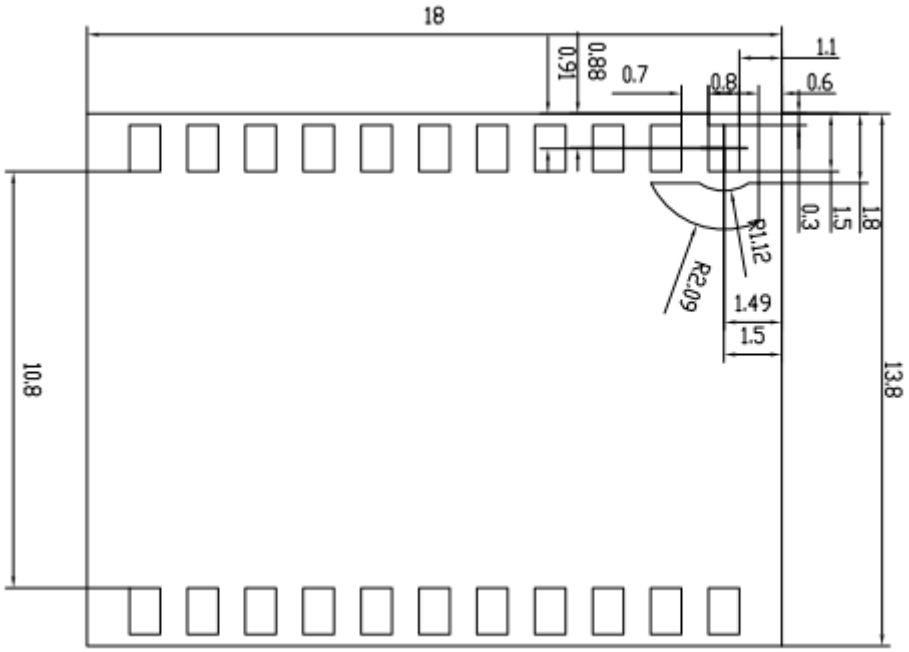
If the module is exposed to air for more than 48 hours at conditions not worse than 30°C/60% RH, bake it at a temperature higher than 90 degree for more than 12 hours before SMT. Or, if the indication card shows humidity greater than 20%, the baking procedure is also required.Do not bake modules with the package tray directly.

9 Mounting N21 onto Application Board

N21 is introduced in 22-pin LGA package. This chapter describes N21 foot print, recommended PCB design and SMT information to guide users how to mount the module onto application PCB board.

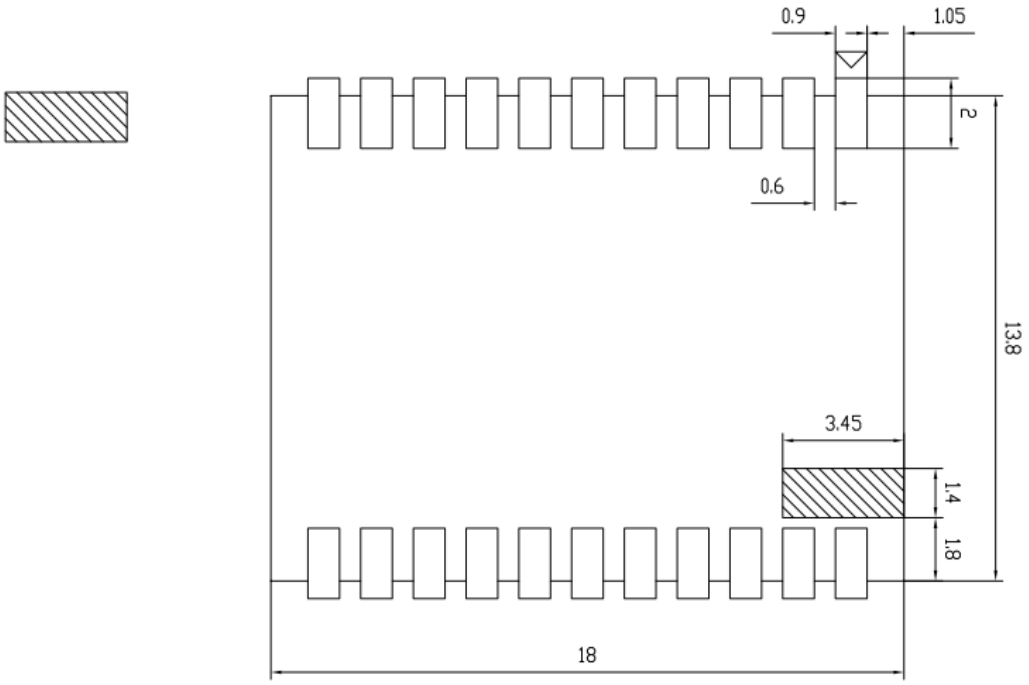
9.1 Bottom Dimensions

Figure 9-1 N21 bottom dimensions (Unit: mm)



9.2 Application Foot Print

Figure 9-2 Recommended PCB foot print (Unit: mm)



The area on the module corresponding to the shade is GND copper foil for production. Do Not route any signal lines or drill signal via-holes in the shaded area of the application PCB.

Only GND traces and GND via-holes are allowed in this area. Otherwise, the signal lines might be short-circuited.

9.3 Stencil

The recommended stencil thickness is at least 0.15 mm to 0.20 mm.

9.4 Solder Paste

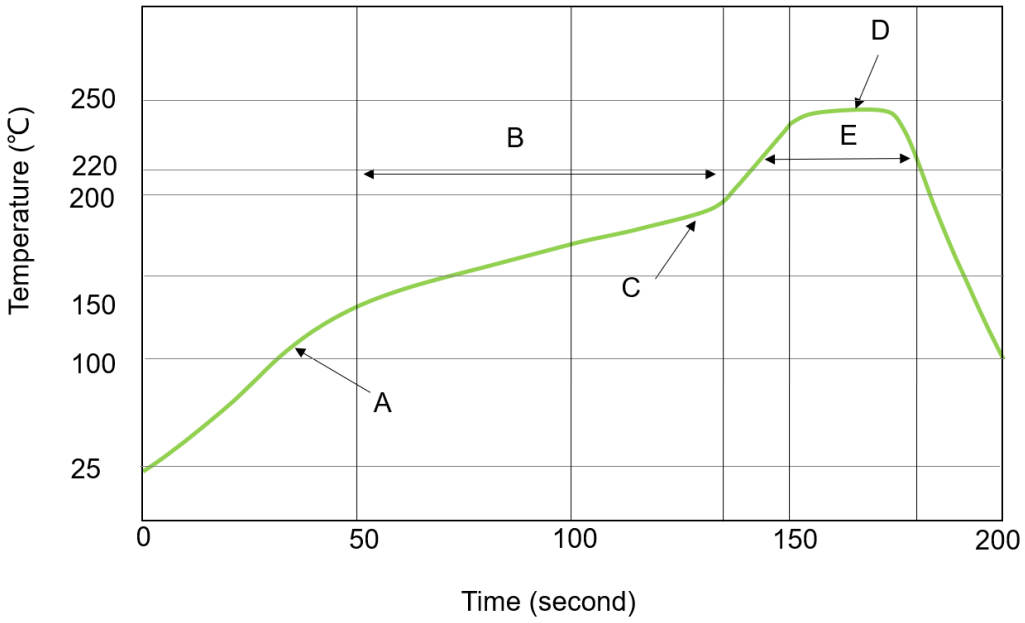
Do not use the kind of solder paste different from our module technique.

- The melting temperature of solder paste with lead is 35 °C lower than that of solder paste without lead. It is easy to cause voiding for LCC inside the module after second reflow soldering.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220 °C for more than 45 seconds and the peak temperature reaches 240°C.

9.5 SMT Profile

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 9-3 SMT furnace temperature curve



Technical parameters:

- Ramp up rate: 1 to 4°C/sec
- Ramp down rate: -3 to -1°C/sec
- Soaking zone: 150-180 °C, Time: 60-100s
- Reflow zone: >220 °C, Time: 40-90s
- Peak temperature: 235-245°C

Neoway will not provide warranty for heat-responsive element abnormalities caused by improper temperature control.

For information about cautions in N21 storage and mounting, refer to *Neoway_Reflow_Soldering_Guidelines_For_Surface-Mounted_Modules*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 245 degrees (depending on the type of the solder paste), and heat the module till the solder paste is melt. Then remove the module using tweezers. Do not shake the module in high temperatures while

removing it. Otherwise, the components inside the module might get misplaced.

A Abbreviations

Abbreviation	Full Name
ADC	Analog-Digital Converter
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCE	Data Communication Equipment
DTE	Data Terminal Equipment
PTW	Paging Time Window
PSM	Power Save Mode
DRX	Discontinuous Reception
eDRX	Extended Discontinuous Reception
EMC	Electromagnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electronic Static Discharge
ETSI	European Telecommunication Standard
FDMA	Frequency Division Multiple Access
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MS	Mobile Station
PCB	Printed Circuit Board
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
TVS	Transient Voltage Suppressor
RTC	Real Time Clock
USIM	Subscriber Identification Module
SRAM	Static Random Access Memory

TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VSWR	Voltage Standing Wave Ratio

