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N25

Hardware User Guide

NB-IoT Module
Issue 1.7
Date 2023-11-17

Notice

This document is specifically for N25.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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Contents

Table of Figures

Table of Tables

About This Document

Scope

This document is applicable to N25 series.

It defines the features, indicators, and test standards of the N25 module and provides reference for the hardware design of each interface.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Date	Change	Changed By
1.0	2019-02	Initial draft	Huang Jianlong
1.1	2019-04	• Updated startup timing, shutdown timing, and reset timing • Added the caution of supply voltage	Huang Jianlong
1.2	2020-02	• Added Cat NB2 • Added functions related to 3GPP Release 4 • Changed the thickness of the module • Changed the operating temperature range • Changed the reset schematic diagram • Changed the startup timing • Changed the remarks of UART1_RXD	Zhao Rongzhou
1.3	2020-05	• Corrected the wireless rate of NB-IoT • Corrected the tolerance information of the module dimensions.	Zhao Rongzhou.
1.4	2023-06	• Added UART interface explanation.	Xique Yan
1.5	2023-07	• Modified VBAT voltage range.	Liang Hui
1.6	2023-10	• Revised and updated content in Section 3.3.1 and Section 3.2. •	Liang Hui

1.7	2023-11	• Updated Figure 3-11.	Liang Hui

Conventions

Symbol	Indication
	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
	Means note or tips for readers to use the module

Related Documents

Neoway_N25_Datasheet

Neoway_N25_AT_Commands_Mannual

Neoway_N25_EVK_User_Guide

1 Safety Recommendations

Please carefully read and strictly abide by the following safety requirements to ensure that the product application meets the national laws and environmental regulations, avoid risks to personal safety, and protect the product and application scenario from possible damage:

- Do not use the module in places where fire and explosion may occur.

  If the module is used in places filled with flammable gases and dust such as propane gas, gasoline and combustible spray, it will lead to explosion or fire.

- In places where wireless communication is prohibited, please disable the wireless communication function.

  In medical facilities or aircraft, the electromagnetic waves emitted by the module may interfere with the operation of surrounding equipment.

During the product application design and use of this module, the following requirements should be met:

- Do not disassemble the product of this module without permission. Otherwise, after-sales warranty service will not be available for the product.
- Design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touching the pins of the module directly in case of damages caused by ESD.
- Do not insert or remove (U)SIM card or mobile device memory card if the product is not in power-off mode.

2 Product Introduction

N25 is a customized NB-IoT+GPRS industrial-grade cellular module for mobile applications. This chapter provides an overview of its features, introduces its basic functional framework, and details its specification parameters.

2.1 Product Overview

Table 2-1 lists the variant and bands that N25 supports.

Table 2-1 Supported frequency bands

Variant	Category	Band configuration
N25-CN-011AS1	Cat NB/GPRS	Cat NB1/Cat NB2: HD-FDD B3,B5,B8 GPRS: 900/1800 MHz
N25-EU-011AS1	Cat NB/GPRS	Cat NB1/Cat NB2: HD-FDD B3,B5,B8,B20,B28 GPRS: 850/900/1800/1900 MHz

N25 stands out for its ultra-low power consumption, extensive coverage, and straightforward peripheral circuits, making it ideal for developing low-speed, low-power IoT communication devices. The module features a 52-pin LGA package with external dimensions of only 24 mm x 20 mm x 2.45 mm, satisfying the space requirements of most customers.

N25 offers the following hardware resource functions:

- UART interfaces for data communication, firmware updates, and commissioning.
- Compatibility with 1.8 V/3.0V USIM cards.
- Hardware resources like STATUS (indicating operational status), WAKEUP_IN (for PSM wakeup), RESET_N, and ADC.

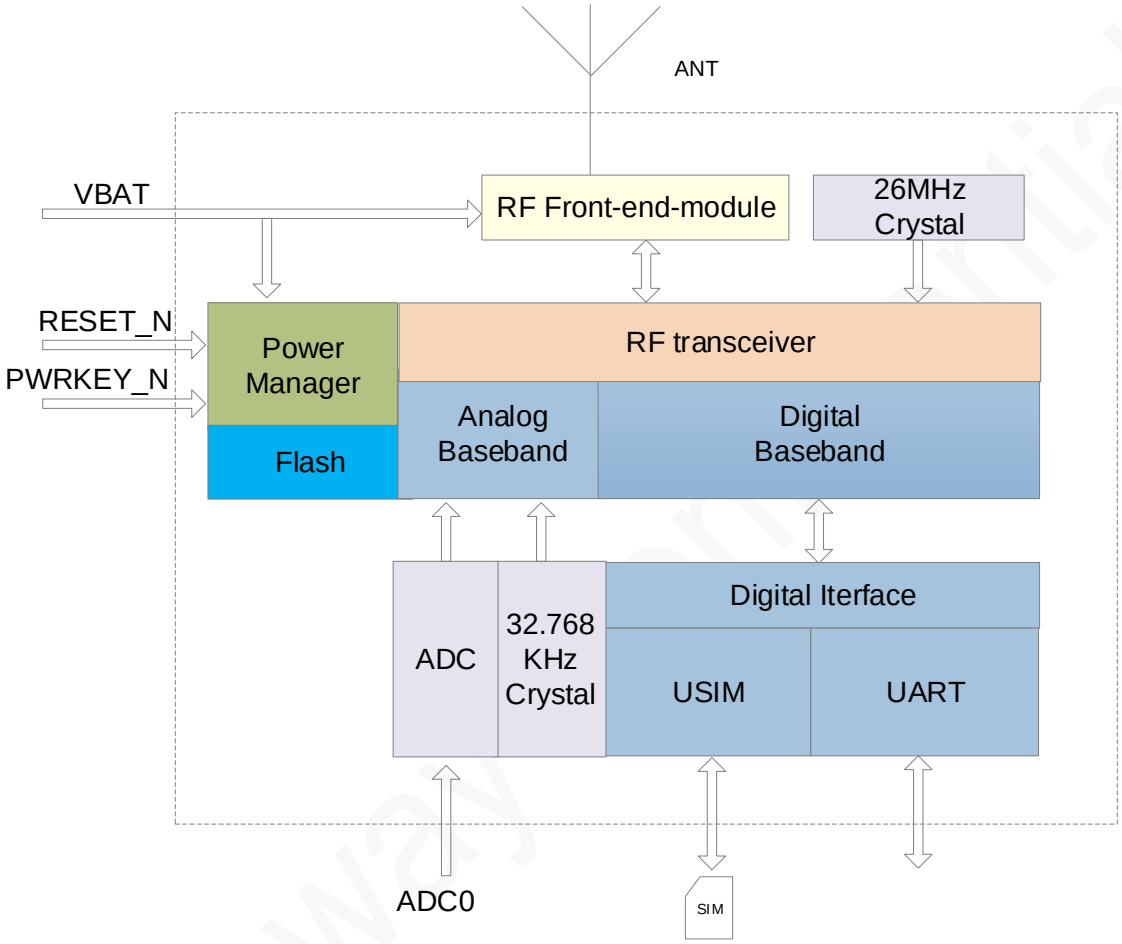
2.2 Block Diagram

The N25 module includes the following functional units:

- Power supply unit
- Clock unit

- Digital interface (USIM, UART)
- Analog interface (ADC)
- RF section

Figure 2-1 Block diagram



2.3 Basic Features

Parameter	Description
Physical features	• Dimensions: (24±0.10mm) x (20±0.10mm) x (2.45±0.10mm) • Package: 52-Pin LGA • Weight: about 1.8 g
Temperature ranges	Operating: -40°C to +85°C Storage: -45°C to +90°C

Operating voltage	VBAT: 3.41 V - 4.30 V, Typ.: 3.8 V
Application processor	MIPS processor, with CPU clock speed up to 192 MHz, 16 kB L2 cache
Memory	RAM: 32Mb ROM: 32Mb
Band	B3, B5, B8, B20, B28
Wireless rate	LTE Cat NB1: 26Kbps (DL)/62.5Kbps (UL) LTE Cat NB2: 127Kbps (DL)/158.5Kbps (UL) GPRS: 85.6 Kbps (DL/UL)
Transmit power	LTE: +23dBm+/-2dB (Power Class 3) GPRS 850/900: 33 dBm+/-2dB GPRS 1800/1900: 30 dBm+/-2dB
Application Interfaces	Antenna interface: One 4G antenna with 50 Ω characteristic impedance
	One set of UART ports (UART1) with hardware flow control, used for sending AT commands.
	SIM Card Interface: One UIM interface, adaptable to 1.8 V/3 V.
	One ADC interface
	Can embed 2x2 mm eSIM (optional)
AT commands	3GPP Rel-13 3GPP Rel-14 Neoway extended AT commands
SMS	TEXT/PDU Point to Point/Cell Broadcast
Cloud platform	China Mobile OneNet, China Telecom Tianyi Cloud, Huawei OceanConnect Platform
Protocols	CoAP/UDP/LWM2M/TCP/IP/PPP/DNS/FTP/HTTP/HTTPS/DTLS/SMS
Certification approval	CCC*, Model Approval*, RoHS*, China Mobile's Warehousing Test*

* means under development.

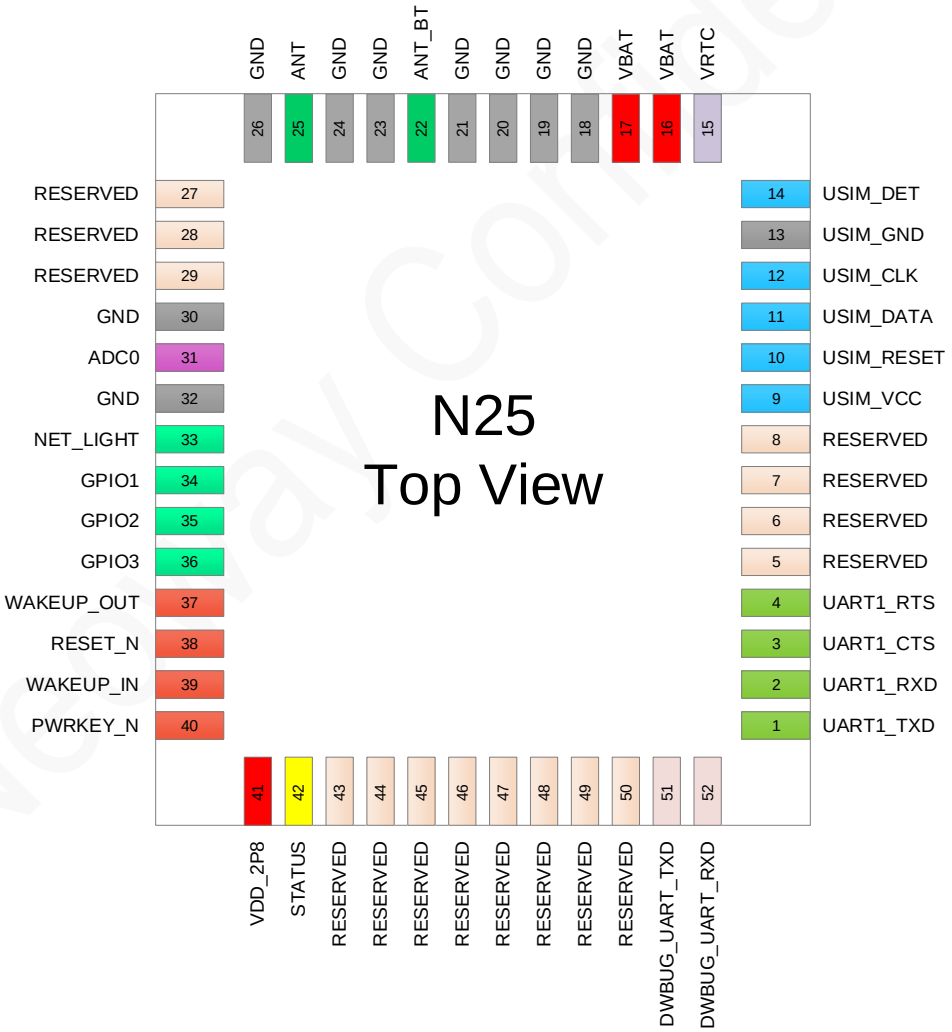
3 Pad Layout

There are 52 pins on N25 and their pads are introduced in LGA package.

3.1 Pad Layout

The following figure shows the pad layout of N25.

Figure 3-1 N25 pad layout



3.2 Pin Description

Table 2-1 lists the definition of IO types.

Table 3-1 IO definition

IO type			
DO	Digital output, CMOS logic level		
DI	Digital input, CMOS logic level		
PO	Power output		
PI	Power input		
AO	Analog output		
AI	Analog input		
DC characteristics			
P1	SIM interface, supporting both 1.8 V and 3.0 V (U)SIM cards	1.8 V DC characteristics: V_{IH}=1.26 V - 1.8 V, V_{IL}=-0.3 V - 0.36 V V_{OH}=1.44 V - 1.8 V, V_{OL}=0 V - 0.4 V	3.0 DC characteristics: V_{IH}=2 V - 3 V, V_{IL}=-0.3 V - 0.57 V V_{OH}=2.28 V - 3 V, V_{OL}=0 V - 0.4 V
P2	2.8 V digital IO	V_{IH} =2.1V - 2.8V, V_{IL}= 0V - 0.7V V_{OH}=2.1 - 2.8V, V_{OL}=0V - 0.7V	
P3	V_RTC power domain 1.1V	$V_{IH\ min}$=0.68V, $V_{IH\ max}$= 1.41V $V_{IL\ min}$=-0.3V, $V_{IL\ max}$= 0.36V	

Table 3-2 Pin description

Signal	Pin SN	I/O	Function description	Level feature	Remarks
Power Interfaces					
VBAT	16, 17	PI	Main power supply input	V_{max}=4.3 V	-
VRTC: Backup Power for RTC	15	PI	RTC backup input	V_{max}=1.4 V	Leave this pin open if unused.
VDD_2P8	41	PO	2.8 V power output	V_{norm}=2.8 V I_{max}=50 mA	Used only for level translation and IO power supply. Leave this pin open if unused.

GND	13, 18, 19, 20, 21, 23, 24, 26, 30, 32				Make sure all GND pins are grounded.
Control Interfaces					
RESET_N	38	DI	Module reset input	P3	Active low
PWRKEY_N	40	DI	Module on/off control	P3	A low pulse for a valid time period can trigger on/off of the module (see section 4.2.1).
UART interface					
UART1_CTS	3	DI	UART data output	P2	-
UART1_RTS	4	DO	UART data input	P2	-
UART1_TXD	1	DO	UART data output	P2	Software version (Standard): For AT communication
UART1_RXD	2	DI	UART data input	P2	
DEBUG_UART Interfaces					
DEBUG_UART_TXD	51	DO	UART data output	P2	Software (standard) version: for software download and log capture. It is recommended to reserve the test points.
DEBUG_UART_RXD	52	DI	UART data input	P2	
USIM interface					
USIM_DET	14	DI	USIM in-place detection	P2	-
USIM_RESET	10	DO	USIM reset	P1	-
USIM_CLK	12	DO	USIM clock output	P1	-
USIM_DATA	11	DIO	SIM data input and output	P1	-
USIM_VCC	9	PO	SIM power output	IO_{max}=50mA	USIM_VCC
ADC interface					
ADC0	31	AI	ADC input		Leave this pin open if unused. Max input 1.8 V.
Antenna interfaces					
ANT	25	AI/O	Antenna pin		Control the impedance of

					antenna traces at 50Ω.
ANT_BT	22	AI/O	BT/ WIFI antenna pin		Control the impedance of antenna traces at 50Ω.
Other interfaces					
WAKEUP_OUT	37	DO	Reset external chips	P2	Leave this pin open if unused.
WAKEUP_IN	39	DI	PSM wakeup control input	P3	Maintaining a high level for 1 second can activate the wake-up function.
STATUS	42	DO	Startup indication	P2	Leave this pin open if unused.
NET_LIGHT	33	DO	Network status indicator	P2	Leave this pin open if unused.
GPIO_1	34	IO	GPIO	P2	Leave this pin open if unused.
GPIO_2	35	IO	GPIO	P2	Leave this pin open if unused.
GPIO_3	36	IO	GPIO	P2	Leave this pin open if unused.
Reserved pin					
RESERVED	5, 6, 7, 8, 27, 28, 29, 43, 44, 45, 46, 47, 48, 49, 50				Must be left unconnected; do not connect them to a power source or ground.

4 Application Interfaces

N25 provides the power, control, communications, peripherals, and RF interfaces to meet the functional requirements of customers in different application scenarios. This chapter describes how to design each interface and provides reference designs and guidelines. Please adhere to the guidelines detailed in this chapter, considering aspects such as trace width, component placement, and impedance control to implement best practices in circuit design to ensure optimal performance and reliability.

4.1 Power Interfaces

The power interfaces play a pivotal role in application design, with both the schematic design and PCB layout serving as critical components. Their configuration directly impacts the performance of customers' applications. Please read the design guidelines of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin SN	I/O	Function description	Remarks
VBAT	16, 17	PI	Module supply input	3.41 V - 4.30 V (Typ.: 3.8 V)
VDD_2P8	41	PO	2.8 V power output	Capable of outputting currents up to 50 mA, this is exclusively for voltage-level translation. Adding ESD protection is recommended during use.
GND	13, 18, 19, 20, 21, 23, 24, 26, 30, 32			Make sure all GND pins are grounded.

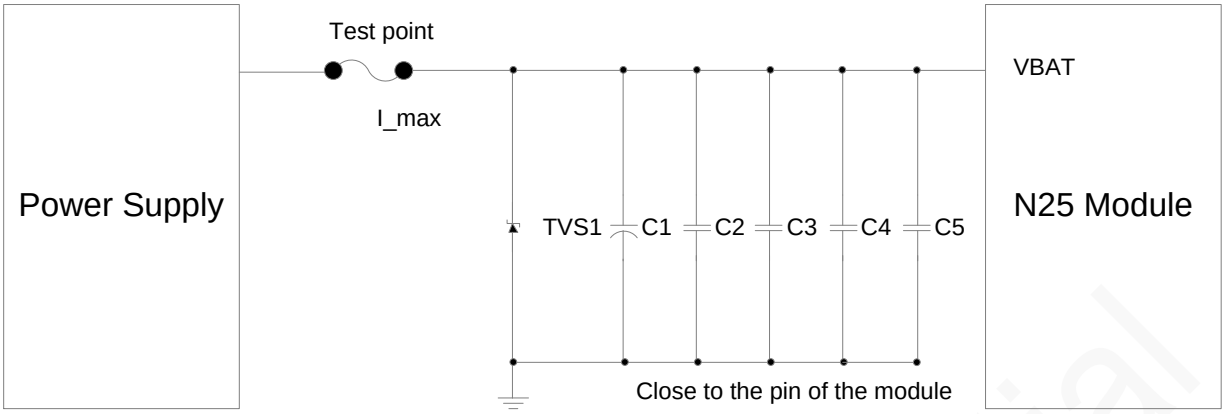
4.1.1 VBAT

The power supply design encompasses two key facets: schematic design and PCB layout. These are integral in sustaining the optimal functionality and safety of the module.

Schematic Design of Power Supply

N25 uses a battery-supplied voltage input of 3.4 V to 4.3V, with 3.8 V as the typical voltage. Figure 4-1 shows the recommended design of the N25 power supply.

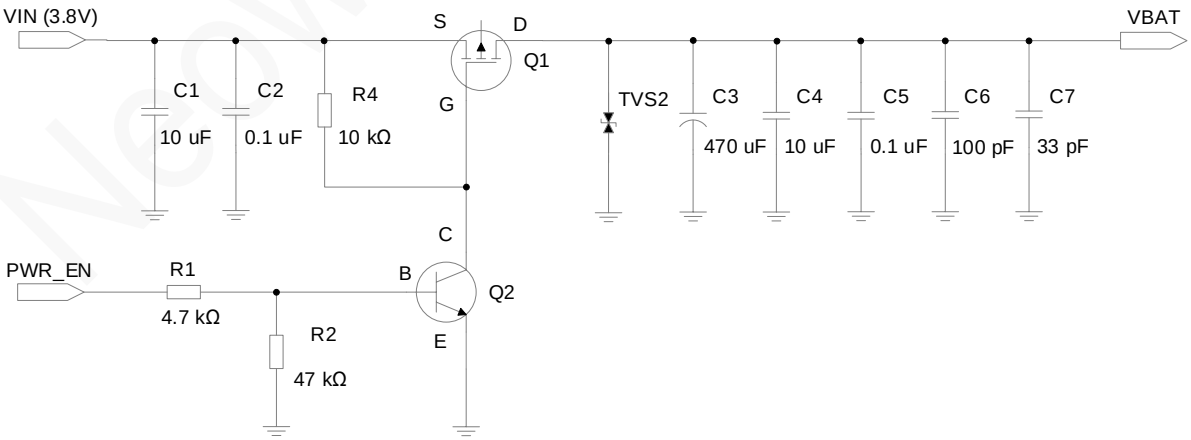
Figure 4-1 Recommended design of the power supply circuit 1



- The maximum input voltage of the module power supply is 4.3 V, and the typical value is 3.8 V.
- The TVS1 protection voltage cannot be higher than the maximum withstands voltage of the module. Place TVS1 close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Choose a tantalum electrolytic capacitor with a large capacitance (either 220 μF or 100 μF), or an aluminum electrolytic capacitor (either 470 μF or 1000 μF) for C1. This improves the power supply's ability to handle instantaneous large freewheeling currents. Ensure the capacitor's withstand voltage value exceeds the power supply voltage by more than 1.5 times.
- Place a low-ESR bypass capacitor near the module to filter out high-frequency interference from the power supply.

If it is necessary to control the power supply, the following circuit design is recommended:

Figure 4-2 Recommended design of the power supply circuit 2



- Choose an enhanced p-MOSFET for Q1 with a maximum safe operating voltage and a drain current exceeding 4 A, and ensure it has a low DC resistance.

- Opt for either a standard NPN bipolar transistor or a digital NPN bipolar transistor for Q2. Design R3 and R4 with sufficient tolerance to accommodate potential increases in the operating voltage of the bipolar transistor at low temperatures.
- Place the TVS diode close to the power input interface to suppress surge voltage before it reaches the downstream circuits, thereby safeguarding both the components and the module.
- Place C3 near the module. Use a tantalum electrolytic capacitor with a large capacitance of either 220 μF or 100 μF, or an aluminum electrolytic capacitor of 470 μF or 1000 μF at C3. This is to enhance the power supply's ability to handle large instantaneous currents. The chosen capacitor's voltage rating must exceed the power supply voltage by at least 1.5 times.
- Place a low-ESR bypass capacitor near the module to filter out high-frequency interference from the power supply.

PCB Layout Guidelines

A low ESR capacitor must be placed at the output side of the power supply to suppress the peak current. Add TVS diodes at the input of the power supply to suppress voltage spikes and protect back-end components. Several key points in power supply design are summarized below:

- The TVS diode can absorb instantaneous high-power pulses and withstand instantaneous pulse current peaks up to tens or even hundreds of amperes. The clamp response time is extremely short.
- Place the TVS diode near the power input. This helps control surge voltage and prevents pulses from affecting nearby PCB wires.
- Place bypass capacitors as close as possible to the power supply interface of the module to filter out high-frequency noise signals in the power supply.
- For the main power circuit of the module, the PCB trace width must be sufficient to safely carry a 2 A current (as required for GSM) without significant voltage drop.
- Ensure the PCB traces are at least 2 mm wide to maintain the integrity of the power section's ground plane.
- In addition, keep the power cable short and thick.
- Place noise-sensitive circuits, such as audio and radio frequency (RF) circuits, especially when using DC-DC power sources, far from power circuits to avoid interference.

It is not recommended to use a diode for creating a voltage drop for module power supply. Any product issues or performance problems resulting from this modification may lead to the voiding of the product warranty. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, due to the forward voltage of the diode will vary greatly in different temperature and current. Due to these two reasons, the diode step-down method will lead to unstable operation of the module.

4.1.2 VDD_2P8

N25 provides one VDD_2P8 output. It can provide the 2.8 V voltage and the maximum output current is 50 mA.

You do not need to control VDD_2P8; the module automatically turns it on during wake-up and active states.

It is recommend to use VDD_2P8 solely for level translation and not for other purposes. It is essential to add ESD protection if you use it.

4.1.3 VRTC

The VRTC pin is the input pin for the backup power supply of the RTC. External power sources can provide power to the module's RTC, with a maximum input of 1.4 V.

4.2 Control Interfaces

Signal	Pin SN	I/O	Function description	Remarks
RESET_N	38	DI	Module reset input	Active low
PWRKEY_N	40	DI	Module on/off control	Active low

4.2.1 PWRKEY_N

N25 allows startup by the following methods:

- By button
- By MCU
- Automatic start once powered up

Figure 4-3 Reference design of power-on controlled by buttons

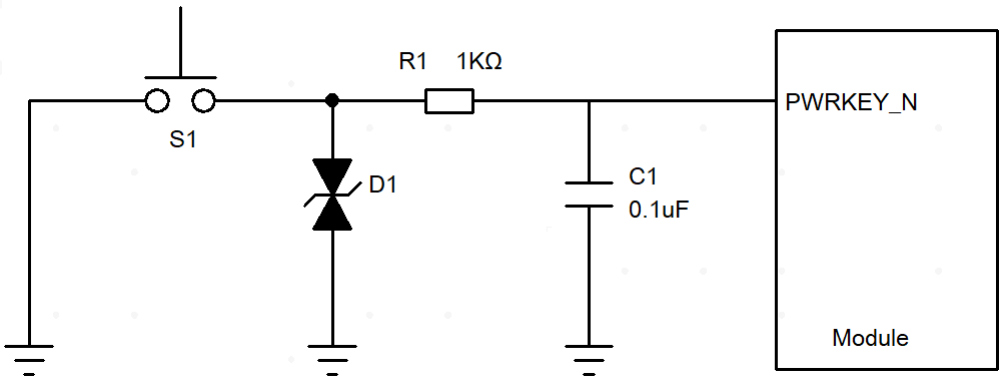


Figure 4-4 Reference design of MCU-control power-on

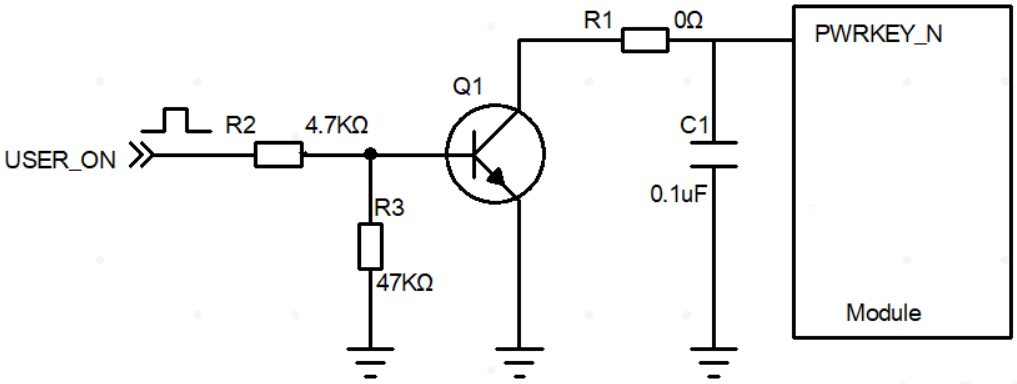
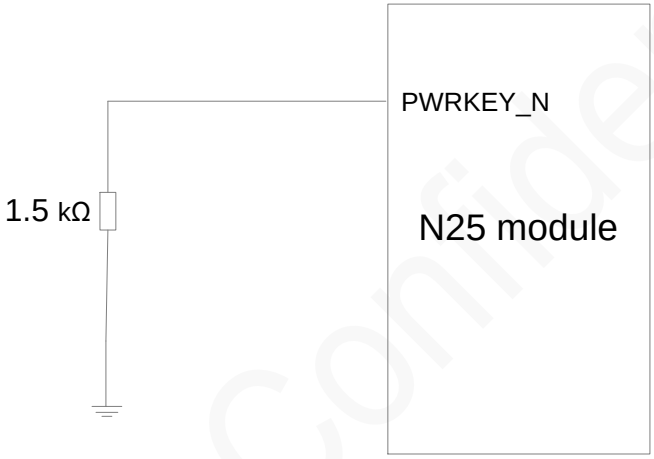


Figure 4-5 Reference design of automatic startup once powered up



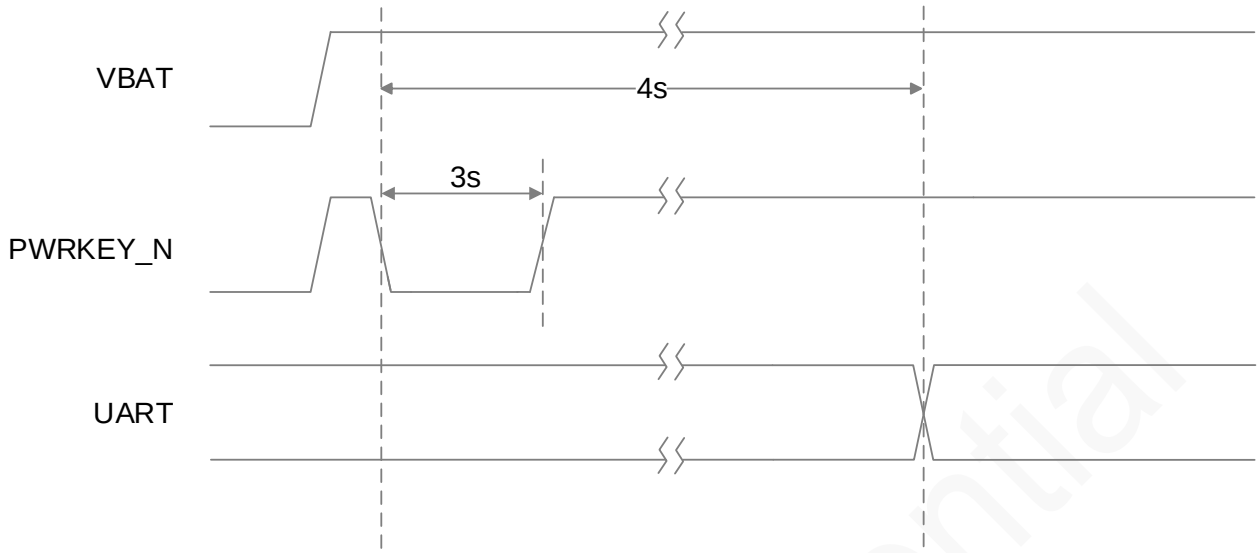
Power-on Process

Apply power to VBAT. Pull the PWRKEY_N pin for at least 3 seconds to start the module. After starting the module, set the PWRKEY_N pin high. Then, the STATUS LED will light up to signal the module's successful initialization. Note that in NB-IoT modules, due to the adaptive baud rate, the serial port baud rate varies. To make the serial port operational, send an AT command. The port will adapt to the incoming baud rate and respond, typically with a code like "+PBREADY." Then, you can execute further AT commands. For the power-on process, see Figure 4-6.

During programming, if the module outputs “+PBREADY”, it indicates a successful reset.

For automatic startup upon power-up, you can refer Figure 4-5 for design. Note that this circuit does not support a shutdown function.

Figure 4-6 Power-on process



For a proper power-on sequence, it is recommended to first power up the external main control MCU and then power up the module's main supply after the MCU's serial port is initialized. If not, indeterminate signals from the MCU during its serial port initialization may cause the module to respond incorrectly."

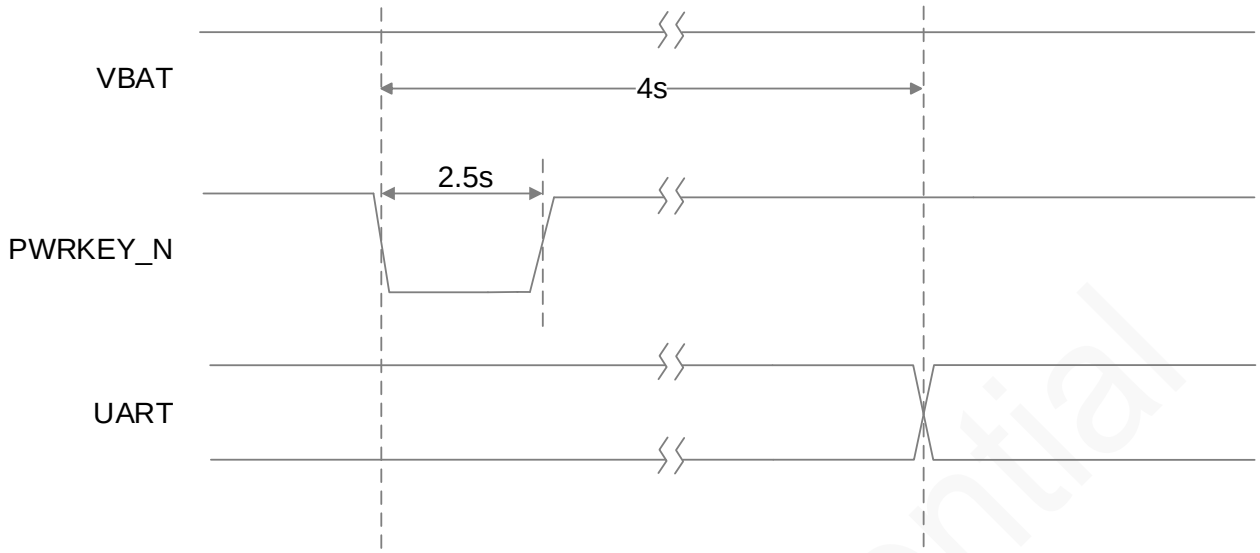
Power-off Process

There are two methods to turn off the module: using the PWRKEY_N pin for a hardware shutdown, or a software-based shutdown.

Hardware Shutdown: To perform a hard shutdown, send a low-level pulse lasting more than 2.5 seconds through the PWRKEY_N pin while the module is in its normal working state. This initiates the shutdown process, which typically takes about 3 seconds. After this period, turn off the main power supply to complete the shutdown.

The following figure shows the hardware power-off process:

Figure 4-7 Power-off process



Software Shutdown: For instructions on how to power off the module using software, refer to the "*Neoway_N25_AT_Commands_Manual*".

4.2.2 RESET_N

RESET_N is the module's reset control. To reset the module while it's powered on, input a negative pulse lasting over 50 ms to RESET_N.

For the reference design of the demo board, please refer to Figure 4-8. If you are using an IO system with 2.8 V, 3.0 V, or 3.3 V, we recommend using a triode for isolation and implementing a high-level reset (MCU). For more details, refer to Figure 4-9.

Figure 4-8 Reference design for push-button reset

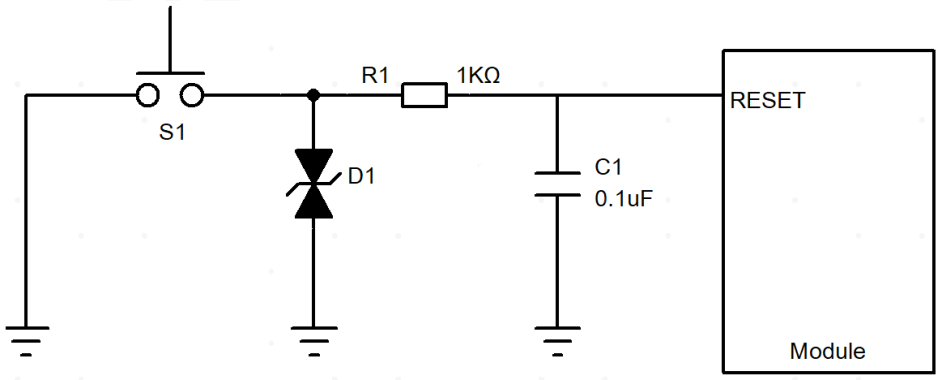
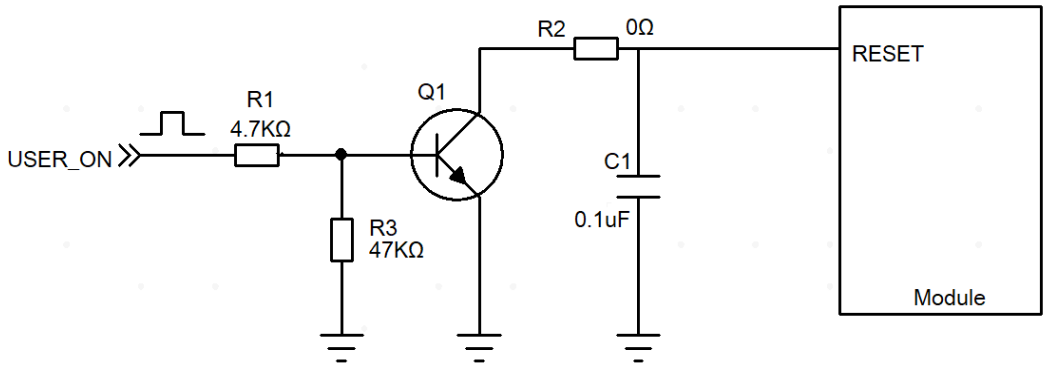
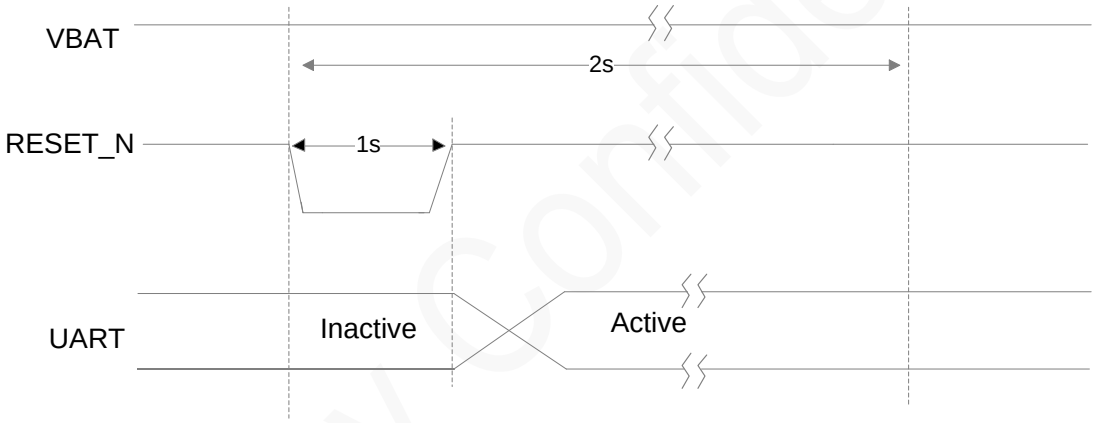


Figure 4-9 Reset circuit with triode separating



N25 module reset process.

Figure 4-10 N25 module reset process



4.3 Peripheral Interfaces

N25 offers a variety of peripheral interfaces.

In all reference designs in this chapter, the signal direction in the pin naming is based on the perspective of the device itself. For instance, the TXD pin means the module transmits data from this pin, while the MCU_RXD pin indicates the MCU receives data through it. Connect these pins to enable signal flow. VCC_IO is the MCU's IO voltage, and VDD_2P8 is the module's IO voltage.

In practical applications, please pay attention to the signal direction indicated in the pin naming of your chosen peripheral device.

4.3.1 UART

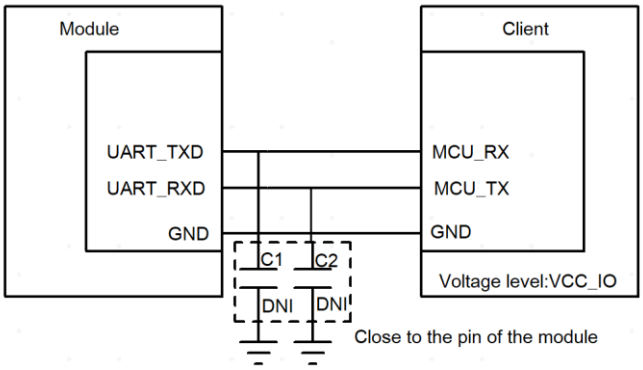
In complex electromagnetic environments, external electromagnetic interference may disrupt the N25 module's UART communication, causing communication issues. To address this, follow these design guidelines for the UART interface:

- Add capacitors between 5 and 10 pF in parallel with the module's UART_RXD and UART_TXD pins for reserved filtering.
- Keep PCB wiring as far from potential interference sources as possible.
- Route UART_RXD and UART_TXD traces on the inner layers of the PCB, maintain short trace lengths, avoid extensive routing on the top or bottom layers, and use a three-dimensional ground layout for these pins to enhance signal integrity.

Signal	Pin SN	I/O	Function	Remarks
UART1_TXD	1	DO	UART data output	• Used for AT communication. • For the RX pin, it is advisable to pre-connect an external pull-up resistor to VDDIO_2P8. It is essential to avoid keeping it consistently pulled low, as doing so can negatively impact both the startup process and the Power Save Mode (PSM) wake-up functionality.
UART1_RXD	2	DI	UART data input	

The N25 module offers a UART1 interface with a 2.8 V logical level. For detailed connection information, please refer to the relevant diagrams.

Figure 4-11 Reference design of the UART interface



Schematic Design Guidelines

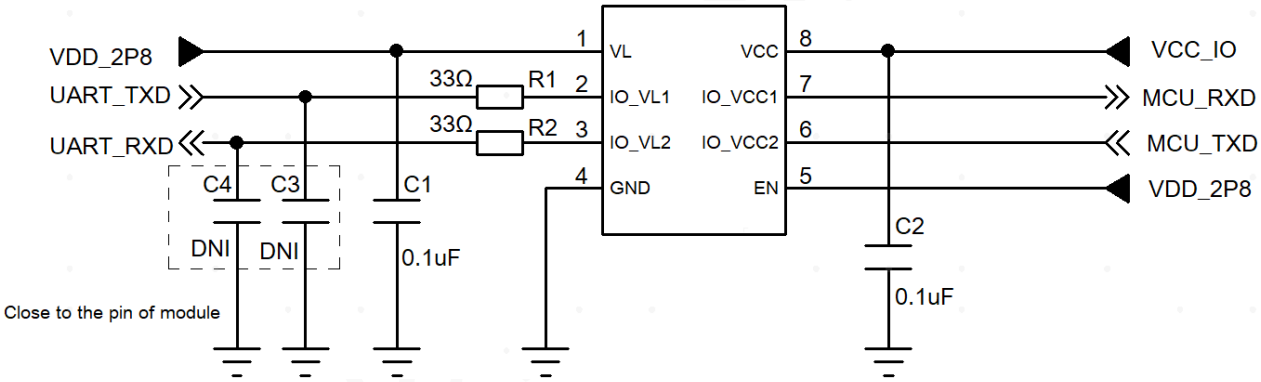
- Ensure signal flow direction matches the connection orientation.
- Use an external voltage-level translation circuit if the UART1 logic voltage doesn't match the MCU's. Avoid using diodes for level translation.
- It is advised to reserve positions for capacitors C1 and C2, typically 5 - 10 pF, adjusting as necessary based on testing.

Select one of three recommended circuits based on logic level and rate differences.

Adjust component values in these circuits based on actual test outcomes. Pay attention to the different types of voltage-level translation circuits.

Voltage-Level Translation Chip Circuit (Baud Rate > 115200 bps):

Figure 4-12 Recommended voltage-level translation circuit 1

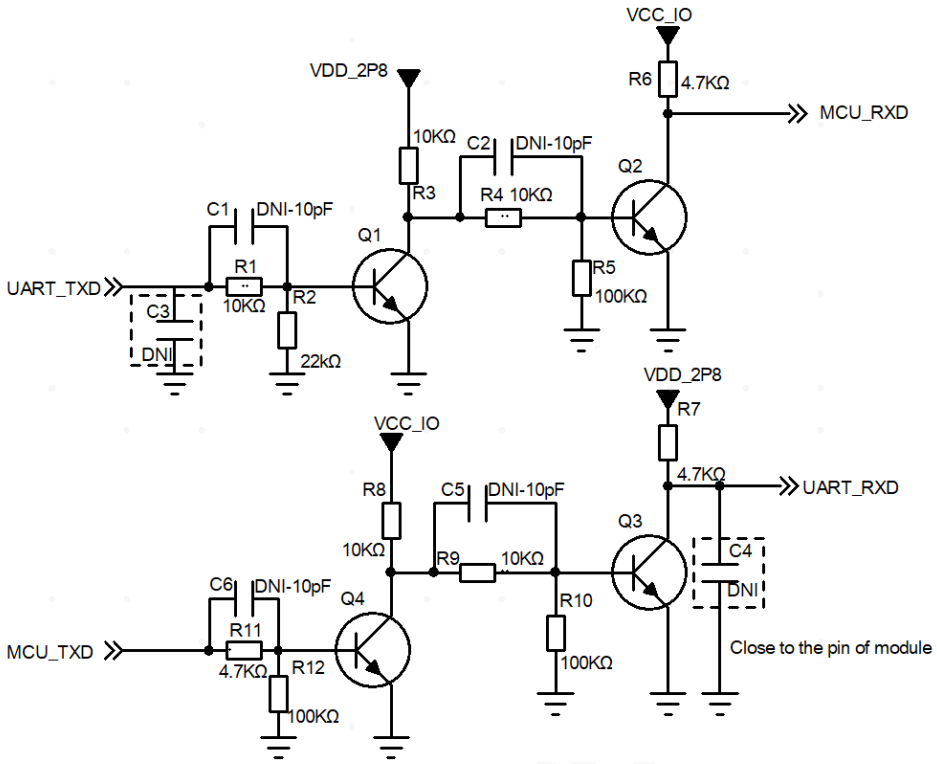


- VL: reference voltage for IO_VL1 and IO_VL2 (1.5 V - 5.5 V).
- VCC: reference voltage for IO_VCC1 and IO_VCC2 (1.5 V - 5.5 V).
- EN pin works at voltage > VL-0.2 V; directly connected to VDD_2P8, and the level translator chip is always working.
- Use capacitors C3 and C4, typically 5 - 10 pF, adjusting as necessary based on testing.

Dual-Triode Voltage-Level Translation Circuit (Baud Rate ≤ 115200 bps):

Design TXD and RXD ports by reference to Figure 4-13.

Figure 4-13 Recommended voltage-level translation circuit 2



The circuit translates the voltage through the turn-on and turn-off of the triode, and dual triode can achieve higher pressure difference after translation.

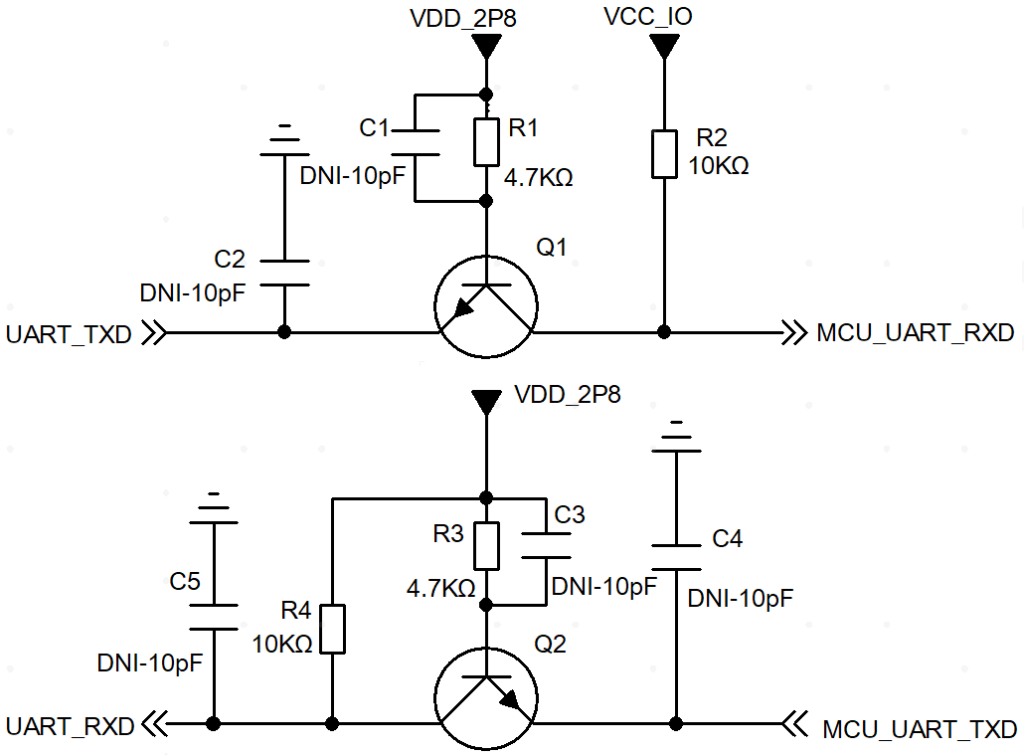
Schematic Design Guidelines

- Ensure the triode's base voltage operates within the specified temperature range for full conduction.
- Reserve acceleration capacitors (C1, C2, C5, C6) to potentially adjust the circuit's delay.
- Use capacitors C3 and C4, typically 5 - 10 pF, adjusting as necessary based on testing.

- Single-Triode Voltage-Level Translation Circuit:
- Design the serial port according to ‘Recommended voltage-level translation circuit 3’ as shown in Figure 4-14.

One-Way Voltage-Level Translation Circuit

Figure 4-14 Recommended voltage-level translation circuit 3



This circuit is a one-way translation solution, operating through the triode's conduction and cutoff. Please note the signal flow direction.

Schematic Design Guidelines

- Maintain the voltage difference between high and low levels below 2 V.
- Use an accelerating capacitor and adjust it according to test results.
- The base voltage of the triode is the lower voltage of the two sides.

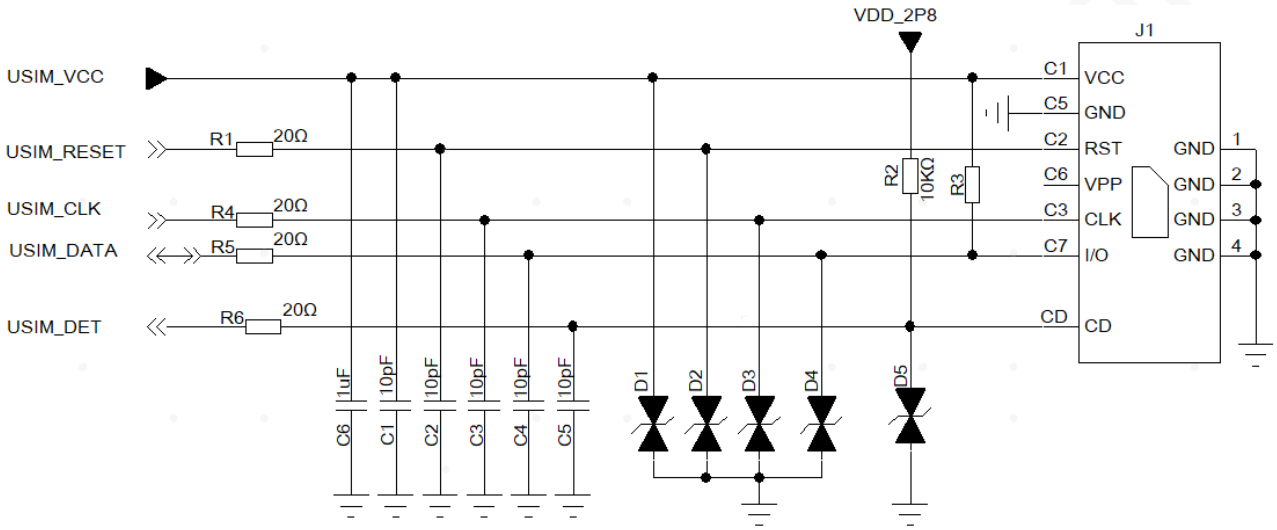
4.3.2 USIM

Signal	Pin SN	I/O	Function description	Remarks
USIM_DET	14	DI	USIM in-place detection	Leave this pin open if unused.
USIM_RESET	10	DO	USIM reset	-
USIM_CLK	12	DO	USIM clock output	-
USIM_DATA	11	DIO	SIM data input and output	A 10 kΩ resistor must be connected in series between this pin and USIM_VCC.

USIM_VCC	9	PO	SIM power output	Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented.

The N25 module provides one USIM card interface compatible with both 1.8 V and 3 V USIM cards, featuring adaptive voltage support. Figure 4-15 shows the reference design.

Figure 4-15 Reference design for the USIM card interface



Schematic Design Guidelines

- USIM_VCC serves as the USIM card's power supply, capable of supporting loads up to 30 mA. It should not be used for other purposes.
- Reserve a position for an external pull-up resistor, as SIM_DATA is not internally pulled up.
- USIM_CLK, the USIM card's clock signal pin, supports a 3.25 MHz clock frequency.
- In complex electromagnetic environments with high ESD protection needs, add ESD protection diodes (junction capacitance ≤ 7 pF) to each signal cable.
- Enhance ESD performance by connecting a series resistor (up to 20 Ω) between each USIM signal pin (USIM_DATA, USIM_RESET, USIM_DET, USIM_CLK) and the module.
- C1 - C5, parallel to each USIM signal trace, are for attaching high-frequency filter capacitors (capacitance ≤ 10 pF, adjusted as needed). These are not mounted by default.

PCB Design Guidelines:

- USIM signals can be disrupted by RF radiation, potentially causing SIM card detection failures. Position USIM signals away from the antenna and RF circuit areas.
- Place USIM card connectors near the module and keep USIM traces as short as possible.

- Place ESD protection resistors and components near the USIM card.
- It is recommended to surround USIM traces with ground to enhance EMC.

4.3.3 ADC

The N25 module offers a single ADC0 interface for acquiring external analog voltages. The ADC0 sampling range is from 0 to 1.8 V. It is strictly prohibited to input voltages exceeding 1.8 V into ADC0.

4.4 RF Interfaces

Signal	Pin SN	I/O	Function description	Remarks
ANT	25	AI/O	Antenna pin	50 Ω impedance characteristic.
ANT_BT	22	AI/O	BT/ WIFI antenna pin	50 Ω impedance characteristic.

4.4.1 Antenna Design

The ANT_MAIN/ ANT_DRX antenna interfaces of N25 require a 50 Ω impedance. To maintain RF performance, include a matching network(L type, T type, or π type) between the module interfaces and antennas. The π type network is recommended.

Figure 4-16 L-type RF matching schematic

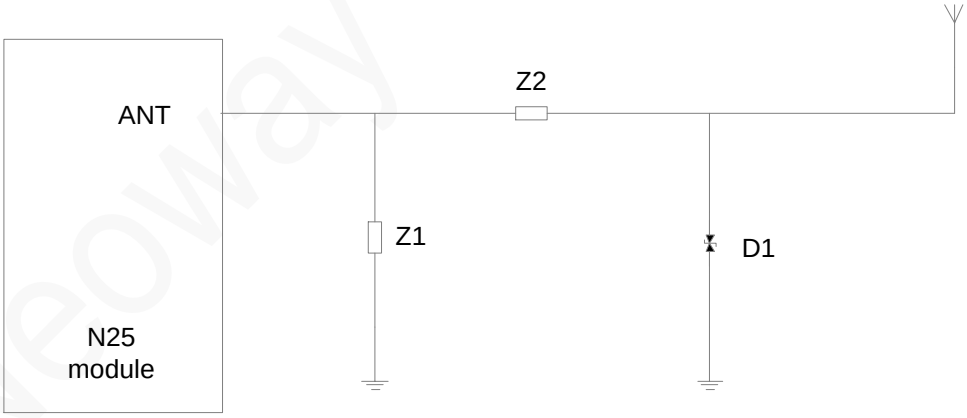


Figure 4-17 T-type RF matching schematic

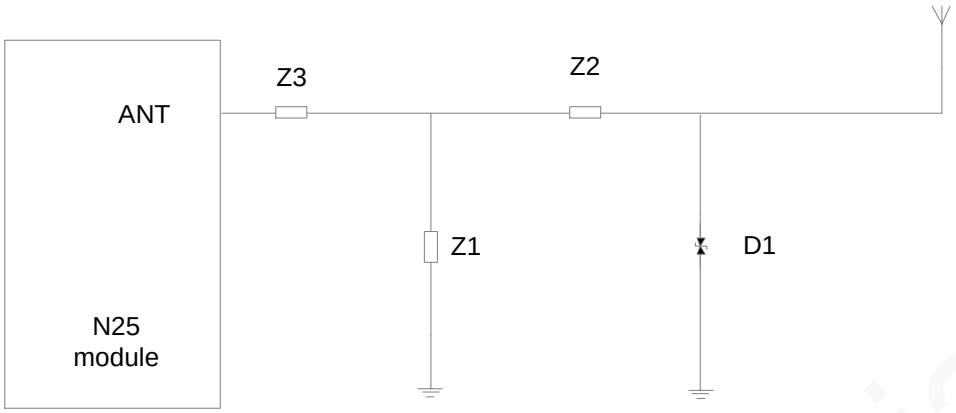
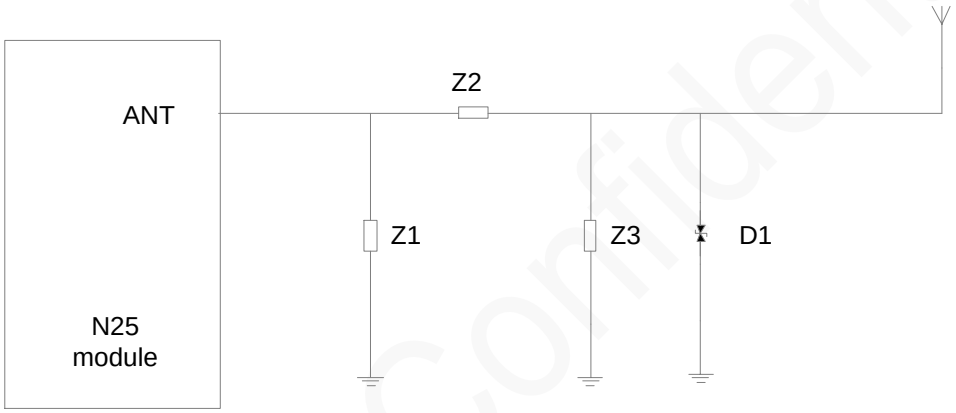


Figure 4-18 π-type RF matching schematic



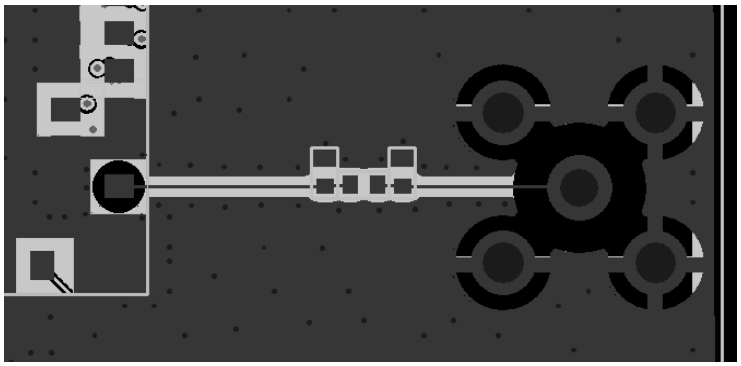
Schematic Design Guidelines

- The matching network's elements are capacitors, inductors, and 0 Ω resistors. Position these RLC components as close to the antenna interface as possible.
- To protect against static electricity from the antenna, add TVS components with ultra-low junction capacitance (≤ 0.5 pF). Ensure the TVS diodes' reverse breakdown voltage is above 15 V.

PCB Design Guidelines:

- Surround the RF connector with copper foil and add numerous ground holes to minimize ground impedance.
- Keep the trace between the RF pin and the module short, maintaining a 50 Ω impedance.
- If SMA connectors are used, avoid large RF solder pads that can create significant parasitic capacitance. Remove copper on the first and second PCB layers under the RF solder pad, as illustrated in Figure 4-19.

Figure 4-19 Recommended RF PCB design



- Distance RF signals and components from high-speed circuits, power supplies, transformers, large inductors, and clocks.

4.4.2 Antenna Assembly

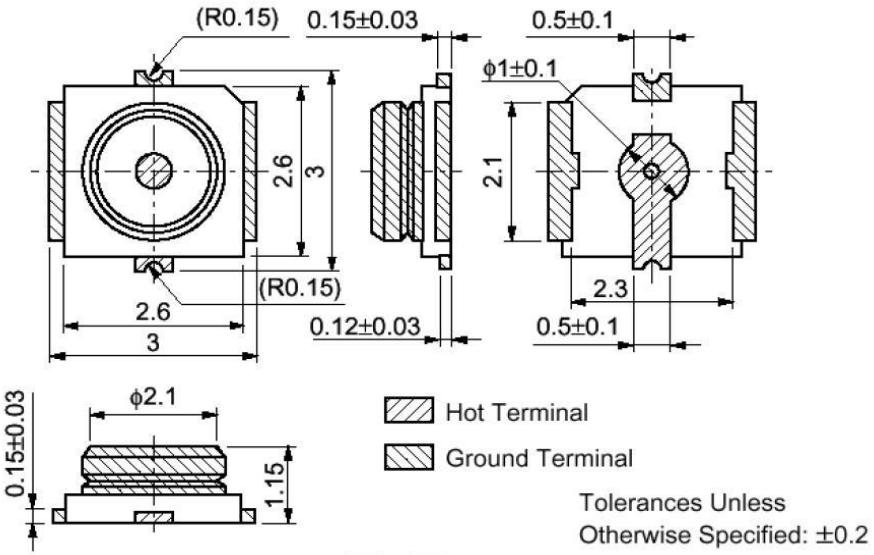
The antenna must meet mobile device standards with a standing wave ratio between 1.1 and 1.5, and an input impedance of 50 Ω. Optimal antenna performance typically involves higher in-band gain and lower out-of-band gain.

The module antenna interface can connect to rubber rod, sucker, or internal PIFA antennas. Ensure proper shielding between external antennas and RF pins. For RF cable connections, keep the external RF cables away from all interference sources, especially digital signals and switching power supplies.

The following methods are commonly used to assemble antennas:

- Connecting to a GSC RF connector
  Recommended model MM9329-2700RA1. The following figure shows its encapsulation specifications. The connection to the external antenna can be made through RF lines.

Figure 4-20 Murata RF connector encapsulation specifications



- The RF cable is connected to the module by soldered. Proper and sufficient soldering is crucial to prevent wire loss and ensure optimal RF performance.

The following figure shows the effect of the two connection methods.

Figure 4-21 RF cable connections

4.5 GPIO

The module is equipped with three GPIO ports, namely GPIO_1 and GPIO_2, with a high voltage level of 2.8 V.

Signal	Pin SN	I/O	Function description	Remarks
GPIO_1	34	IO	Generic GPIO	-
GPIO_2	35	IO	Generic GPIO	-
GPIO_3	36	IO	Generic GPIO	-

4.6 Other interfaces

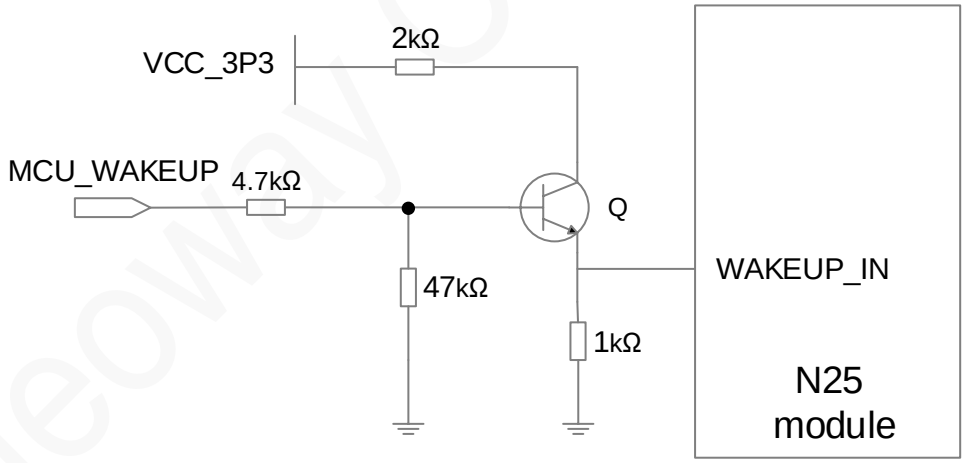
Signal	Pin SN	I/O	Function description	Remarks
WAKEUP_OUT	37	DO	Wake up external chips	-
WAKEUP_IN	39	DI	PSM wakeup control input	Active high
STATUS	42	DO	Startup indication	-
NET_LIGHT	33	DO	Network status indicator	-

4.6.1 WAKEUP_IN

WAKEUP pin is used to wake up the module PSM status. To initiate data transmission when the module enters PSM mode, users should actively pull the WAKEUP_IN pin high for at least 1 second to wake up the module. After waking up, the module won't automatically register on the network. Users must send a data transmission request from their side, utilizing AT commands. If there is no data transmission request, the module will re-enter PSM mode. For detailed usage instructions, please refer to *Neoway_N25_AT_Commands_Manual*.

For the reference design of WAKEUP_IN, see Figure 4-22.

Figure 4-22 Reference circuit connection of WAKEUP pin



4.6.2 WAKEUP_OUT

This interface serves to awaken external chips and is used as an output. Its usage aligns with that of GPIO, with a high voltage level set at 2.8 V.

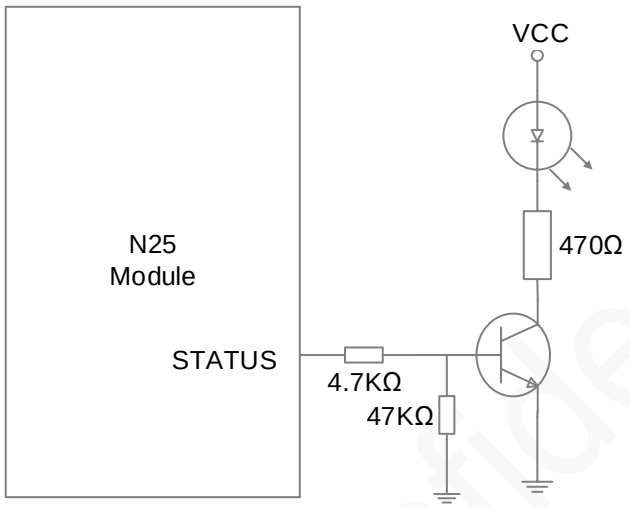
4.6.3 STATUS

In the N25 module design, the STATUS signal indicates successful power-up. When the module is off,

this pin has a low voltage level. Once the module successfully powers up, the voltage level of this pin rises to 2.8 V. For a visual representation of the power-on status, you can drive a LED using a transistor, as shown in reference Figure 4-23.

For details, see *Neoway_N25_AT_Commands_Manual*.

Figure 4-23 Driving LED with a triode



5 Electrical Characteristics and Reliability

This chapter describes the electrical characteristics and reliability of the N25 module, including the input and output voltage and current of the power supply, current consumption of the module in different states, operating and storage temperature range, and ESD protection characteristics.

5.1 Electric Features

Table 5-1 N25 operating conditions

Pin SN	Parameter	Minimum value	Typical value	Maximum value
VBAT	V_{in}	3.41 V	3.8 V	4.20 V
	I_{in}	/	/	2 A

- If the voltage is lower than the threshold, the module might fail to start. If the voltage is higher than threshold or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it outputs a current not less than 2 A.

5.2 Current Consumption

Table 5-2 N25 current consumption (Typical)

Network Status standard and band	Power (dBm)	PSM (μA)	Idle (DRX/eDRX) (mA)	Active (mA)	
				TX	RX
Cat NB: B3, B5, B8, B20, B28	23	<4.5	1.7/1	230	30
	0	<4.5	1.7/1	61	30
	-10	<4.5	1.7/1	43	30

5.3 Temperature Characteristics

Table 5-3 N25 temperature characteristics

Status	Min. value	Typical value	Max. value
Operating	-40℃	25℃	85℃
Storage	-45℃	/	90℃

If the ambient temperature exceeds the operating temperature of the module, some individual RF indicators of the module may deteriorate, but it will not have a major impact on the normal use of the module.

5.4 ESD Protection Characteristics

Electronic products generally need to undergo strict ESD testing. The following is the ESD protection capability of the main pins of the module. When designing related products, customers need to add corresponding ESD protection according to the industry where the product is used to ensure product quality.

Test environment: humidity 45%; temperature 25 ℃

Table 5-4 N25 ESD protection characteristics

Contact point	Contact discharge	Air discharge
VBAT	±8 KV	±15 KV
GND	±8 KV	±15 KV
ANT	±8 KV	±15 KV
Shielding cover	±8 KV	±15 KV
Others	±2 KV	±4 KV

6 RF Characteristics

This chapter details the RF related characteristics including the frequency bands, TX power and RX sensitivity of the module.

6.1 Operating Frequency Bands

Table 6-1 N25 operating frequency bands

Mode	Operating frequency band	Uplink	Downlink
Cat-NB1/Cat-NB2	HD-FDD-LTE B3	1710 - 1785 MHz	1805 - 1880 MHz
	HD-FDD-LTE B5	824 - 849 MHz	869 - 894 MHz
	HD-FDD-LTE B8	880 - 915 MHz	925 - 960 MHz
	HD-FDD-LTE B20	832 - 862 MHz	791 - 821 MHz
	HD-FDD-LTE B28	703 - 748 MHz	758 - 803 MHz
GPRS	GPRS850	824 - 849 MHz	869 - 894 MHz
	GPRS900	880 - 915 MHz	925 - 960 MHz
	GPRS1800	1710 - 1785 MHz	1805 - 1880 MHz
	GPRS1900	1850 - 1910 MHz	1930 - 1990 MHz

6.2 TX Power and RX Sensitivity

Table 6-2 N25 RF transmitting power

Band	Max Power	Min. Power
HD-FDD LTE B3	23dBm+2/-2dB	<-40dBm
HD-FDD LTE B5	23dBm+2/-2dB	<-40dBm
HD-FDD LTE B8	23dBm+2/-2dB	<-40dBm
HD-FDD LTE B20	23dBm+2/-2dB	<-40dBm
HD-FDD LTE B28	23dBm+2/-2dB	<-40dBm

GSM850, EGSM900	33 dBm+2/-2 dB	/
DCS1800, PCS1900	30 dBm+2/-2 dB	/

Table 6-3 N25 Cat NB1/Cat NB2 (no retransmission)/GPRS receiving sensitivity

Band	REFSENS	Duplex Mode
LTE B3, B5, B8, B20, B28	≤-113dBm@200KHz ≤-123dBm@15KHz	HD-FDD
GSM850/EGSM900/DCS1800/PCS1900	＜-108 dBm@200KHz	FDD

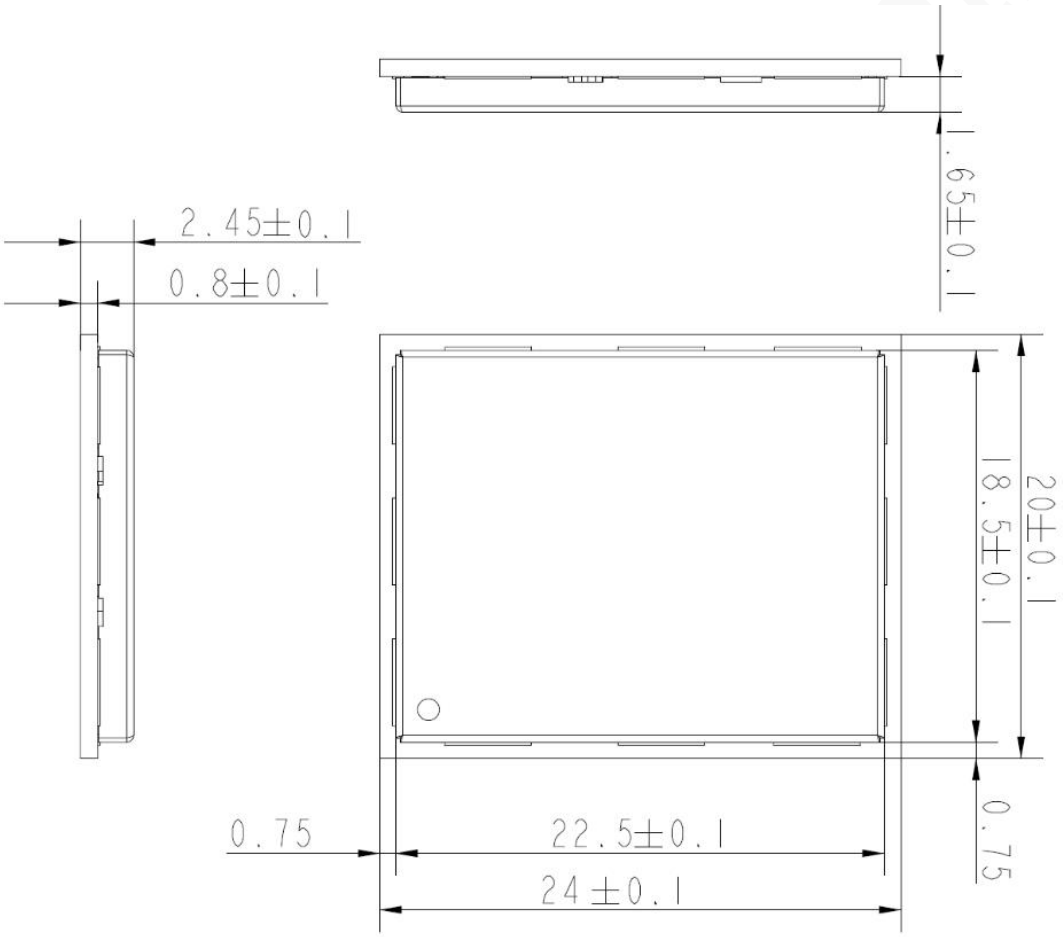
The module's transmission power and reception sensitivity are measured through RF conduction tests conducted in a laboratory. These tests involve connecting the module to an RF comprehensive tester and using the MT8821C, providing results for reference.

7 Mechanical Characteristics

This chapter describes the mechanical features of N25, such as dimensions, labels, and packaging.

7.1 Dimensions

Figure 7-1 N25 Top and side view dimensions (unit: mm)



7.2 Labeling

The label is printed using anti-deformation, anti-fading and high-temperature resistant materials, and can withstand a high temperature of 260°C.

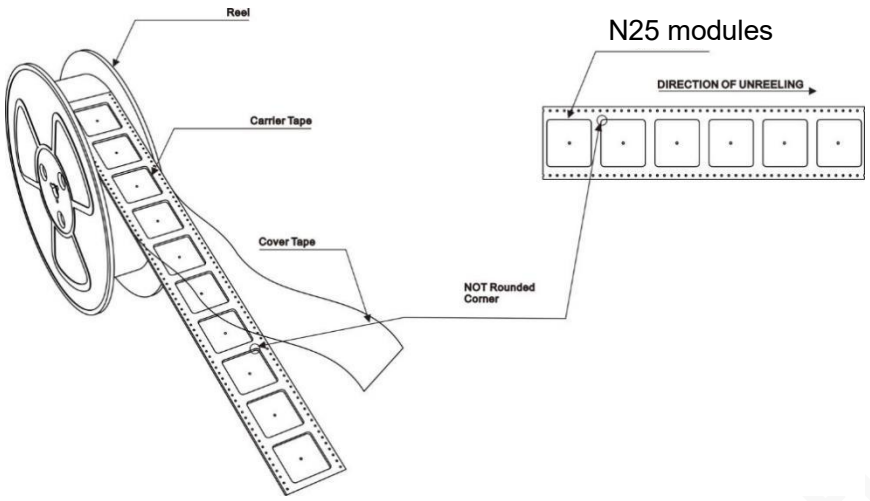
- The preceding label is for reference only, the actual effect is subject to the actual product.
- The silk-screen printing must be clear. No blur is allowed.
- The material and surface finishing must comply with RoHS directives.

7.3 Packaging

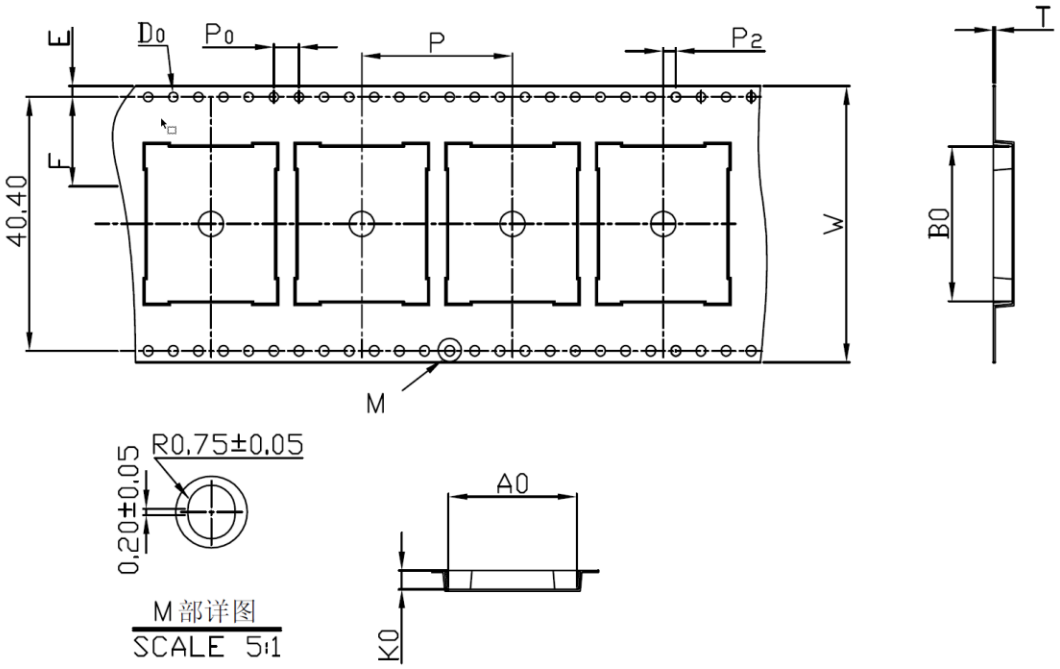
The N25 module adopts the SMT method for oven soldering. To prevent the products from being damp before they are delivered to customers, the tray is used for moisture-proof packaging. The aluminum foil bag, desiccant, humidity indicator card, tray, vacuum and other processing methods are used to ensure the dryness of the product and extend its service life.

7.3.1 Tape&Reel

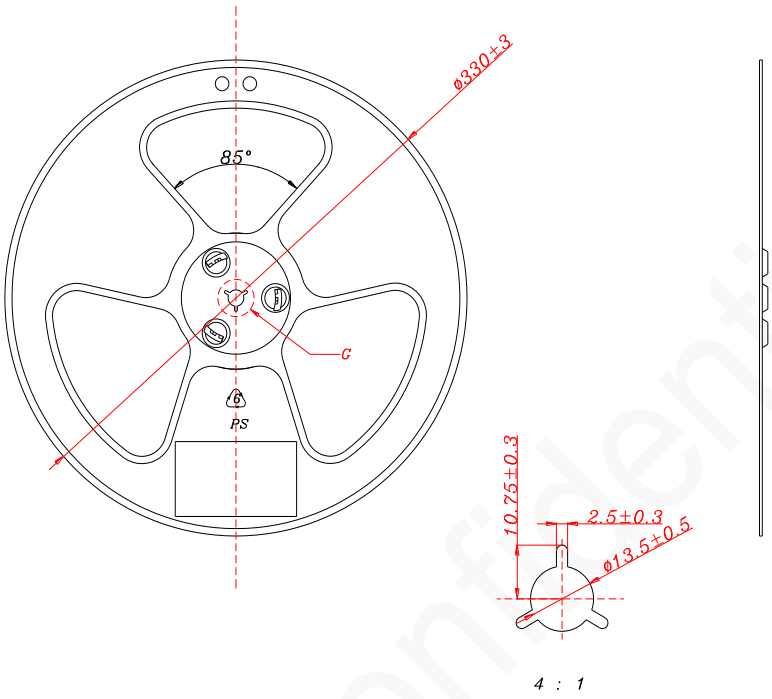
Neoway modules are delivered as reeled tapes as shown below:



Tape Dimensions



Reel Dimensions



7.3.2 Moisture Sensitivity Level

N25 is a level 3 moisture-sensitive electronic element, in compliance IPC/ JEDEC J-STD-020 standard.

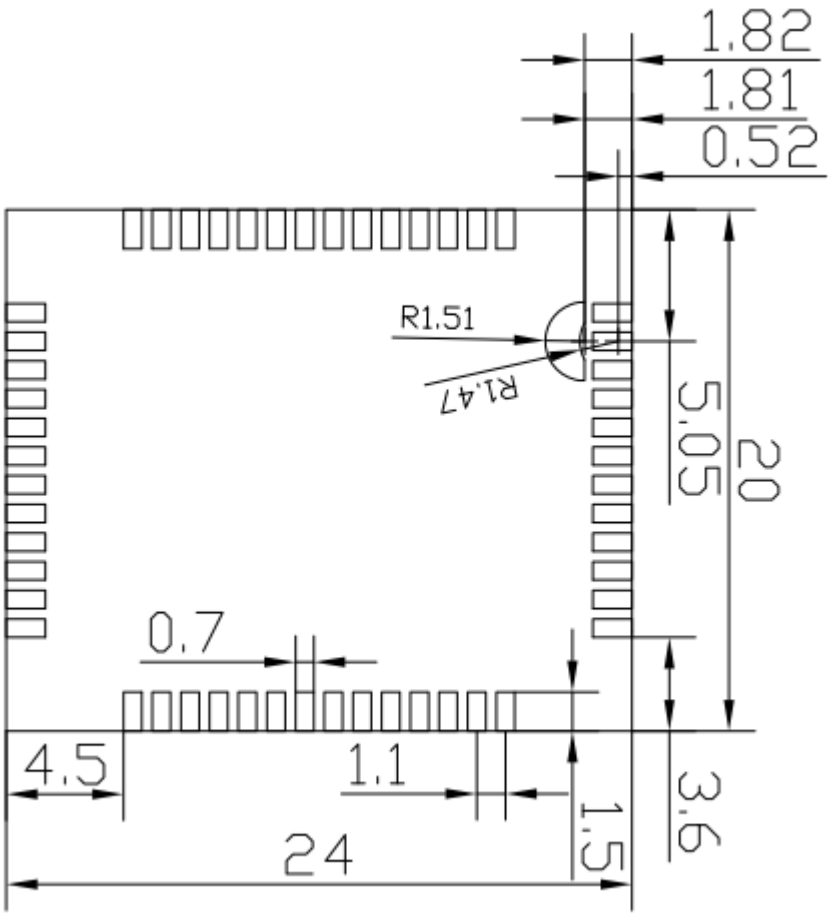
After unpacking, avoid leaving the module exposed to air for too long. If exposed to air for a long time, the module could become damp, increasing the risk of damage during reflow soldering or laboratory soldering. Bake it before mounting the module. The baking conditions depend on the moisture degree. It is recommended to bake the module at a temperature higher than 90 degrees for more than 12 hours. In addition, since the package tray is made of non-high temperature resistant material, do not bake modules with the package tray directly.

8 Mounting N25 onto Application Board

The N25 module is constructed with a 52-pin LGA package and is assembled using the SMD (Surface-Mount Device) soldering method.

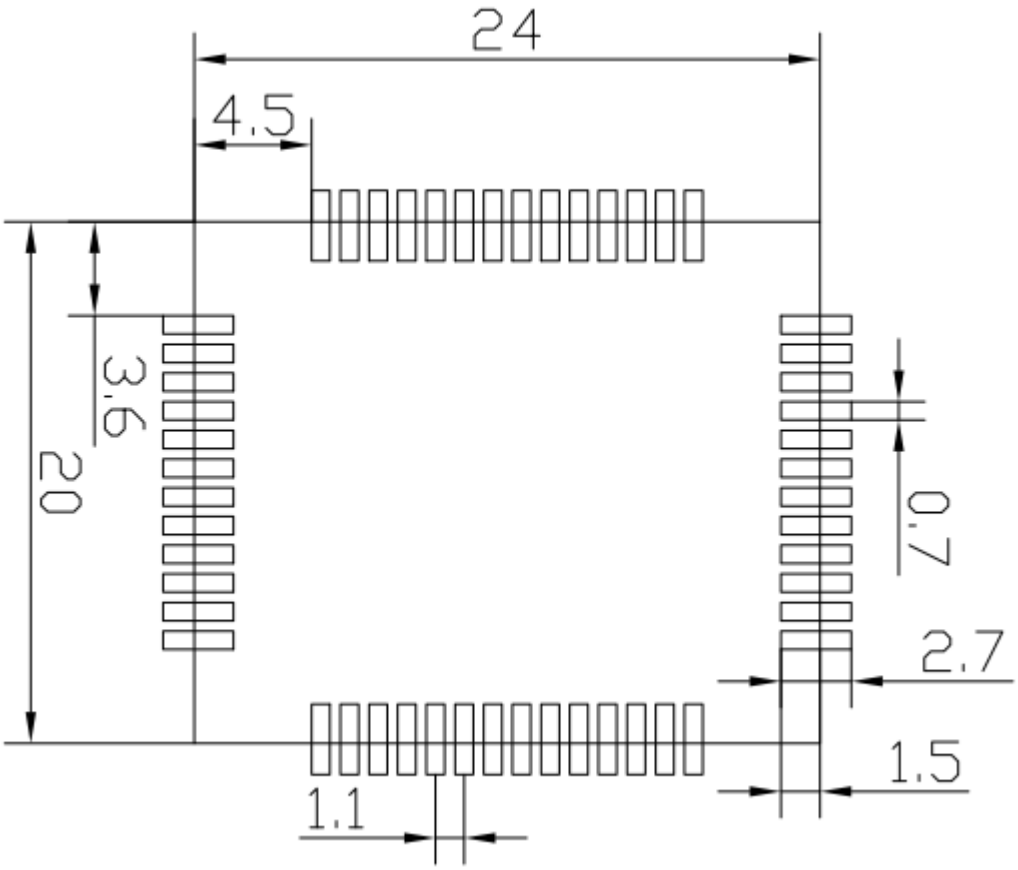
8.1 PCB Package

Figure 8-1 Bottom view of N25 PCB package (Unit: mm)



8.2 Application PCB Package

Figure 8-2 N25 Recommended PCB package (Unit: mm)



8.3 Stencil

The recommended stepped stencil thickness is 0.15 - 0.20 mm. Users may make minor adjustments based on the actual SMT performance.

8.4 Solder Paste

It is recommended to use the same kind of leaded solder paste used during the production process of Neoway.

- The melting point of the leaded solder paste is 35℃ lower than that of the lead-free solder paste, and the temperature in the reflow process is also lower than that of the lead-free solder

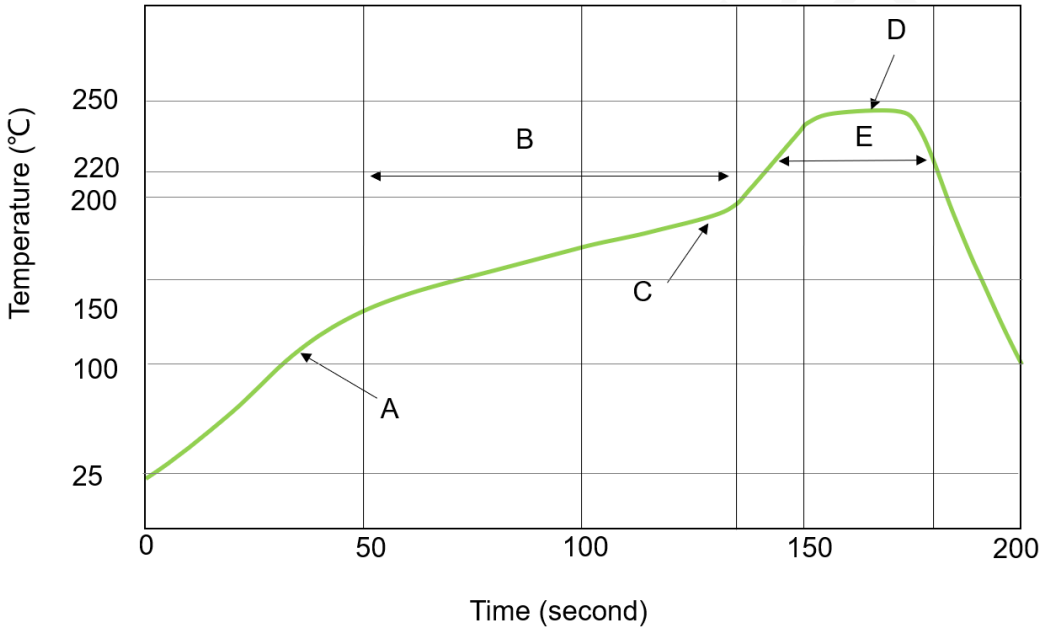
paste. Therefore, the soldering time is shorter accordingly, which easily causes a false solder because LCC/LGA in the module is in a semi-melted state during the secondary reflow.

- When using only solder pastes with lead, please ensure that the time above 220°C (reflow temperature) exceeds 45 seconds and the peak temperature does not exceed 240°C.

8.5 Oven Temperature Profile

If the PCB is large, it is important to avoid bending of the printed circuit material during an SMT process. So a bending prevention tool must be placed on the bottom of the printed circuit board. It is recommended to use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 8-3 Oven temperature profile



Technical parameters:

- Ramp up rate: 1 to 4 °C/sec
  Ramp down rate: -3 to -1 °C/sec
- Soaking zone: 150 to 180°C, Time: 60 to 100s
- Reflow zone: > 220°C, Time: 40 to 90s
- Peak temperature: 235 - 245°C

Due to abnormal temperatures, thermal sensitive devices may fail and cause other adverse effects. Neoway assumes no responsibility for such consequences.

For detailed precautions for storage and SMT of N25, See *Neoway Module SMT and Reflow Soldering Suggestions*.

When manually desoldering the module, use heat guns with a great opening, adjust the temperature to 245 °C (depending on the type of the solder paste), and heat the module till the solder paste is melted. Then remove the module using tweezers. Do not shake the module in high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

A Abbreviations

Abbreviation	Full name
ADC	Analog-Digital Converter
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCE	Data Communication Equipment
DTE	Data Terminal Equipment
PTW	Paging Time Window
PSM	Power Save Mode
DRX	Discontinuous Reception
eDRX	Extended Discontinuous Reception
EMC	Electromagnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electronic Static Discharge
ETSI	European Telecommunication Standard
FDMA	Frequency Division Multiple Access
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MS	Mobile Station
PCB	Printed Circuit Board
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
TVS	Transient Voltage Suppressor
RTC	Real Time Clock
SIM	Subscriber Identification Module
SRAM	Static Random Access Memory

TDMA	Time Division Multiple Access
UART	Universal asynchronous receiver-transmitter
VSWR	Voltage Standing Wave Ratio